

DAPHNE Status and Plans

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Outline

- Introduction
- 1 channel self-triggering
- 40 channels self-triggering and data Tx using GbETH
- Self trigger works for positive and negative slopes
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- CI

Introduction

All tests mentioned in this presentation were performed using DAPHNE and the gateway developed at EIA University.

To simulate a change at the AFE inputs, I have just configured all AFE's with some of the training patterns. So first, I configured them to transmit 14 bits in low state(CFG AFE ALL ZEROS), and afterwards I configured them to transmit 14 bits in high state(CFG AFE ALL ONES) to cause a trigger action. The other way around also works . I.e. [0's→1's or 1's → 0's]

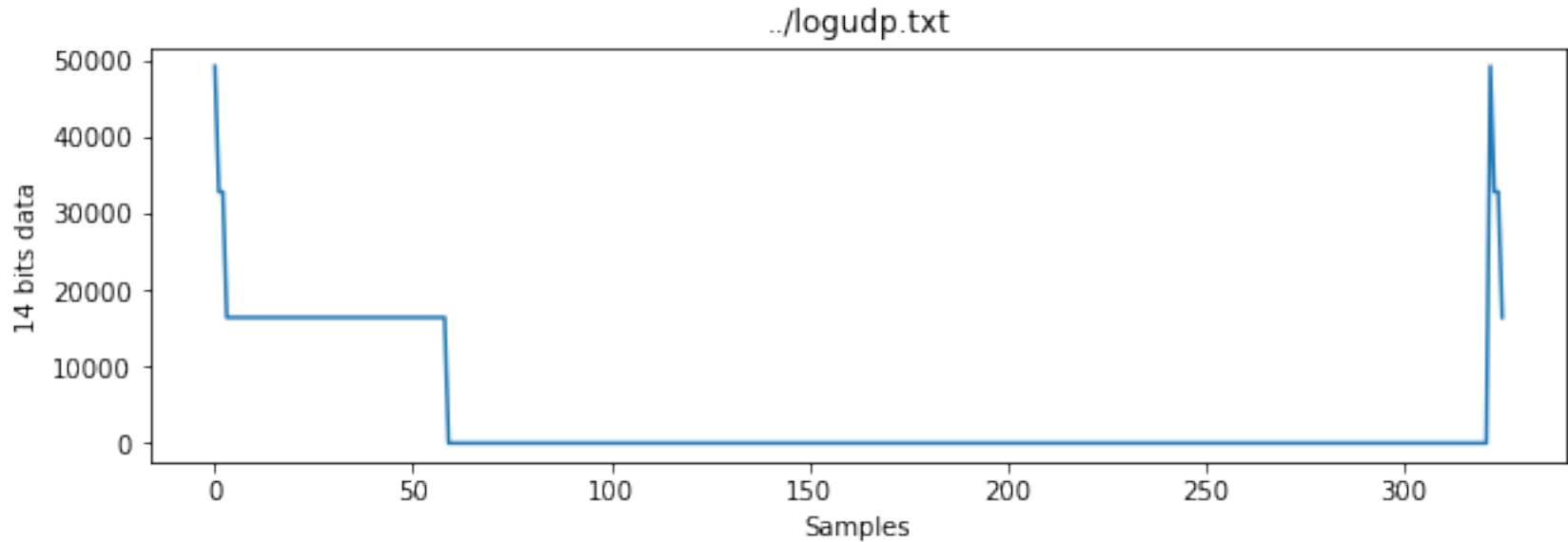
A change of around 40adc counts will make the self-triggering algorithm to trigger and record the signal, just to be sent afterwards using Gb Ethernet.

CI

Self-trigger working with 1 channel

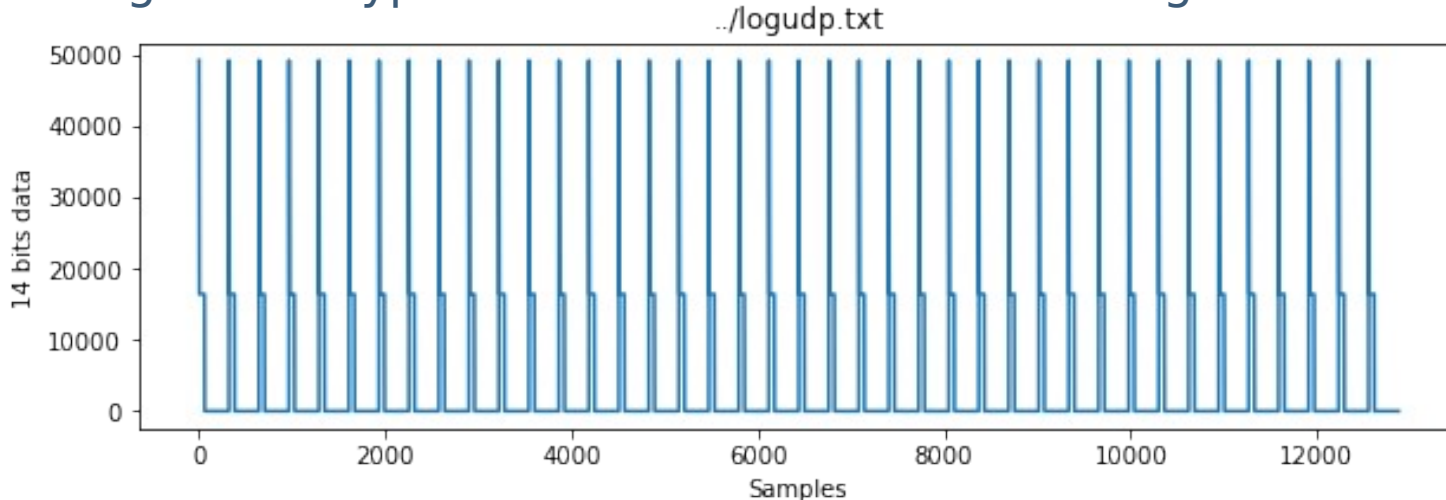
One channel self-trigger, caused by a change from 1's → 0's

Note that each waveform is formed by 320 data.



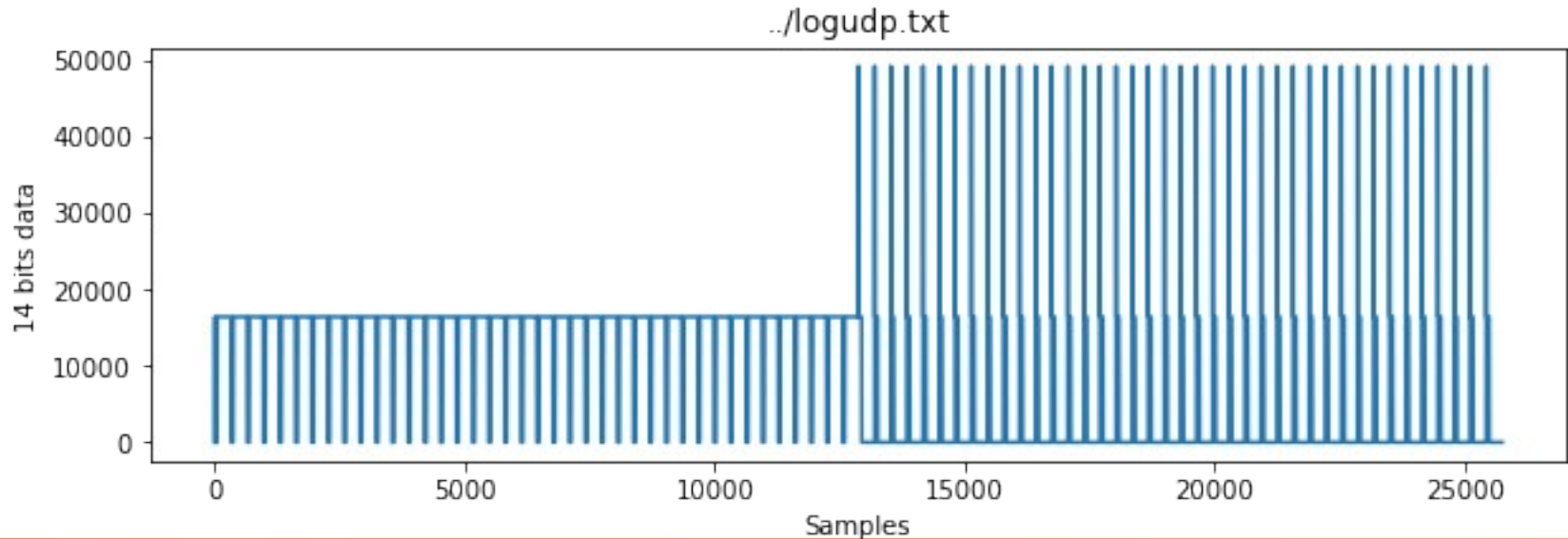
Self-trigger working with 40 channels

- 40 channel self-trigger, caused by a change from 1's → 0's
- Daphne sends all channels, one after the other, on which there was a trigger condition. In this case 40 at once.
- The spikes present in the plot, they are just an additional 2 bit representing a data-type needed on the full-mode integration.



Self-trigger works for positive and negative slopes

- Trigger its done just be changing the training patterns from all 0's to all 1's and vice-versa.



Conclusions

- The self-trigger functionality has been successfully tested on daphne board using AFE's training patterns.
- By using EIA University gateway approach, 40 channels have been instantiated and tested with promising results.
- All 40 self-triggering state machines work, all 40 independent FIFO's work as expected, and all data can be retrieved by using gigabit ethernet.

Future work

- Fine tuning has to be done on the state machine to transmit data using the Gigabit Ethernet.
- Integration with the full-mode developed by Carlos Montiel is imminent. Nevertheless, most FPGA modules are in place to perform this important phase.

- CI

Thanks!