DUNE Timing System Update 2023

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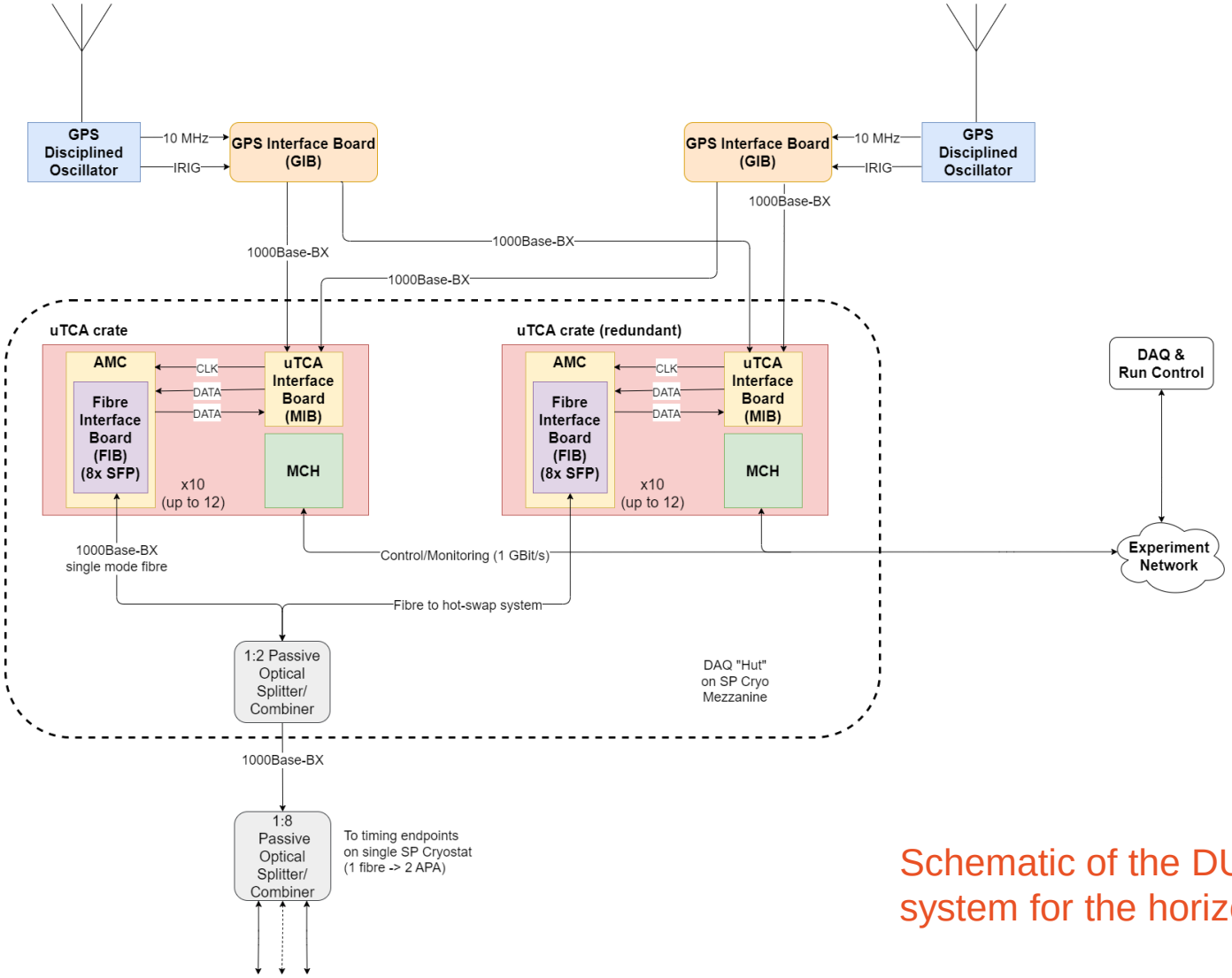
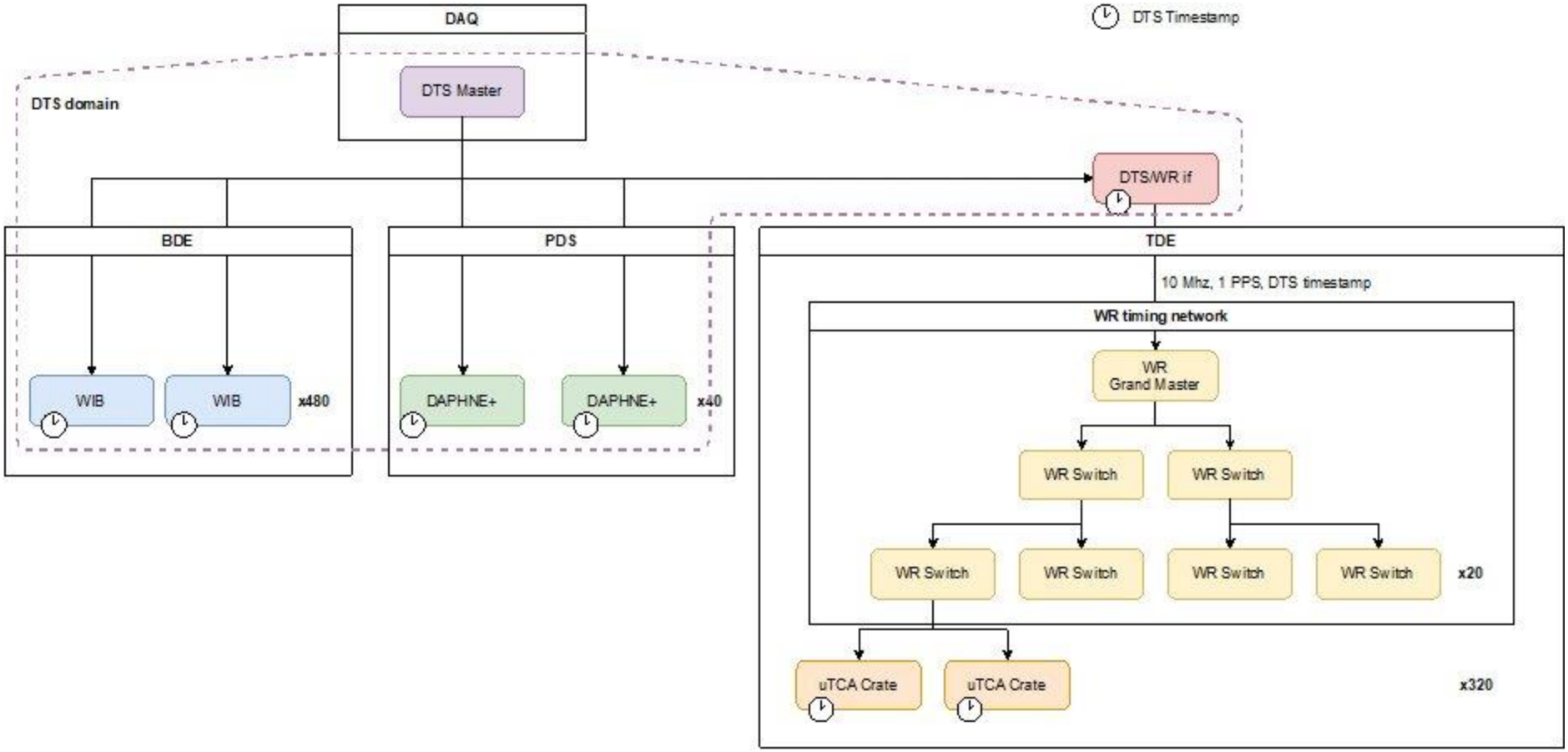
Overview - HD



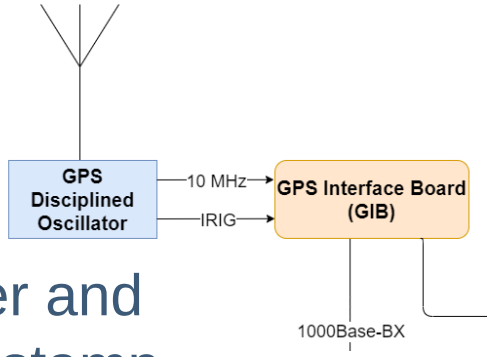
Schematic of the DUNE timing system for the horizontal drift module

Overview - VD



Schematic of the DUNE timing system for the vertical drift module

GPS Interface Board

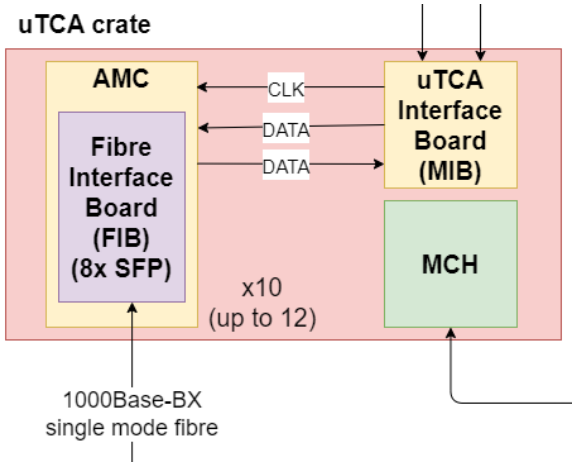


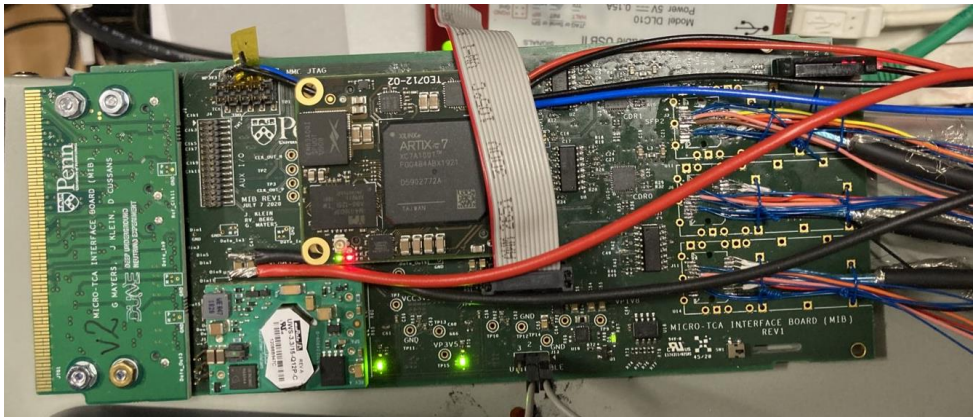
- Receives time data from a GPS receiver and generates a DUNE Timing System timestamp
- Hardware installed at ProtoDUNE and driven with WR-len to imitate a GPS receiver
  - GIB hardware also at University of Bristol and University of Pennsylvania

- GPS IRIG-B time code decoder and timestamp initialisation block integrated into design
- Loopback design in place and tested
- Software supplied to read/write registers for board/firmware setup and testing

MicroTCA Interface Board

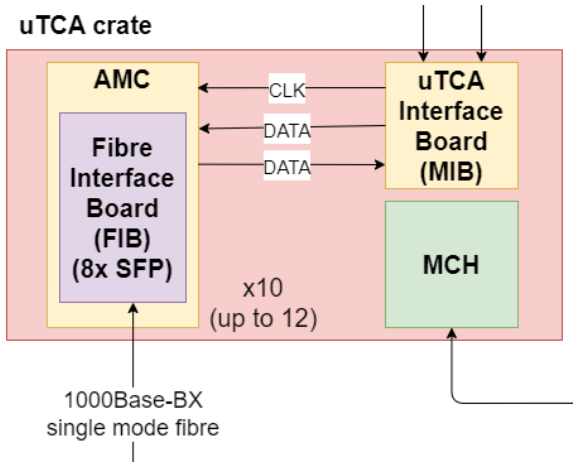
- Receives clock data from a GIB through a fibre
- Transmits timing data to FIBs through the backplane of the μTCA crate
- Acts as a master able to inject commands
- Tests have demonstrated it can broadcast data downstream
- A hardware redesign is in progress
  - This has been delayed, work began December 2022

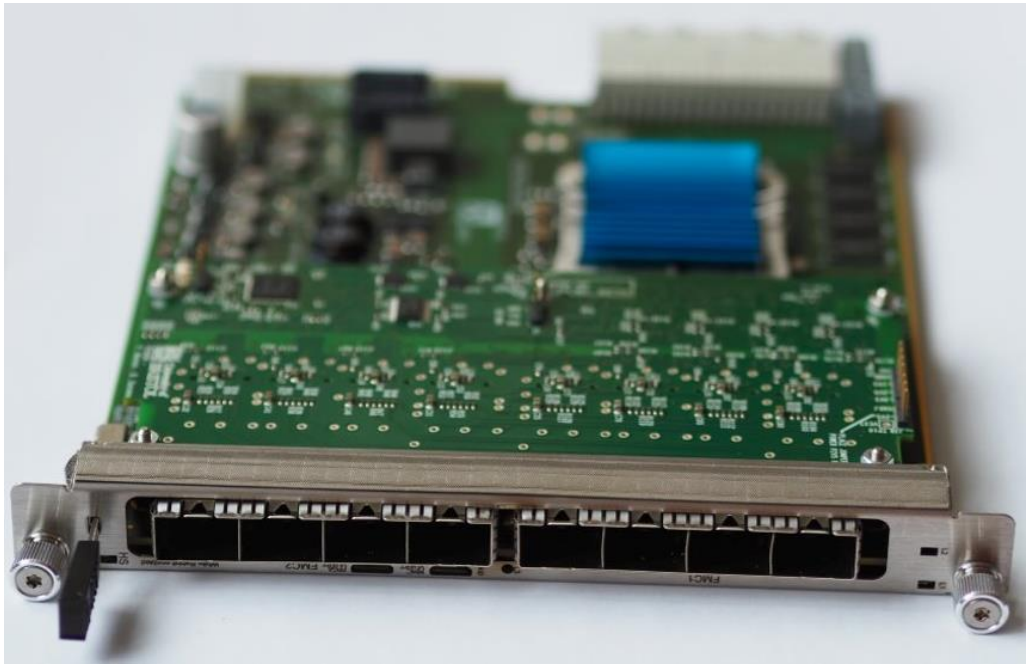




Fibre Interface Board

- Receives timing data from the back-plane of the µTCA crate
- Acts as an active fanout with eight SFP slots
- Shown to be able to transmit timing data from an upstream source using the old protocol via back-plane receive + transmit data





Production for DUNE far detectors

- Long delays in obtaining boards: MIB and FIB use off-the-shelf boards not expected to be available until 2024
- We need our hardware to be installed and ready before other hardware is installed
- Reserved enough FPGA chips as a back-up if problems with obtaining hardware persist
  - This will require significant redesigns for the FIB and MIB

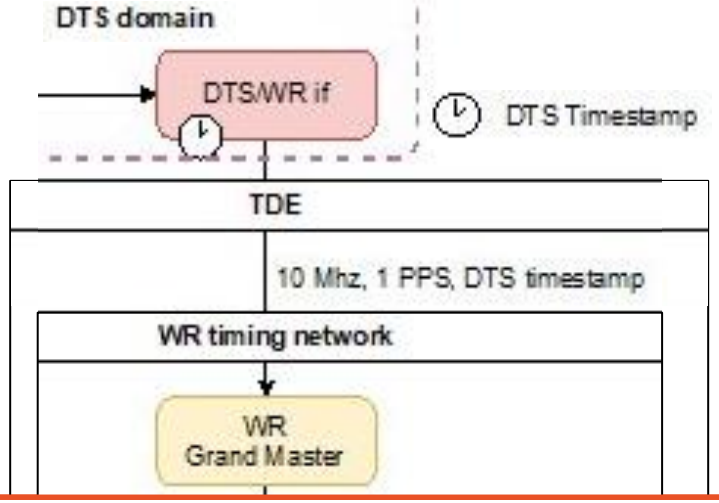
- A new version of the timing FMC, with no CDR chip, has been produced and is available for use by other groups

No CDR chips

- Clock and Data Recovery (CDR) chip previously used (ADN2814) is hard to find
- Developed a new protocol which is not reliant on the chip by using duty cycle shift keying
  - arXiv:2210.15517 **[hep-ex]**
- Firmware blocks must be updated to use the new protocol
- New protocol was tested during integration week for:
  - Warm Interface Boards (receive data from APAs)
  - Central Trigger Board (Collects triggering information)
- GIB, MIB, and FIB firmwares need to be updated (FIB additionally needs hardware redesign)

VD Top Drift Electronics Timing

- The interface to all parts of the DUNE far detector is the DUNE timing system
- VD TDE uses White Rabbit (IEEE-1588) to synchronise their readout
- To assist the VD TDE at ProtoDUNE-II, we will provide a 10 MHz/1 pulse per second source, synchronised to the DTS
  - It has been demonstrated that the WR can lock to 10 MHz/1PPS produced by the DTS
  - Firmware developed by the University of Montreal



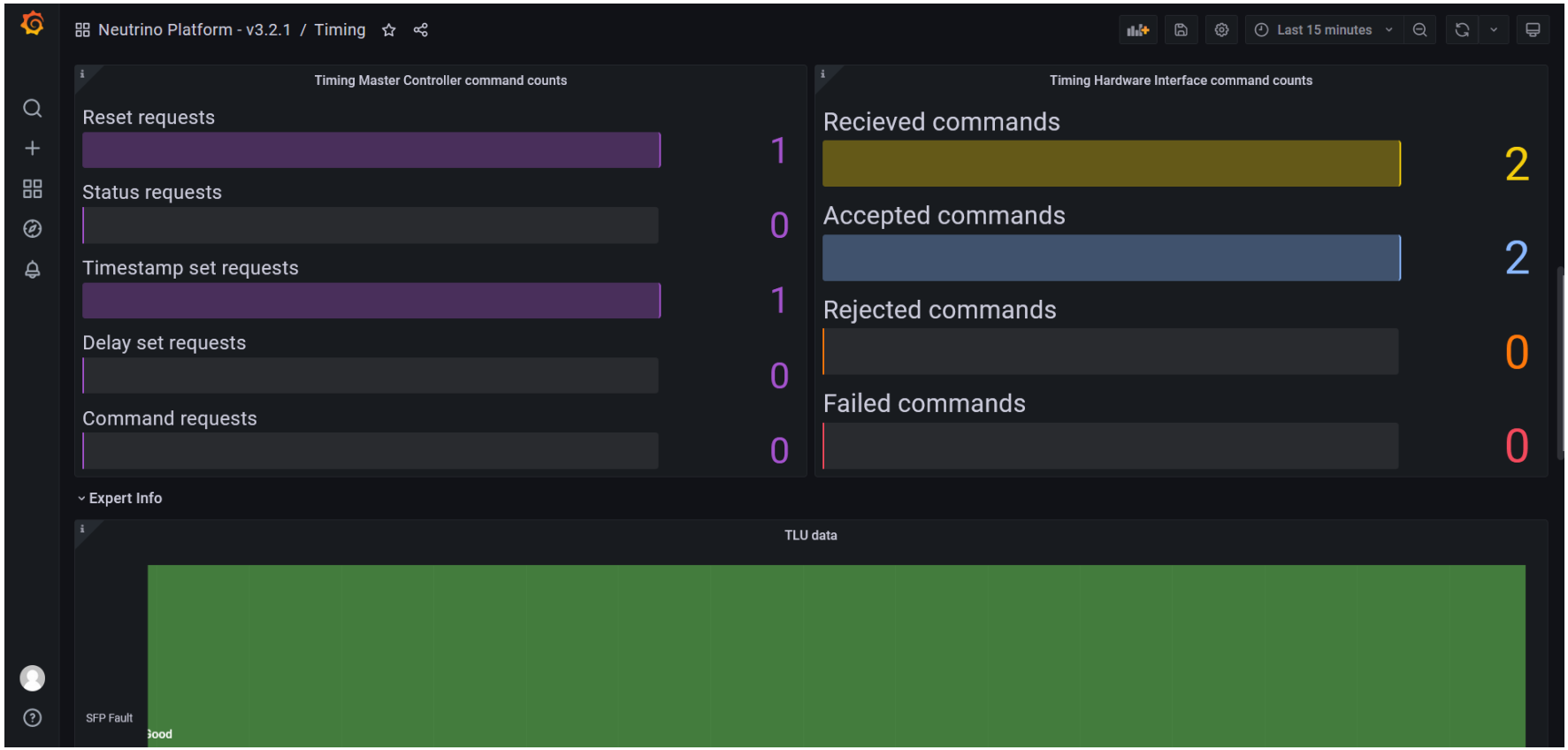
Firmware status

- Currently available firmware as follows:
  - Master - timestamp generation and command injection
  - Boreas - master with a Hardware Signals Interface (HSI) block
  - Endpoint - receives timestamps and commands
  - Ouroboros - master and endpoint in one device
  - Chronos - endpoint with HSI block
- To be implemented:
  - GIB with new timing protocol
  - MIB and FIB with updated hardware

Software updates

- Software updated to use the new protocol
- Core C++ libraries backwards compatible
- Commands interface reworked
  - 256 commands available, address as integers
  - The number of sent/received commands is recorded
- Running using nanoRC has received updated support
  - Currently implementing software state recovery – restarting a software session without affecting hardware
  - Endpoint monitoring service – regularly check delays and status of endpoints
  - Grafana page for monitoring timing sessions

Grafana


Neutrino Platform - v3.2.1 / Timing
Last 15 minutes
Timing Master Controller command counts
Reset requests
1
Status requests
0
Timestamp set requests
1
Delay set requests
0
Command requests
0
Timing Hardware Interface command counts
Recieved commands
2
Accepted commands
2
Rejected commands
0
Failed commands
0
Expert Info
TLU data
SFP Fault

Timing in 2023

- MIB and FIB hardware updates
- Port missing firmware designs to new protocol
- Support ProtoDUNE-II operations
- Continued support for readout and calibration system developers who are integrating with timing system

Summary

- New protocol has been developed to avoid reliance on a CDR chip
  - Firmware must be updated for GIB, MIB, and FIB
- MIB and FIB hardwares require updates
- Fallback plan against hardware procurement issues is prepared
- Preparations for ProtoDUNE-II are making progress

Backup

Documentation

- Start here guide: https://sparamesvaran.github.io/Dune-timing-documentation/Setting-up-the-FMC/
- Twiki page: https://twiki.cern.ch/twiki/bin/view/CENF/DTSOperations
- New protocol paper: https://arxiv.org/abs/2210.15517
- timinglibs wiki: https://github.com/DUNE-DAQ/timinglibs/wiki
- Guide to setting up DAQ software: https://github.com/DUNE-DAQ/daqconf/wiki/Instructions-for-setting-up-a-v3.2.x-software-area

New protocol nanorc session

- An example configuration file for setting up a timing session on a device using the new protocol:

```
{
  "boot": {
    "opmon_impl“: "cern“,
    "ers_impl": "cern"
  },
  "timing_hardware_interface": {
    "host_thi": "np04-srv-012",
    "firmware_type": "pdii",
    "timing_hw_connections_file": "${PWD}/timing_connections.xml"
  },
  "timing_master_controller": {
    "host_tmc": "np04-srv-012",
    "master_device_name": "PROD_MST_PC059_1_CH"
  }
}
```

Operational monitoring – enables Grafana page

Server the hardware interface is hosted on

Indicates to use the new firmware

Custom hardware connections if non-standard setup

Server the master controller is hosted on

Name of the device in the connections file

Testing scripts

- A series of scripts was developed to test a given set of hardware firmware and software
- Configuration files store the specific setup
  - Allows easy updating when new firmware/software is created
- Useful for regression testing
- Planned to be implemented in CI in 2023

Beam window

- GPS disciplined oscillators are expected to be consistent within 50ns
- Beam window is expected to a have scale of 1μs
- Timestamp the beam window from the accelerator in Fermilab
- Will allow triggering during beam window in the far detector modules

Duty cycle shift keying

- CDR chip would receive one signal stream, and outputs a clock and any incoming data
- Without the CDR chip, we need a protocol to do this in the FPGA
- The following protocol uses a signal stream which can change at 4x the clock frequency
- Each in each clock cycle, the signal will be on for ¾ a clock cycle for “1”, or ¼ a clock cycle for “0”