FPGA Readout commissioning at NP04

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Overview

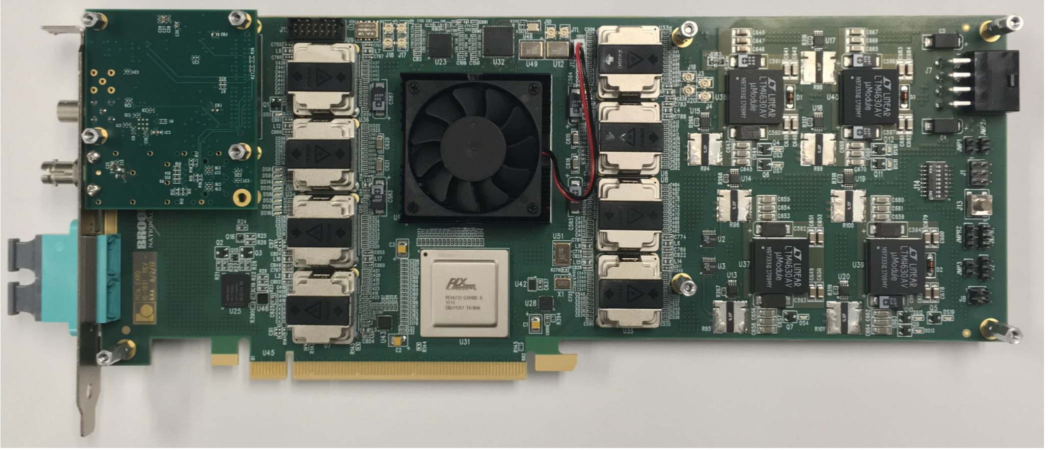
FPGA readout was designed to receive ADC data from the detector electronics of DUNE/ProtoDUNE, produce trigger primitives (TPs) using FPGA cards, buffer the incoming data and waits for a readout request from dataflow.

Readout commissioning at NP04 was done to bring FPGA readout into working order, insuring the system behaved according to specification in realistic conditions:

- Hardware installation/maintenance
- Readout firmware and software development
- Integration tests with readout firmware and software with detector electronics (APAs)
- Validation of data

FPGA readout: Hardware

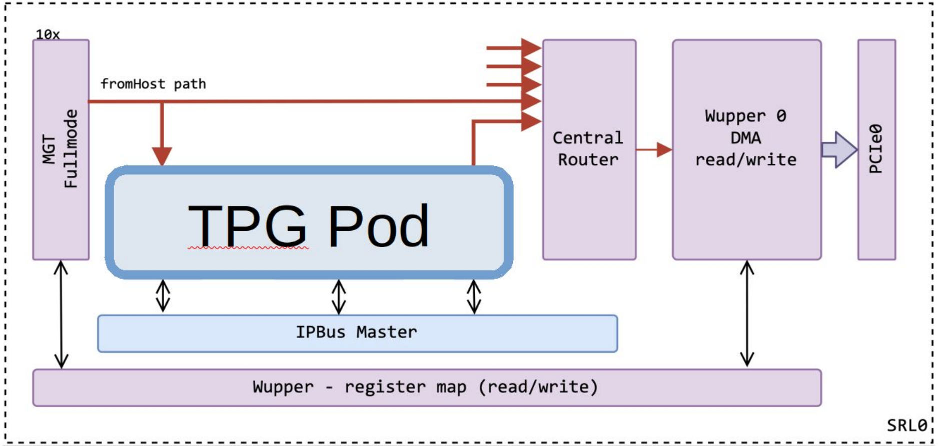
- Xilinx® Kintex® UltraScale FPGA on a board capable of supporting up to 48 optical links via MiniPOD transceivers, with a 16-lane PCIe Gen 3.0 interface.
- Supports a maximum transmission rate of 9.8Gb/s per link in the FULLMODE configuration
- In practice the amount of resources used depends on the front end (FE) being supported, e.g. readout of 1 APA use 10 optical fibre receivers to readout ADC data.



FELIX BNL-712 card

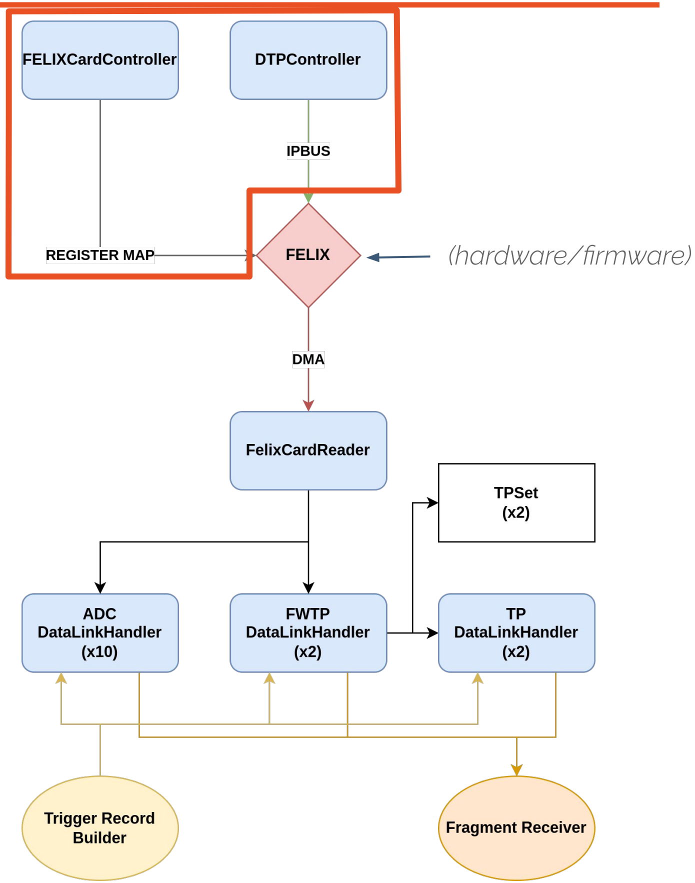
FPGA readout: Firmware

- Firmware developed at DUNE builds upon existing firmware designed by ATLAS TDAQ which handles overall functionality of the card
- Raw ADCs from the FE electronics are received via optical links (MGTs), and streamed to the direct memory access (DMA) and the TPG (Trigger Primitive Generation) pod.
- The TPG pod contains blocks which handle and process the raw ADCs, and produce firmware trigger primitives (FWTPs), which are then also sent to the DMA (See Antony Earle's talk for more)



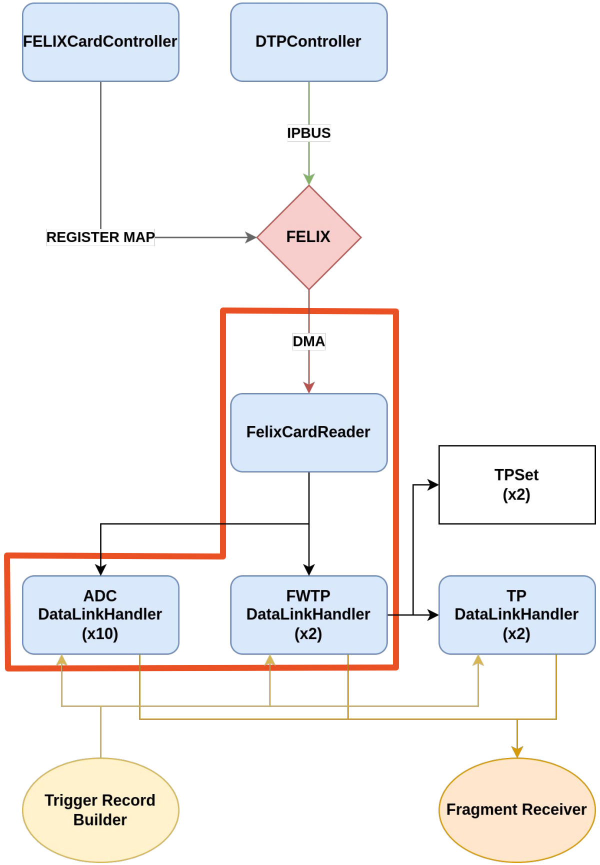
Blocks in blue were designed by FPGA readout

Readout DAQ application



- A readout application brings various software modules together to orchestrate the readout for a particular part of the detector (using APAs as an example)
- Modules which read/write register values to control and monitor the hardware/firmware:
    - FelixCardController - control and monitor the FELIX card
    - DTPController - control and monitor the TPG pod

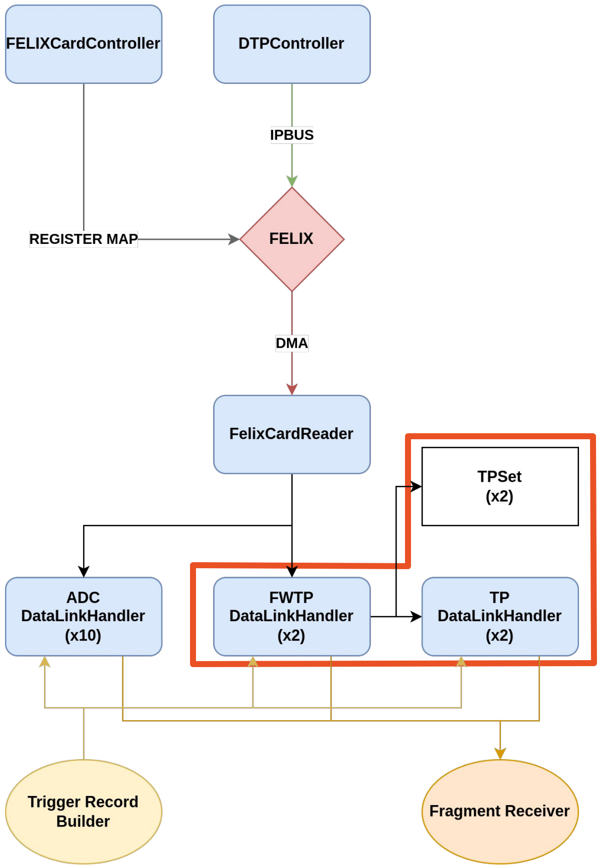
Readout DAQ application



- Modules to read data from memory and processing:
  - FelixCardReader - read data from DMA
  - DataLinkHandlers (DLHs) - buffers and, if needed, processes data

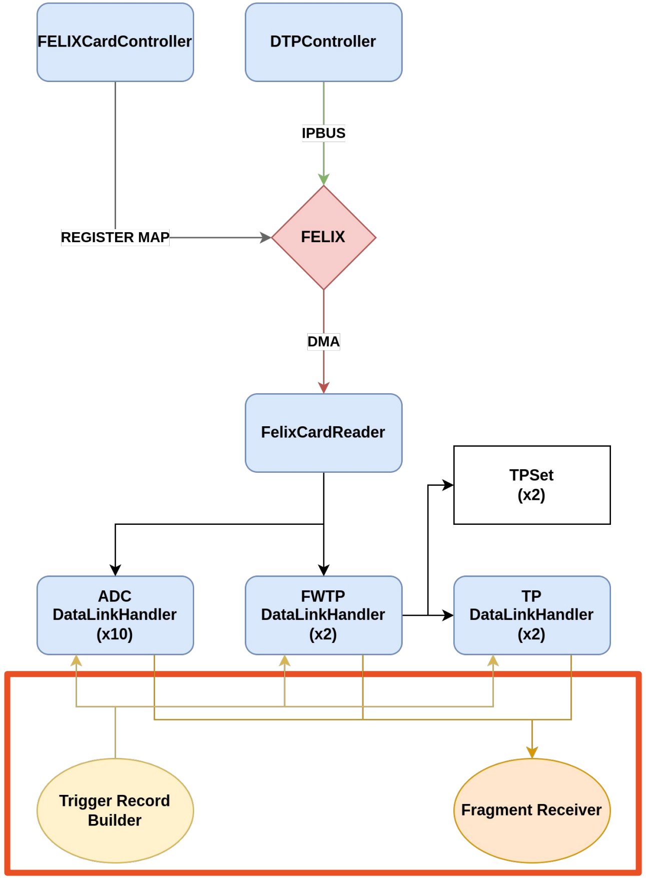
Readout DAQ application

- For ADC data no processing is needed, but firmware TPs are stitched together and reformatted to the TriggerPrimitive fragment type which is then sent to Trigger from the TPSet queue.



Readout DAQ application

- Once a trigger decision is made, a request from the trigger record builder (TRB) is made to each fragment producer (i.e. DLHs)
- Then, data in a given time window is sent to the fragment receiver (FR) and written to file in a trigger record.

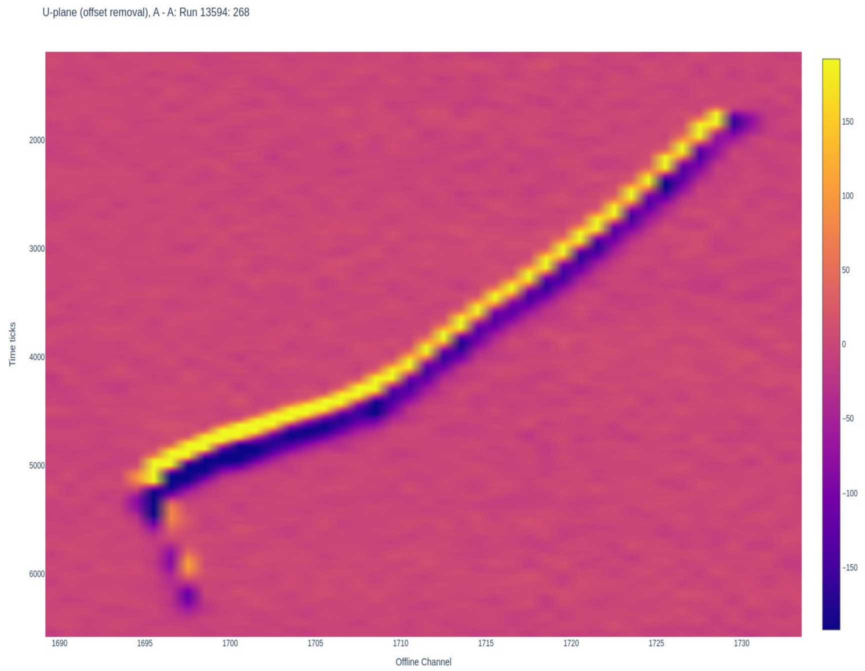


Commissioning timeline

- June 2022:
  - Vertical drift coldbox tests (1 FELIX)
- July-November 2022:
  - APA Tests in cold boxes and installation in the cryostat (1 FELIX)
- November 2022:
  - DUNEDAQ Integration week (5 FELIX cards)
    - 2 FELIX cards on np04-srv-028 for APAs 1 and 2
    - 2 FELIX cards on np04-srv-029 for APAs 3 and 4
    - 1 FELIX card on np04-srv-030 for the DAPHNE

Vertical Drift coldbox (dunedaq-v3.0.0)

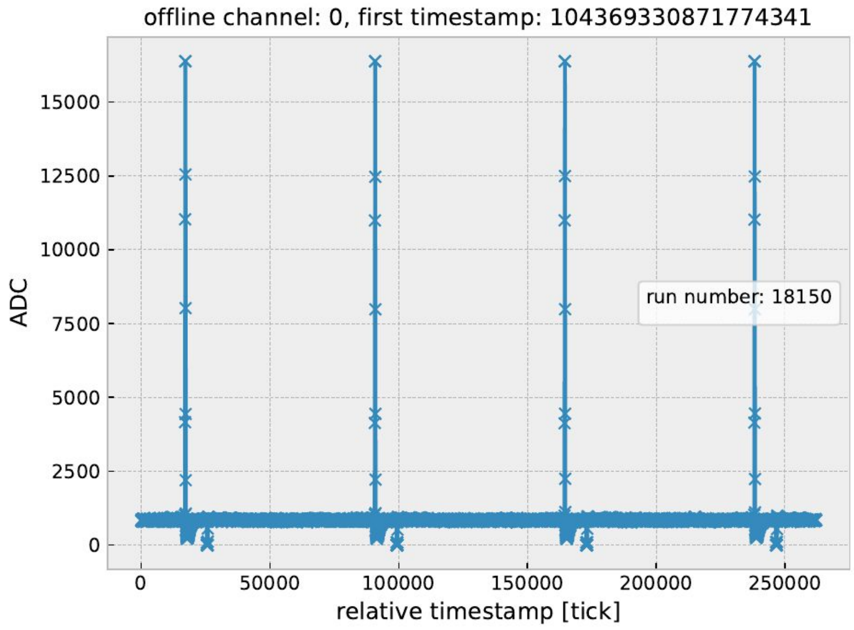
- First time FWTPs were tested and used with the multiplicity trigger.
- Data taking was unstable due to multiple problems when processing the data, resulting in the readout application crashing or firmware TPG stopping at random.
    - Initiated a review of the firmware and software to identify potential causes.
- No validation tools existed at the time, so data from successful runs could not be studied in detail
    - Development of validation software commenced



Cosmic ray track triggered on induction plane firmware TPs

Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0)

- Tests were done primarily with APAs outside the coldbox
- Initially tried to validate and test the system with noise data from the electronics, but this proved difficult, as this didn't provide a constant flux of TPs for which the performance of the readout could be easily predicted.
    - Re-discovered the pulse generator for the APAs which allowed for ideal testing conditions (constant TP flux, obvious and identical pulse shapes).



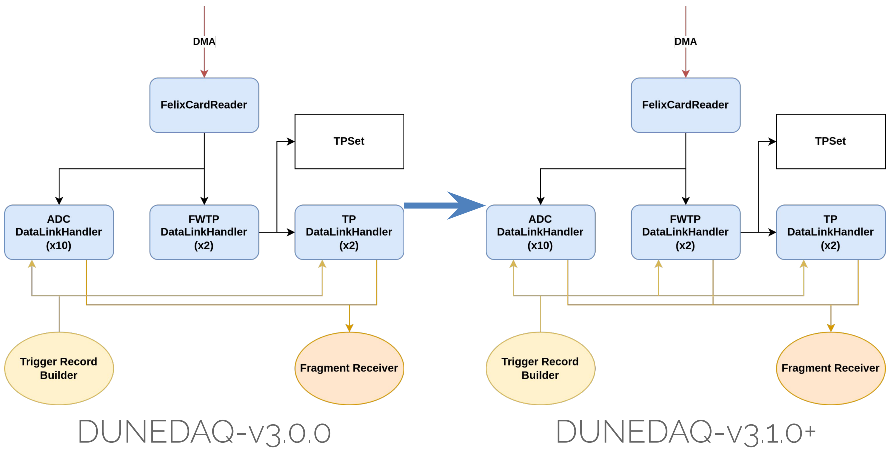
Calibration pulse shape on a single channel

Problems found and addressed

Problems	Solutions
The old ProtoDUNE (Warm Interface Board) WIB was replaced with the new DUNE WIB	Updates to the firmware and software to support the new DUNE WIB data format were needed before any testing could be done
Other changes to firmware improved stability of TPG pod to lower the chance of TP generation halting	More efficient data streaming through the TPG pod, adding large readout buffers before the DMA etc.
The readout application software did not consider the fact the ADC data stream and TP data streams were inherently different, which caused instabilities in the software and missing data	• DLH configuration for the TPs were changed to handle the fact TPs did not arrive in time order • TPs in the buffer were indexed using both time and wire rather than just time, since multiple TPs in a buffer could have the same timestamp

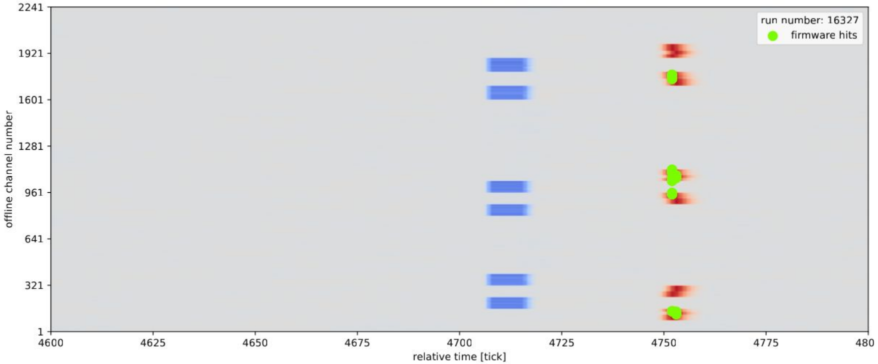
Readout application changes

- Initial attempts at data validation used binary dumps from the DLH's rather than triggered data.
  - This made matching ADC pulses to FWTPs difficult as the time window for ADC and FWTP binary dumps were difficult to align
  - Solution was to write FWTPs to trigger records by having dataflow send readout requests to the FWTP DLH

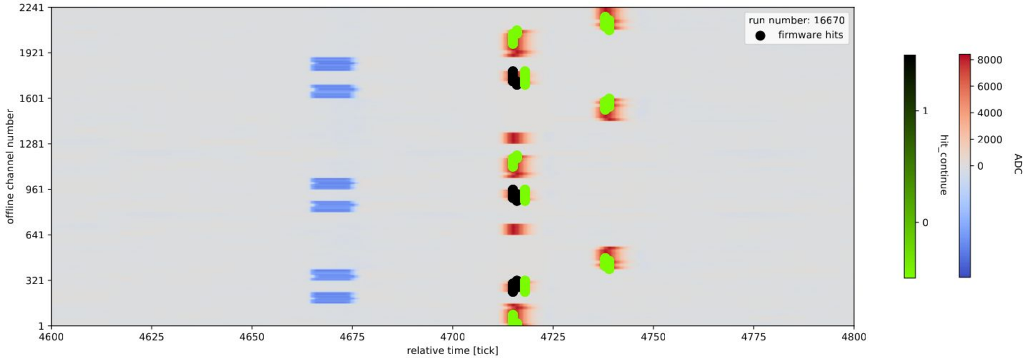


Validation

- Read data from trigger records and unpack the data into pandas data frames for easy analysis/plotting
- Plot single TPs and the pulses which generated them *(see backup slides for examples)*
- Plot global properties of TPs *(see backup slides for examples)*
- Plot 2D event displays and overlay trigger primitives
    - Useful as these event displays highlighted missing TPs in Trigger records, which prompted the fixes in software



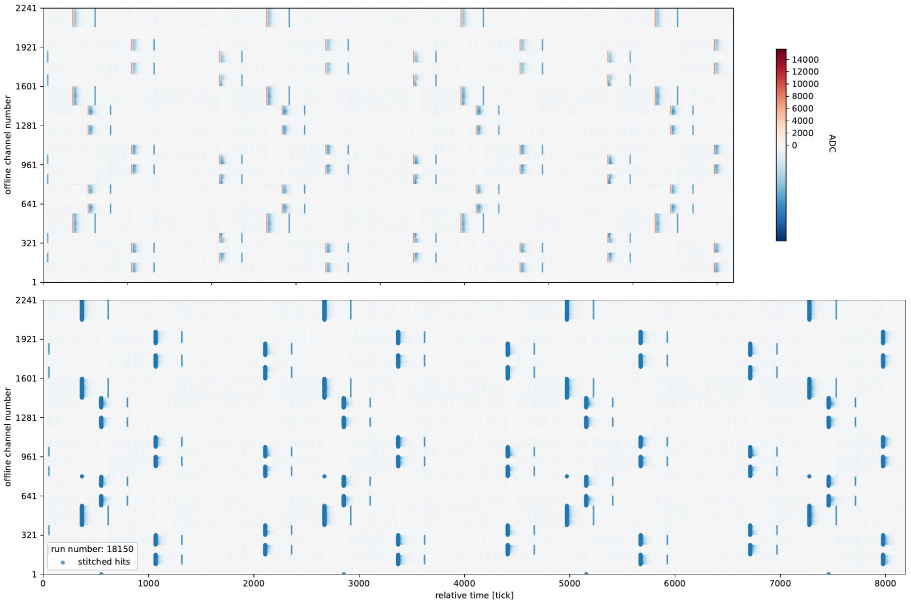
Before the software fixes



After the software fixes

DUNEDAQ integration week (dunedaq-v3.2.x)

- Minor bugs in the software were being debugged, but was stable overall.
    - Quality of life improvements like optical link alignment checks were made and additions to monitoring on grafana were made
- Firmware was still unstable due to backpressure blocking the processing stream
    - Restructured the TPG pod to effectively double the bandwidth of the data stream to the central router from 16b to 32b and allowed better control of data streaming to the DMA
    - Stability improved but was still not fully fixed



Event displays show TPs on each positive pulse

Summary

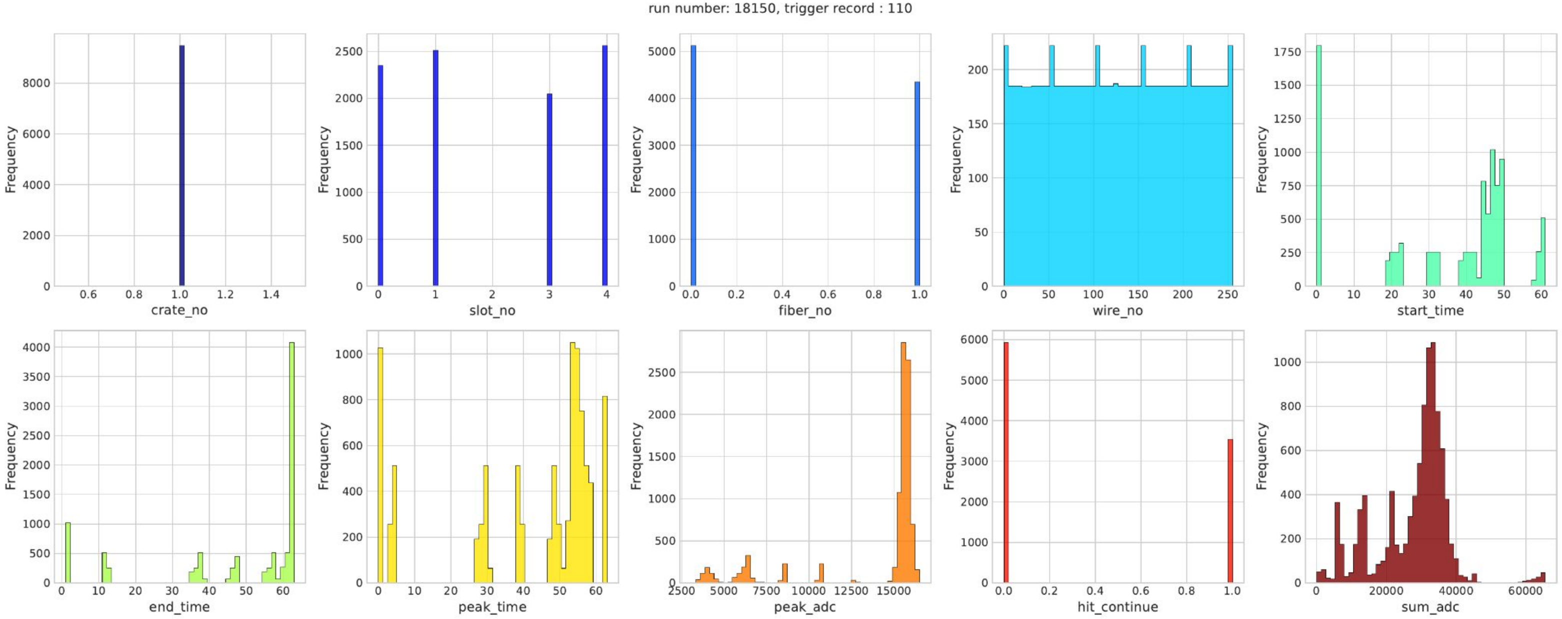
- Readout commissioning was mostly successful in 2022, increasing the readout firmware and software development rate massively.
- Major issues in firmware and software were identified and many lessons were learnt over the year
- readout validation was finally established and provided useful insight into the performance of FWTP generation.
- The state of software is mostly stable and optimizations are still being worked on.
- Firmware has been more stable than before, but there are still cases where TP generation stops, and long term stability has not really been tested yet.
- More work to be done in preparation of the VD coldbox commissioning this month.

Backup Slides

Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0): Validation

Feature list includes:

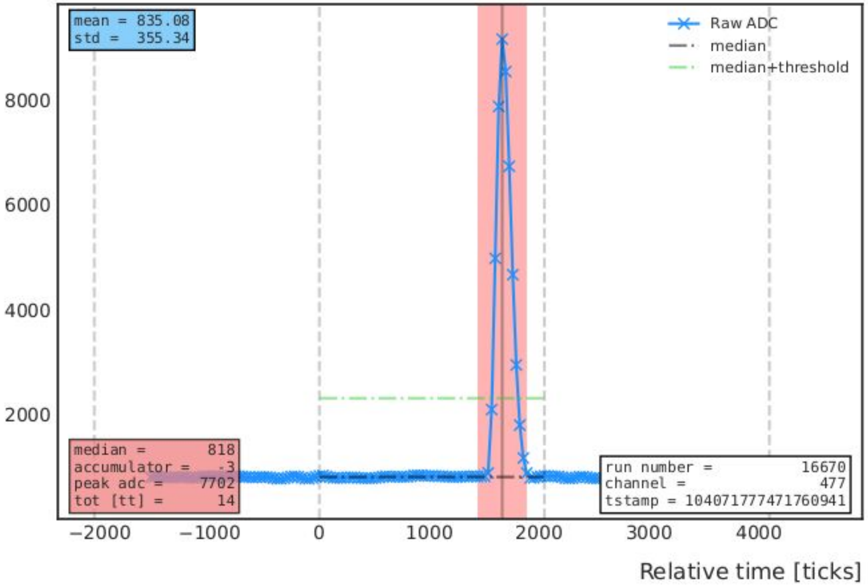
- 1d plots of FWTP properties



Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0): Validation

Feature list includes:

- Waveforms of hits overlaid with trigger primitives, for various pathological cases

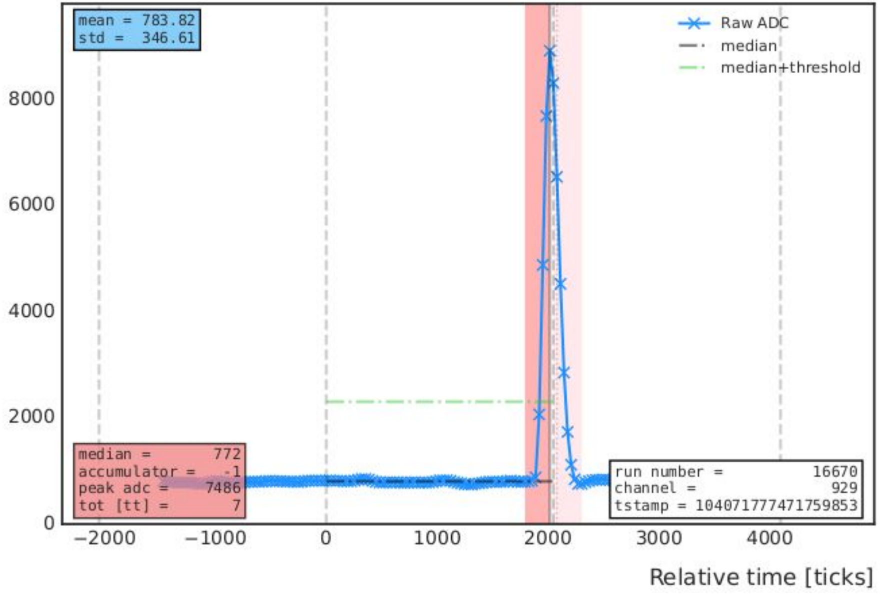


	309
ts	0
offline_ch	477
crate_no	0
slot_no	4
fiber_no	0
wire_no	130
flags	0
median	818
accumulator	-3
start_time	45
end_time	59
peak_time	52
peak_adc	7702
hit_continue	0
tp_flags	0
sum_adc	13377

Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0): Validation

Feature list includes:

- Waveforms of hits overlaid with trigger primitives, for various pathological cases



	24	278
ts	0	2048
offline_ch	929	929
crate_no	0	0
slot_no	1	1
fiber_no	1	1
wire_no	49	49
flags	0	0
median	772	771
accumulator	-1	1
start_time	56	0
end_time	63	8
peak_time	63	1
peak_adc	7486	7486
hit_continue	1	0
tp_flags	0	0
sum_adc	41502	49841

VD coldbox Jan 2023

- Changes to consolidate the different hardware layout will be worked on:
  - Update firmware to produce more output streams for the TPs - lower the chance of backpressure due to higher TP rates.
  - FELIX at the Vertical drift coldbox will have 12 ADC links rather than 10, so firmware needs to be updated for this.
  - DAQ configurations generation needs to be updated to account for the above changes.

Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0): Firmware

- Vertical drift used the ProtoDUNE WIB which was replaced with the new DUNE WIB
  - Data reception and unpacking were updated for handling DUNE WIB packets.
  - ADC data in DUNE WIB packets are represented as 14bits (12bits for protoDUNE WIBs), so the bitlength for ADC data needed to be expanded in firmware.
- Other changes to the firmware were made to improve the control sequence of starting the trigger primitive generation, as well as make full use of the bandwidth of the streaming bus.
- Large readout buffers (several kB) added before the DMA to handle the processing back pressure

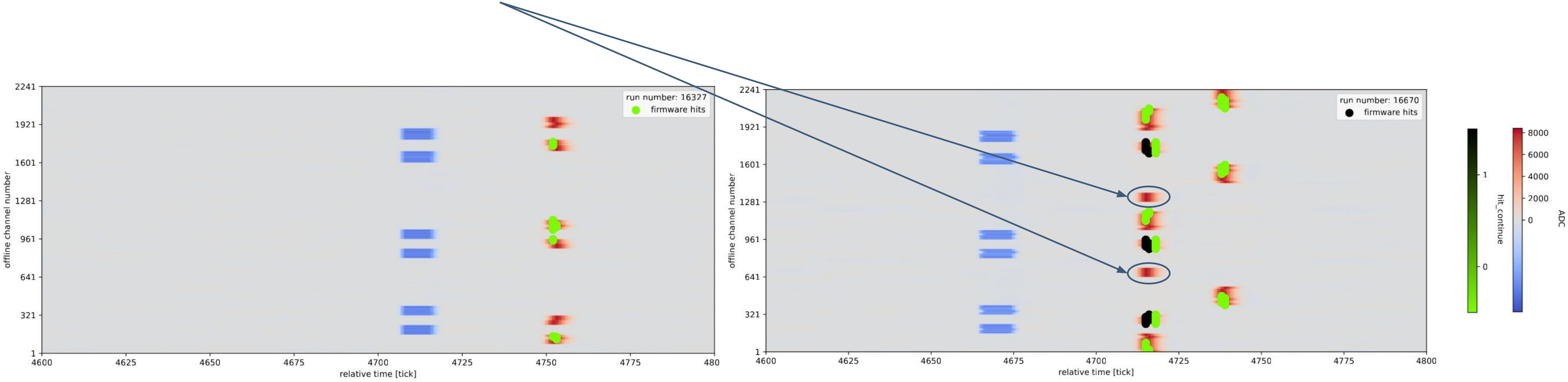
Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0): Software

- Changes to the DLH models were made to account for the fact the ADC data stream is inherently different to the TP data streams.
  - ADC data is a fixed sized data stream ordered in timestamp
  - TP data is a variable size data stream unordered in timestamp
  - Not accounting for these results in missing data, but also makes the system less stable at runtime
- Composite key comparison was implemented to uniquely identify TPs in the latency buffer
  - Packets of TP data can have the same timestamp, so also need to look at geometric information (channel number) to uniquely identify a TP.
- The latency buffer type used for both ADC and TP data assumed time ordered data, but this is not the case for FWTP and TP data
  - Switched to using a skiplist latency buffer model to account for this.

Horizontal Drift integration (dunedaq-v3.1.0/v3.2.0): Software

Event Displays made using the validation tools (more on this next) before and after the changes to the DLHs:

- Some TPs were still missing after the fixes, but this was due backpressure in firmware causing TPs to not be readout for one of the ten ADC links

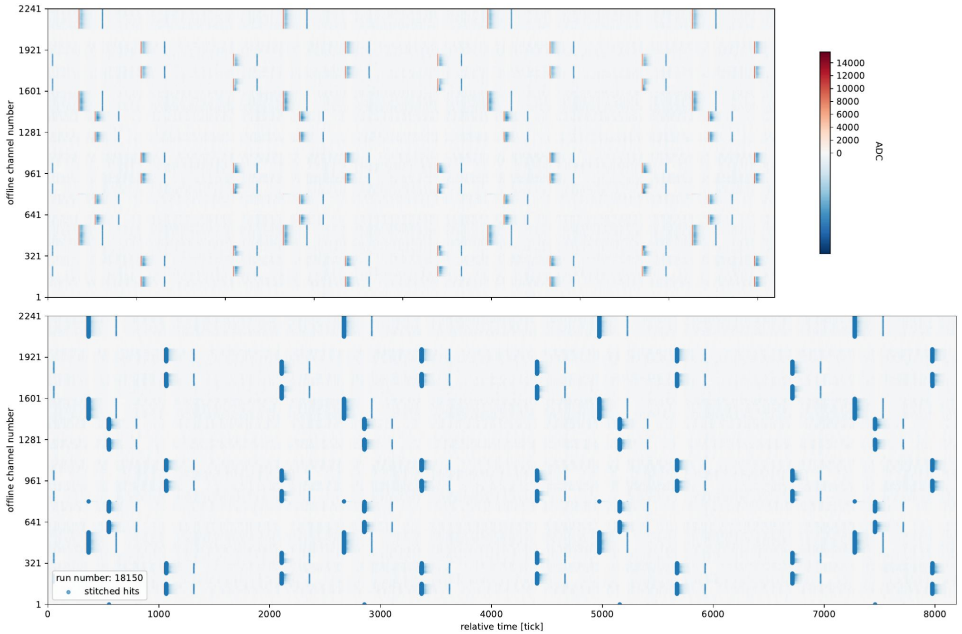


Before the software fixes

After the software fixes

DUNEDAQ integration week (dunedaq-v3.2.x): Firmware

- Reset mechanism was made more reliable for the processing blocks in the TPG pod.
- An outflow block was added before the central router. This controls whether the back-pressure signal is propagated from the central router, this provides a better control of data streamed to the DMA.
- By restructuring the blocks in the TPG pod it was possible to double the bandwidth of the processing chain when send data to the central router.
    - Required changes in software as well.
- Stability of the firmware improved.



Event displays show TPs on each positive pulse

DUNEDAQ integration week (dunedaq-v3.2.x)

Deploying FWTP readout:

- DAQ configurations were provided over the week which contain:
  - DUNEDAQ applications (i.e. readout/dtpcontroller/FelixCardReader)
  - FelixCardController
  - WIB configurations (toggle calibration pulses)
- So as long as you knew the basic instructions for running any DAQ configuration, you could run with firmware TPs configured
- More comprehensive instructions for running and debugging the readout were written which allowed (mostly) autonomous operation of the DAQ system.
  - developers working on trigger were able to run and modify firmware TP configurations for their integration tests
  - People working on data FWTP validation could run and debug the DAQ without a software expert (unless the problem was really bad)