DAPHNE Test at Milano-Bicocca

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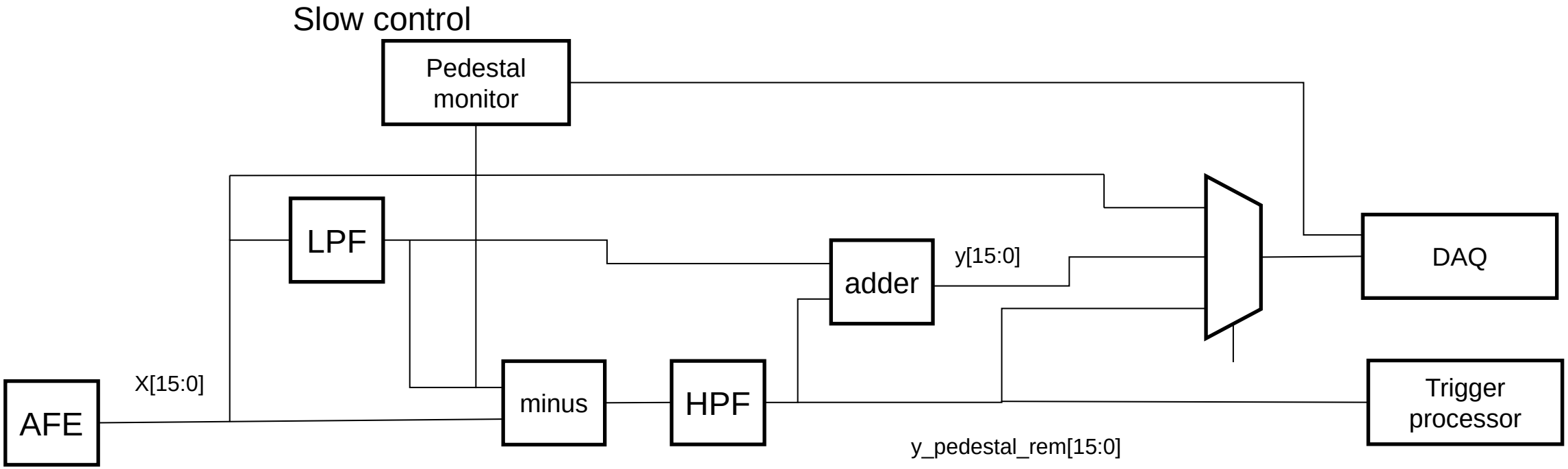
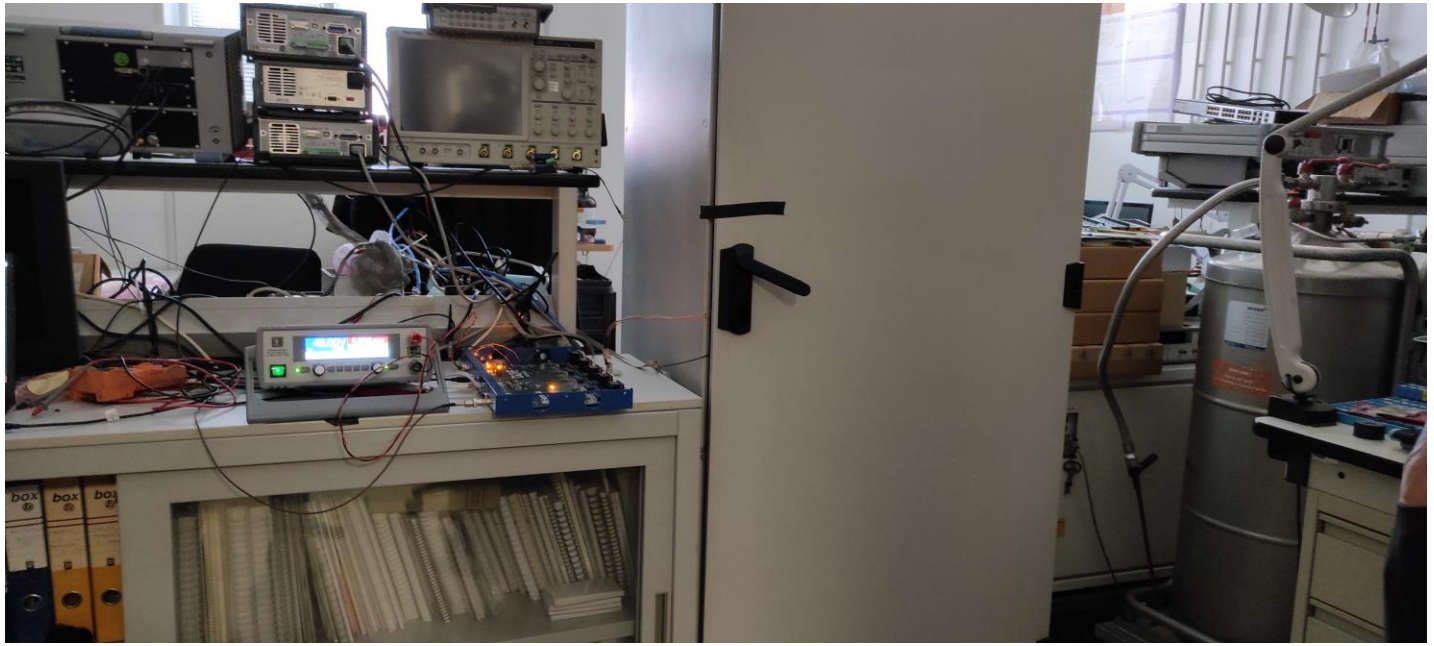
Introduction

- DAPHNE test with a X-ARAPUCA supercell.
  - SNR and Digital filter test.
- Self-trigger module test.

Digital Filtering

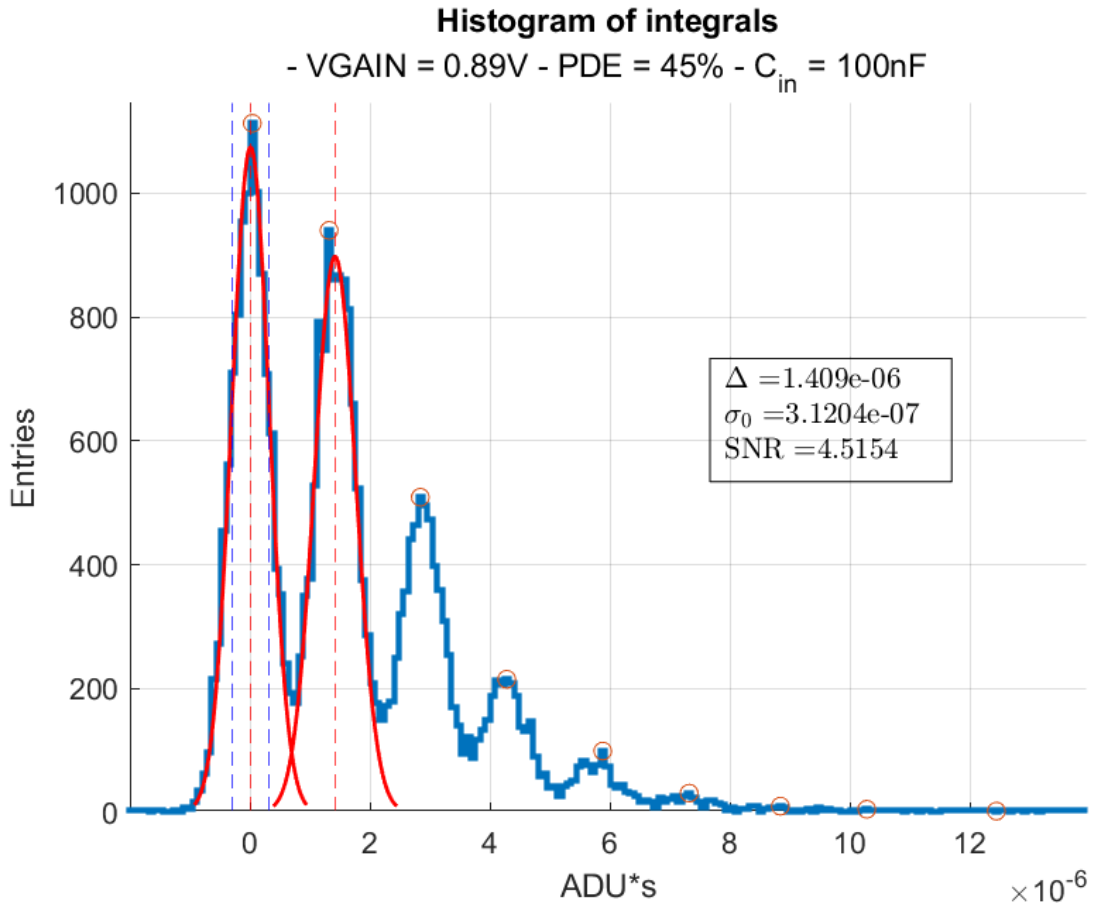


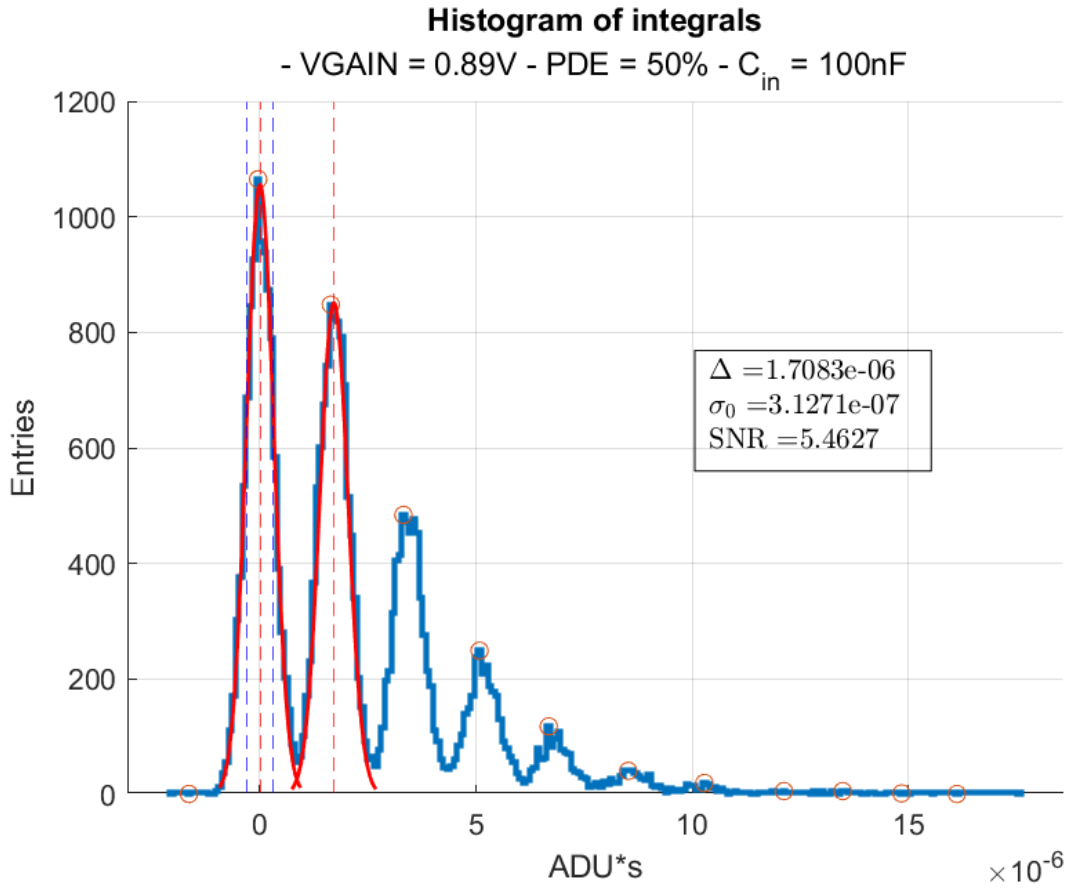
X-ARAPUCA supercell test



X-ARAPUCA supercell test

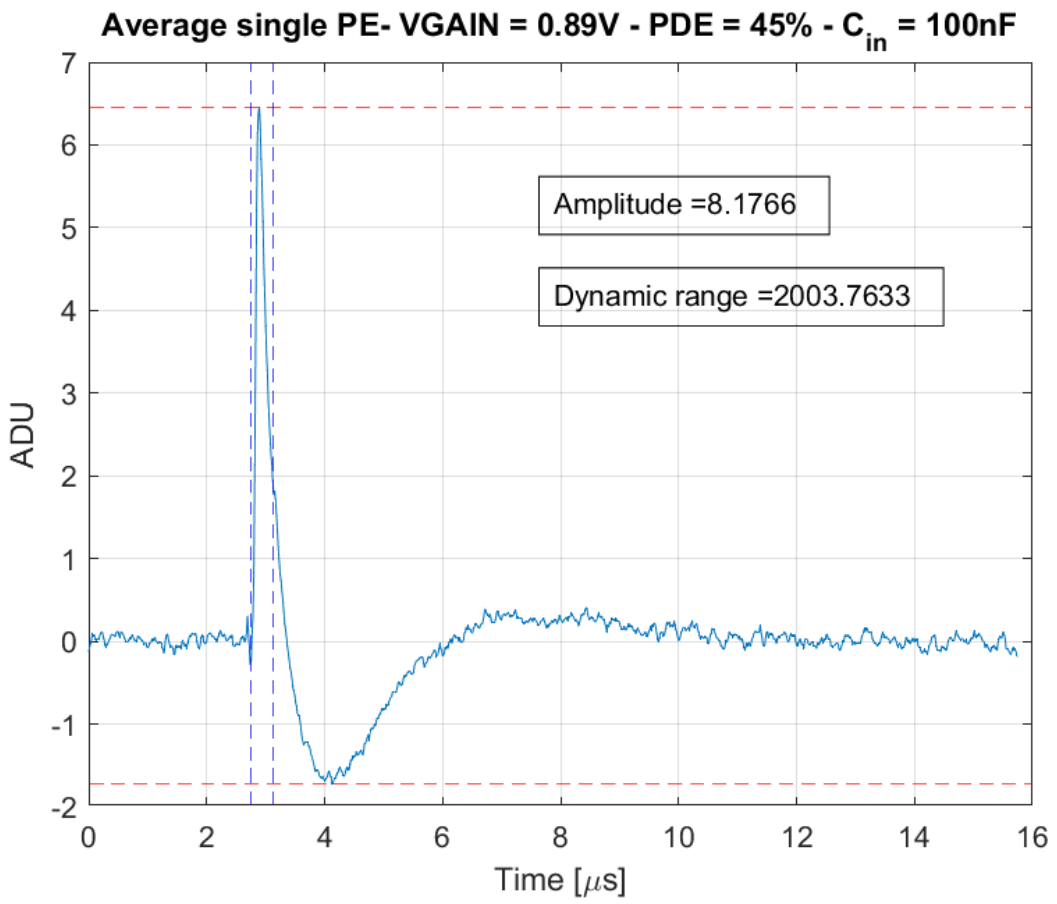
AFE integrators ON

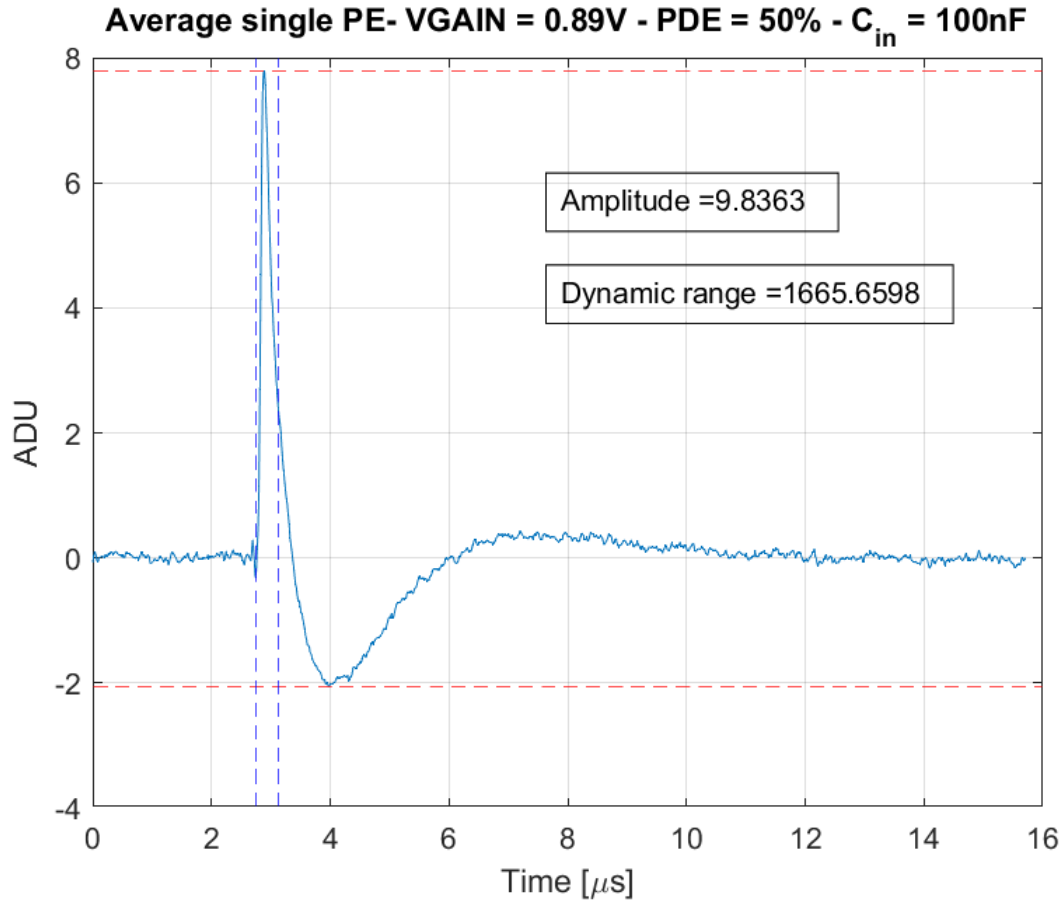




X-ARAPUCA supercell test

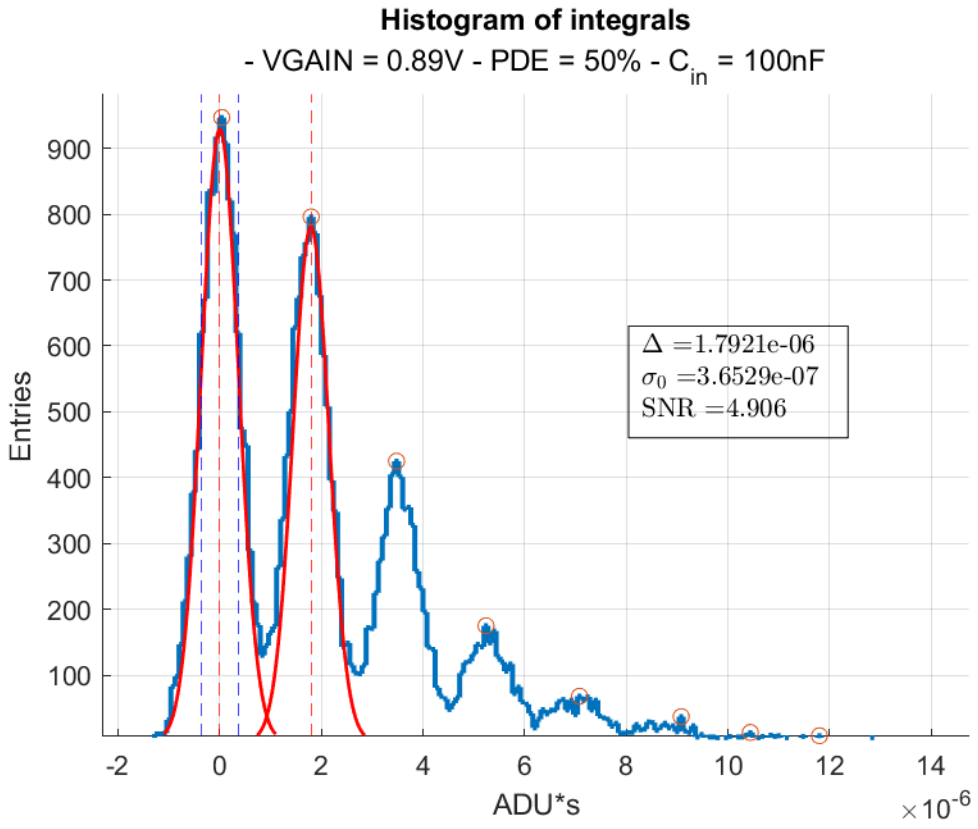
AFE integrators ON



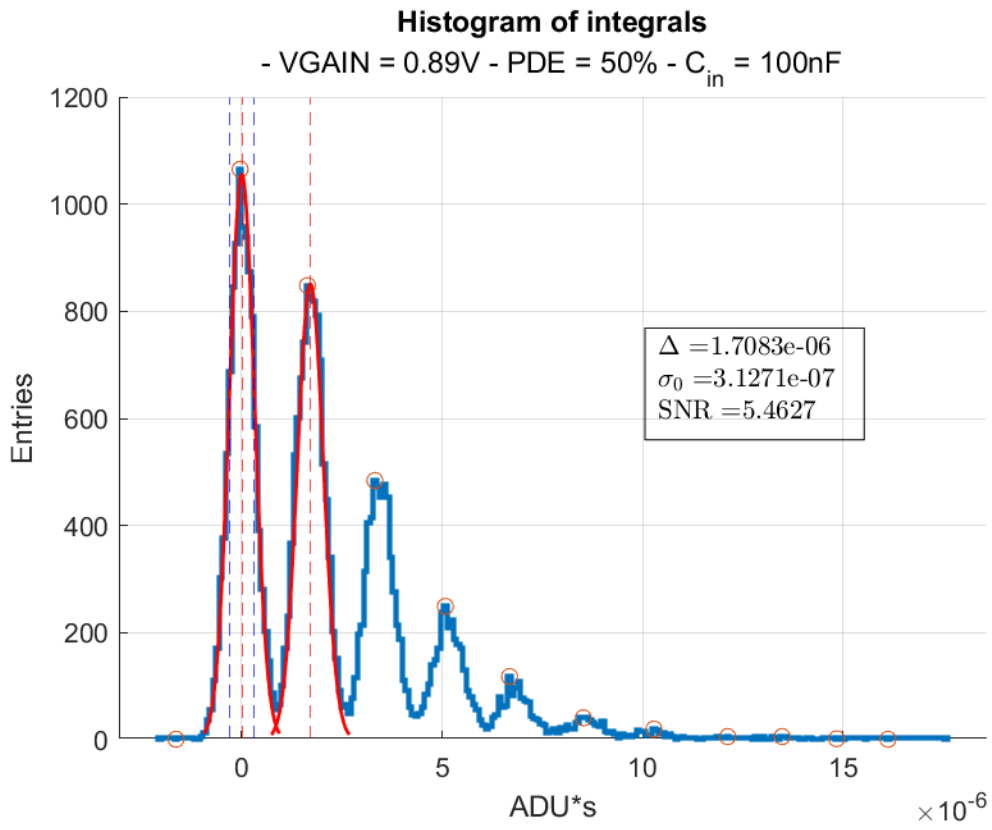


X-ARAPUCA supercell test FPGA filter

AFE integrators OFF FPGA Filtered

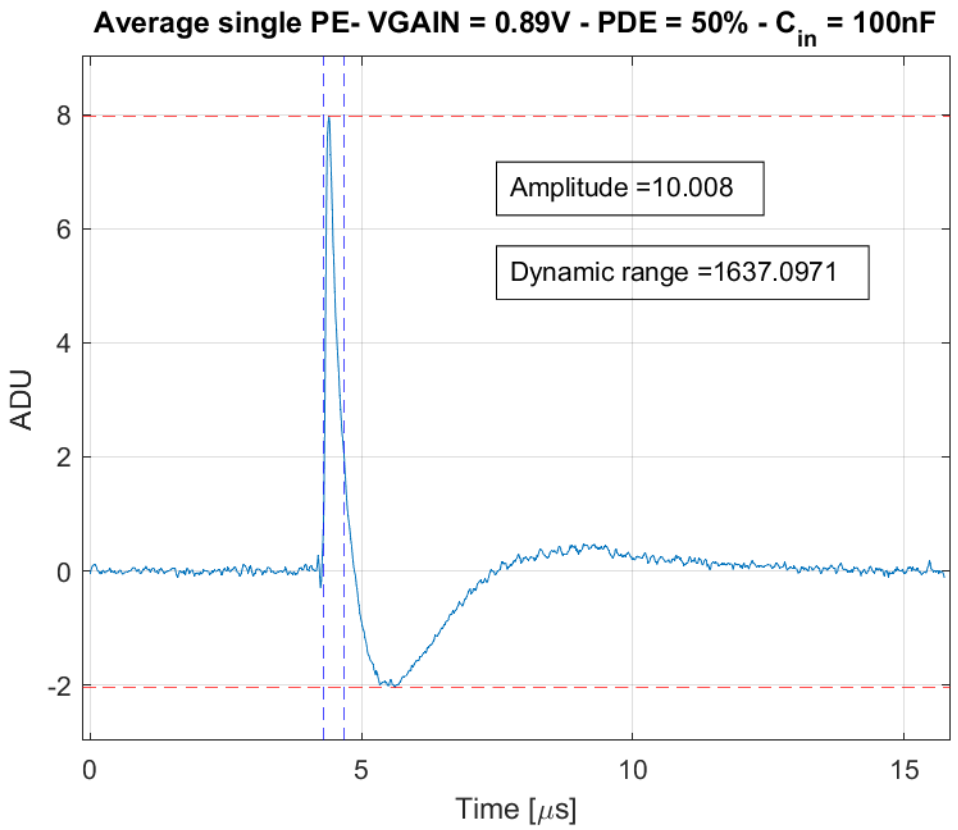


AFE integrators ON

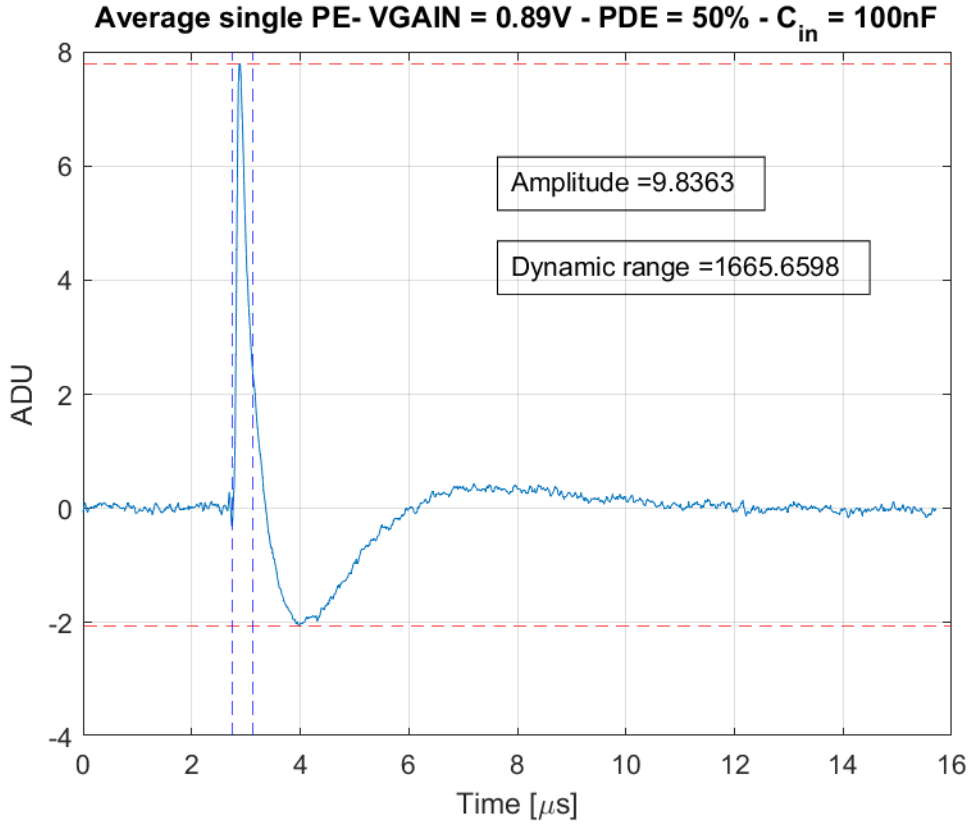


X-ARAPUCA supercell test

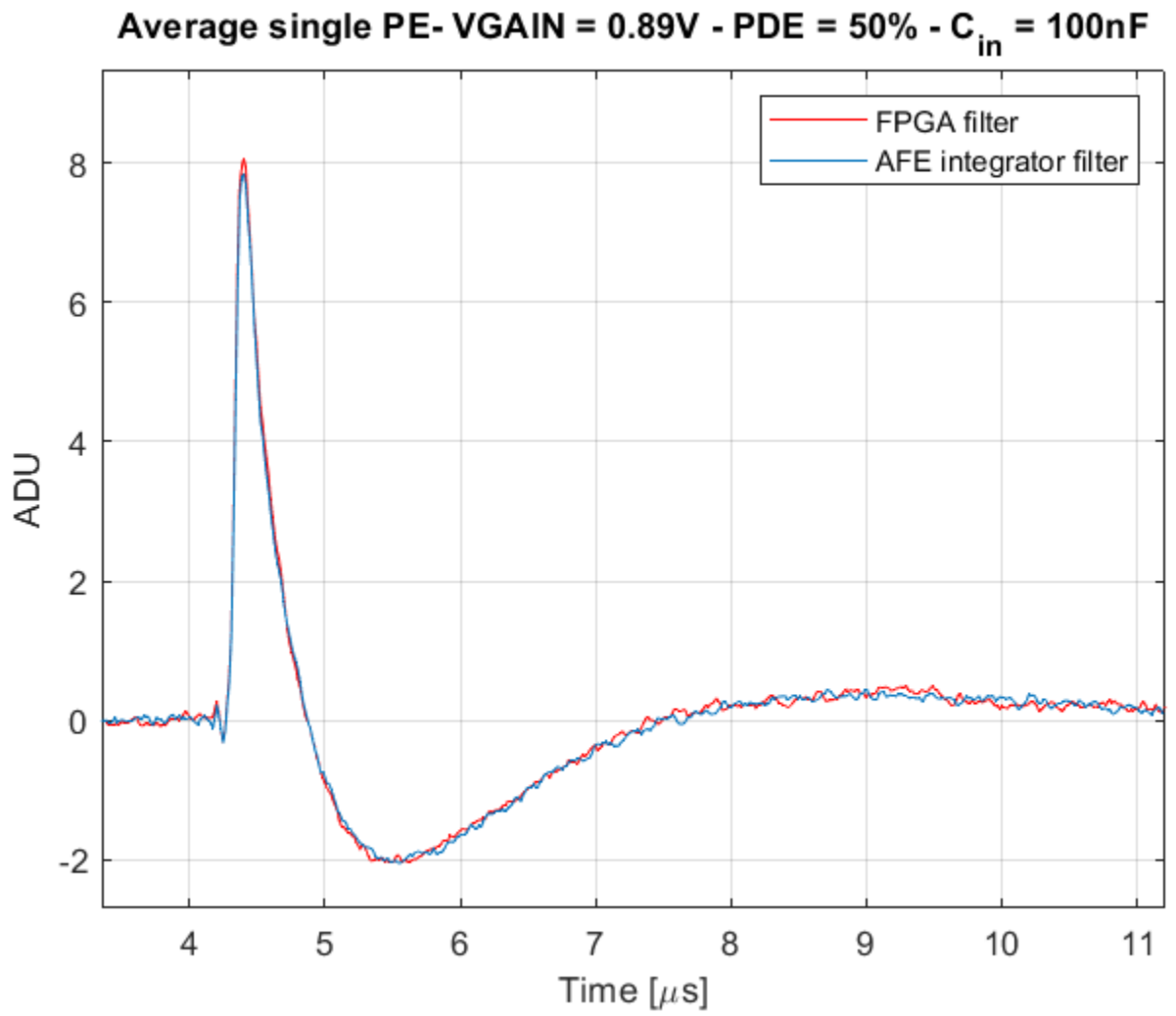
AFE integrators OFF
FPGA Filtered



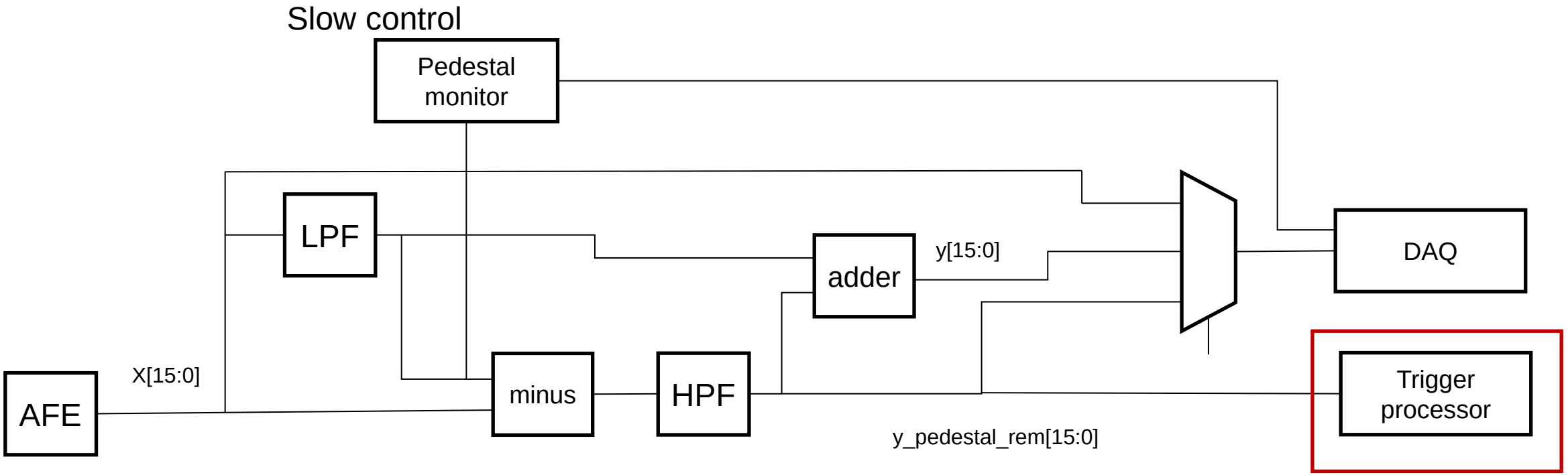
AFE integrators ON



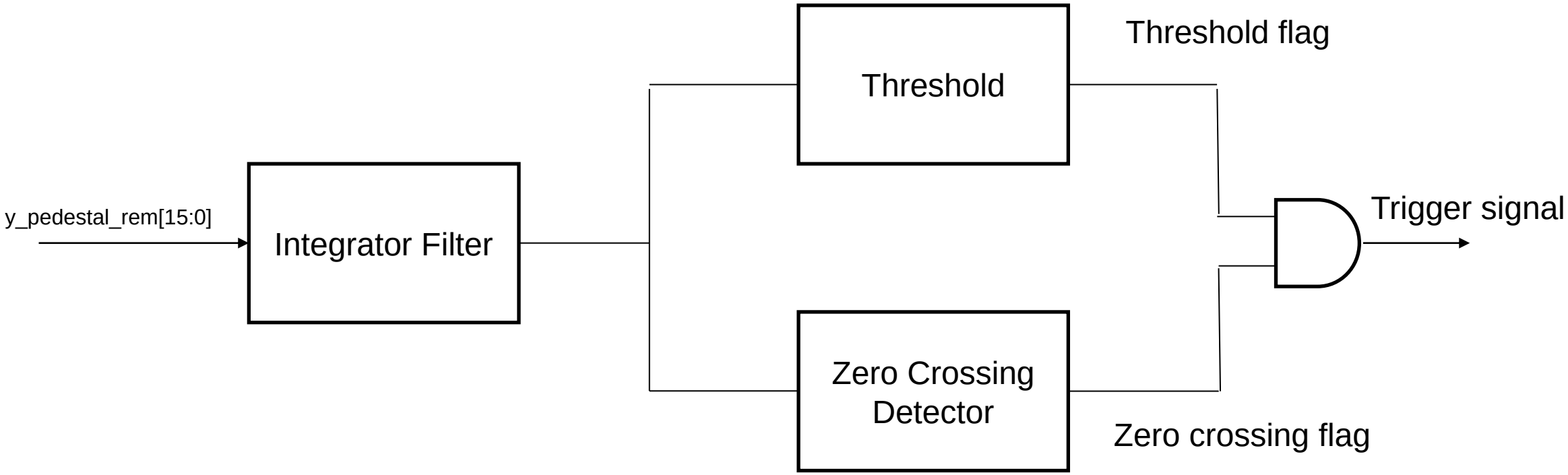
X-ARAPUCA supercell test



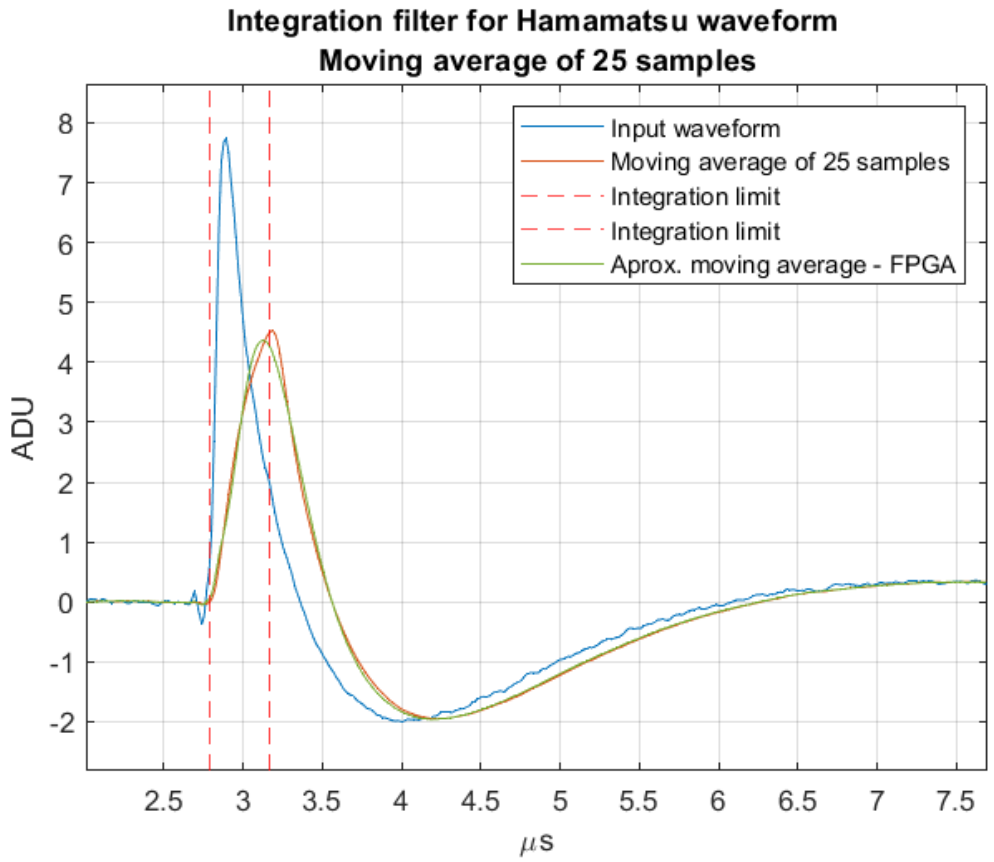
Self-triggering

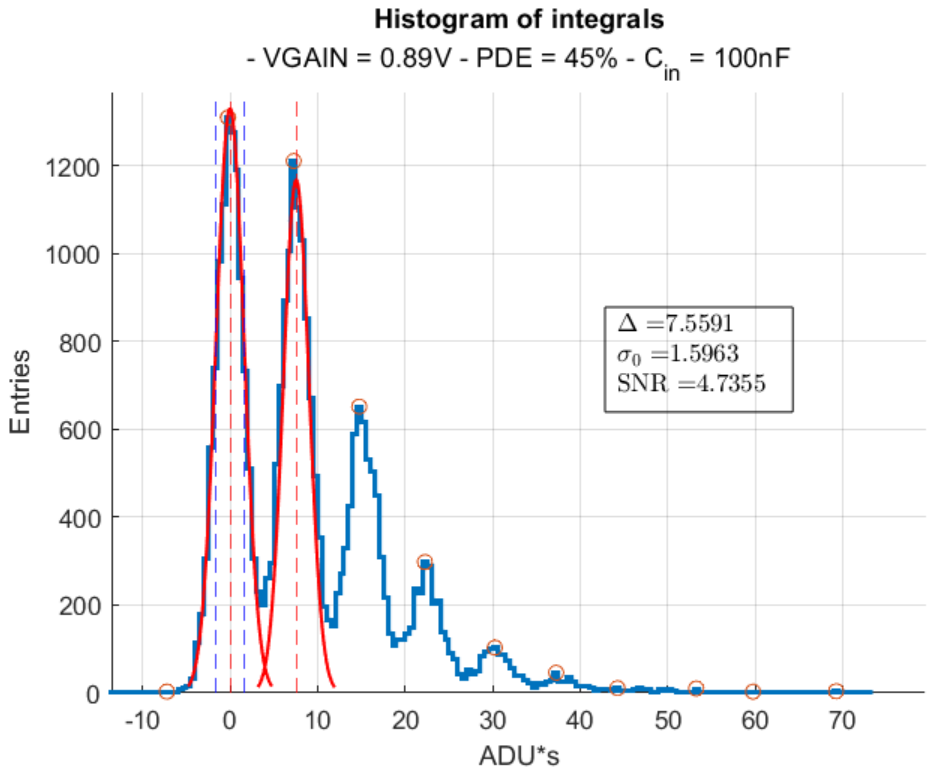


Trigger processor



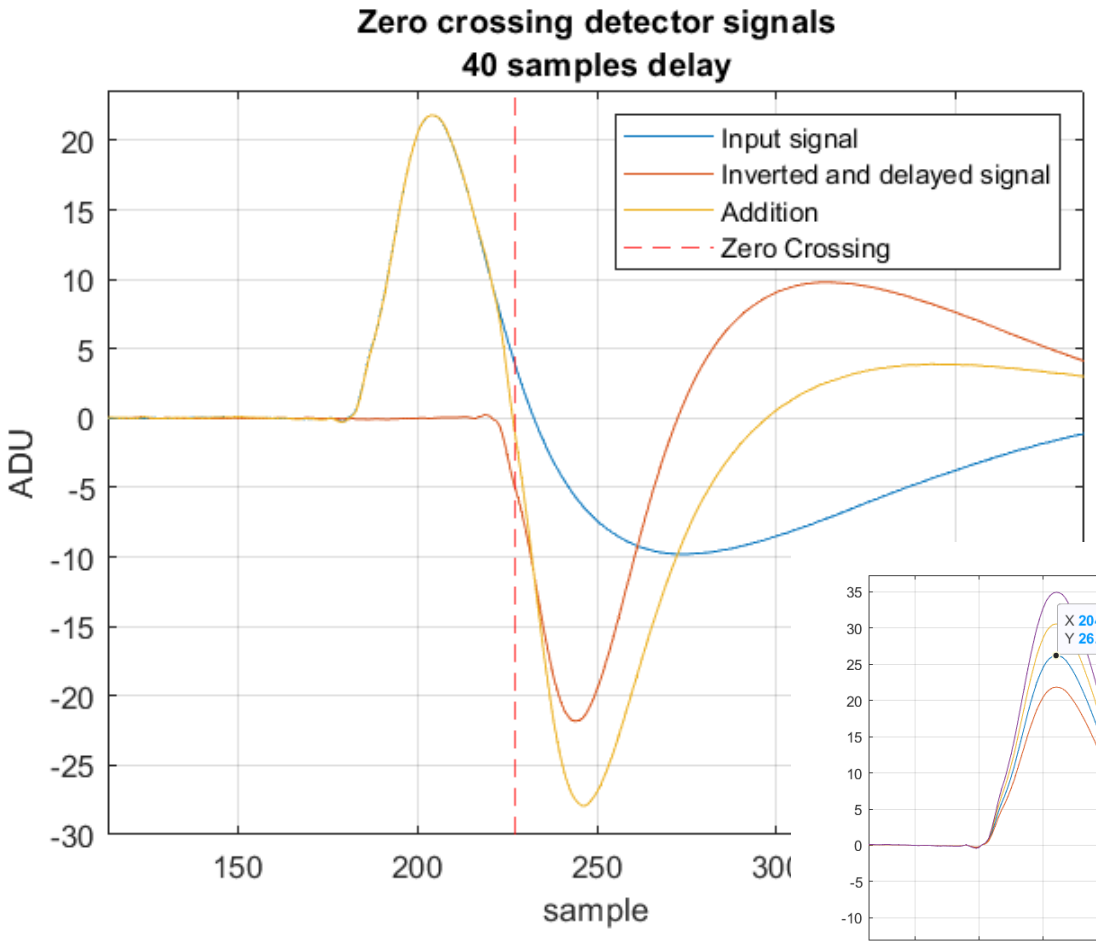
Integrator filter





- Using the same architecture used for the “AFE integrator” filter, we approximated a moving average filter of 25 samples. (For FBK is 40 samples).
- The integration is performed by the filter and is given by the peak value.
- The peak value is extracted, and a histogram can be performed.
- Then, after calibration, we can trigger at any point in the histogram (e.g., 1.5 P.E.) just by setting a threshold in the integrated waveform (green).
- In the FPGA implementation, we multiply by a factor of 2 to reduce the quantization error. (this factor is included in the histogram figure)

Zero-crossing detector

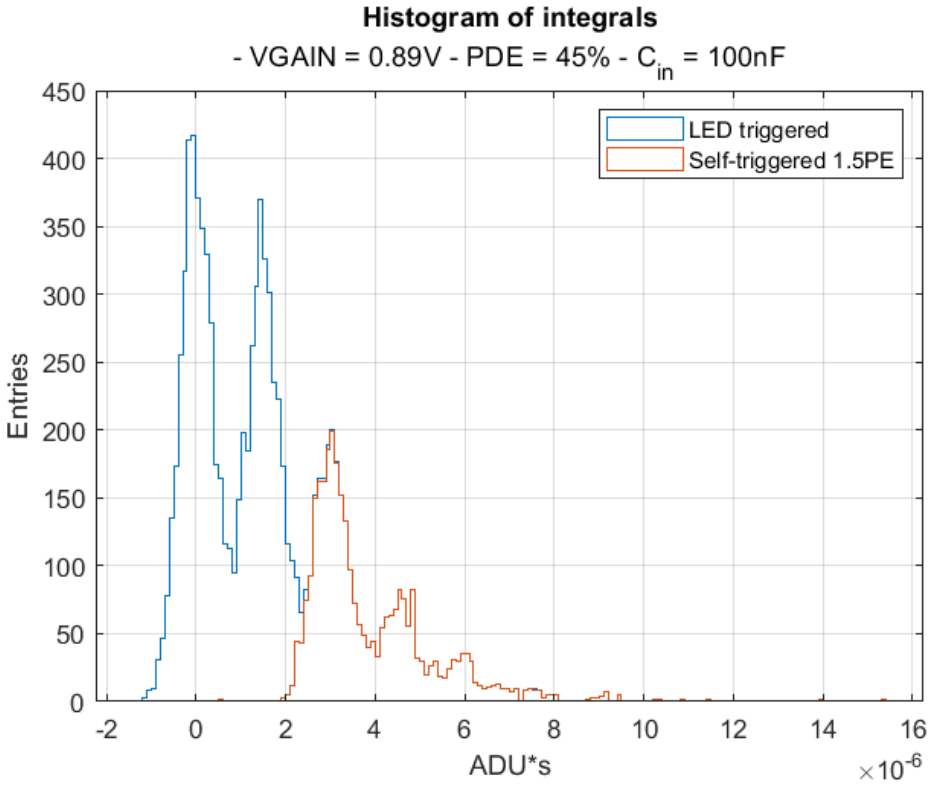


- To avoid the time walk jitter in the threshold flag, we use a zero-crossing detector.
- The input signal is inverted and delayed by a fixed number of samples (40 in this case).
- The input signal and the delayed are summed. The zero crossing is detected, and the flag is asserted.
- The final trigger signal is the logical and of the threshold flag and the zero-crossing flag.

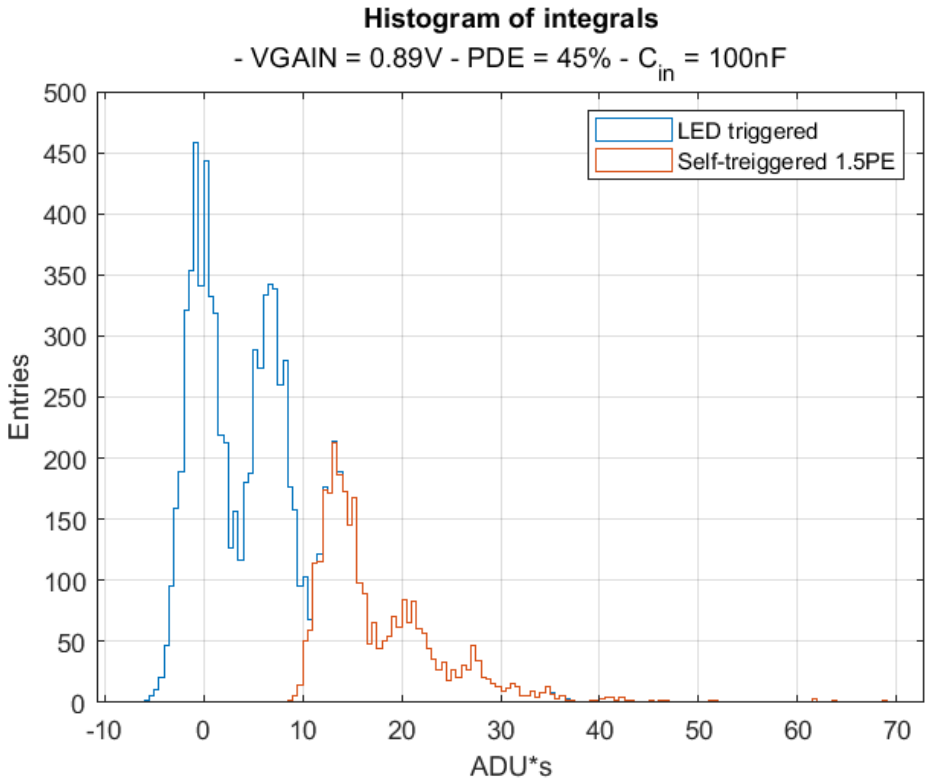
Obs: Given that the signal is bipolar in nature. The zero crossing can be detected without the procedure described above, and just using the input signal. We have found that using the described method improves the jitter in the zero-crossing detection caused by the electronic noise. We will continue to improve the minimization of this jitter effect to try to minimize FPGA resource utilization.

Trigger processor hardware simulation

Integration of waveforms

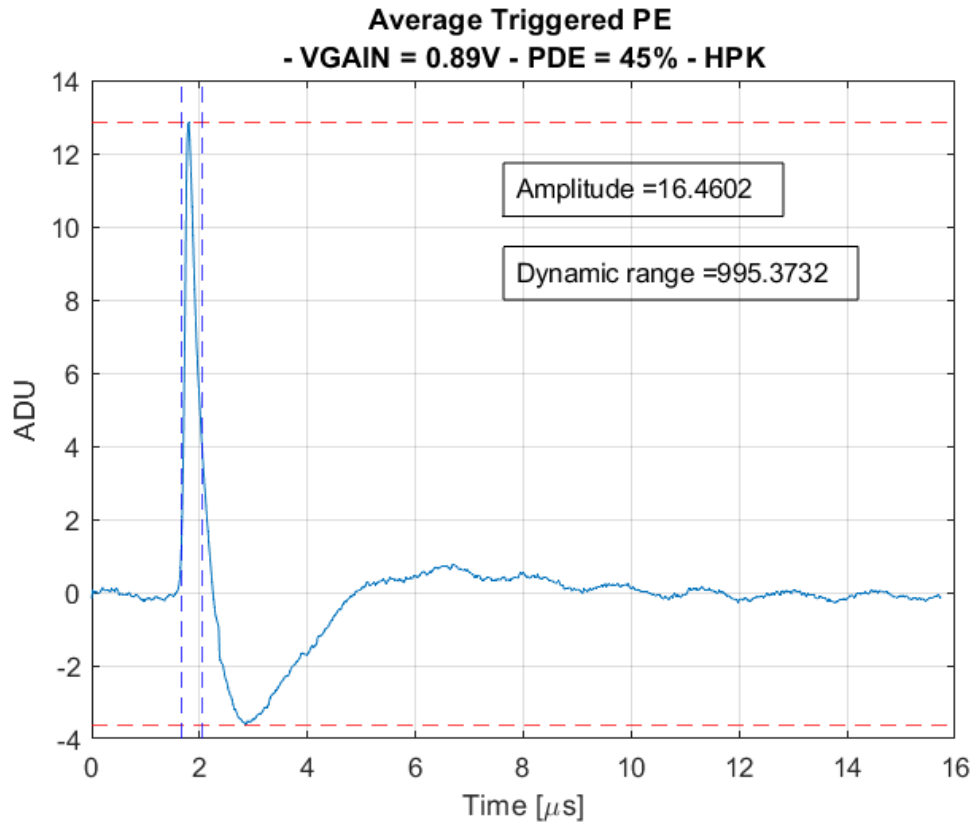


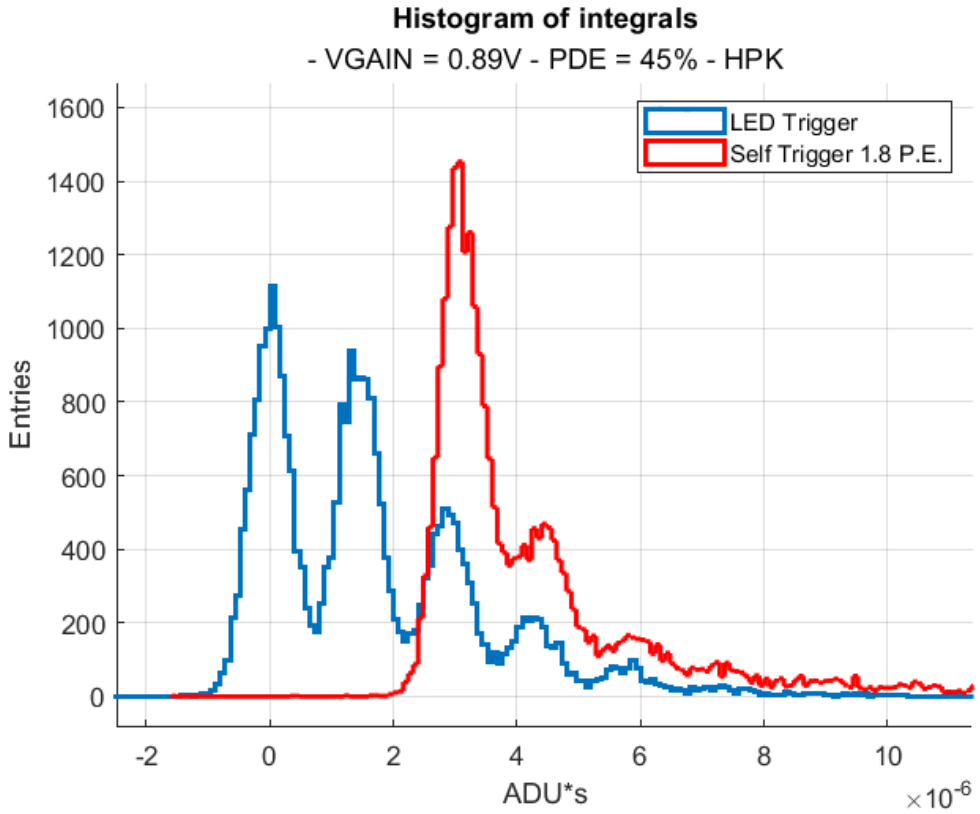
Integration filter peak values



- The simulation of the trigger processor hardware is done using RAW daphne data (i.e. unfiltered data).
- Using the approximated filter, the module is calibrated with a threshold flag of 11. This value correspond to 1.5 PE in the blue histogram in the right.
- The result of the simulation is the red histogram in the left figure, where one can see that the trigger module cuts most of waveforms that have an integral value below the corresponding to 1.5 P.E. set by the threshold

Trigger processor test - Supercell





- Using the supercell setup, we tested the self-triggered module with DAPHNE.
- Due to an error in the setup, we tested the calibration for Vov = 3V with Vov=2.5. The original 1.5PE becomes ~2PE.
- The trigger result are good, the main issue is the trigger jitter. The best results we obtained is a jitter of around 12 samples.