PIP-II Low Level RF Beam Pattern Generator (BPG)

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CONTENTS

SCOPE

The Beam Pattern Generator (BPG) is the controller for beam delivery and RF synchronization to downstream target machines and future experiments as well as the source for precise timing reference for the Linac. Primary responsibilities of the BPG system are to generate the beam pattern as requested by experiment and to derive the Booster injection pattern, drive Medium Energy Beam Transfer(MEBT) Fast Kickers and to correct system errors in that system, has the capability to drive the Low Energy Beam Transfer(LEBT) Chopper, provide the injection RF signal which the Booster will lock too as well as synchronize pulses for the Booster to generate the Booster revolution marker. The BPG also generates an output trigger, precisely aligned with the 162.5 MHz RF clock. The scope of this document is to describe the architecture and the technical requirements of the BPG system.

ACRONYMS, TERMS, AND DEFINITIONS

BPG	Beam Pattern Generator
CSV	Comma Separated Variable
EPICS	Experimental Physics and Industrial Control System
GUI	Graphical User Interface
IOC	Input-Output Controller
LEBT	Low Energy Beam Transfer
MEBT	Medium Energy Beam Transfer
L2	WBS Level 2
L3	WBS Level 3
PIP-II	Proton Improvement Plan II Project
PV	Process Variable
USB	Universal Standard Bus

REFERENCED DOCUMENTS

[1] PIP-II 800 MeV Proton Linac Beam Pattern Generator, IPAC 2021

[2] PIP-II Document 5349-v1, Beam Pattern Generator Overview

[3] PIP-II Final Design Report Accelerator Systems, Section 1.6.7 Beam Pattern Generator

[4] Injection Paper---- Physics document

[5] LLRF FRS

[6] Booster PIP-II Integration Block Diagram, Ed Cullerton

SYSTEM DEFINITION

Background

The Beam Pattern Generator is the system that synchronizes the beam injection and the RF systems between the PIP-II LINAC to the Booster. The RF frequencies of these two accelerator systems are not harmonically related. Synchronization is accomplished by controlling two MEBT beam choppers, which select 162.5MHz beam bunches from the LEBT and RFQ to produce an appropriate reduced beam bunch pattern that enables bucket-to-bucket transfer to the Booster RF at 46.46MHz (84th Revolution Harmonic). This chopping pattern also reduces the beam current to an average of 2mA over the Booster injection, matching the Linac nominal beam current. The BPG also generates the RF frequency/ phase reference which the Booster will phase lock to during injection. The BPG is fully programmable, allowing for arbitrary beam patterns with adjustable timing parameters, having a fine adjustment resolution of ~38ps. The latter is accomplished using digital signal processing techniques.

System Diagram

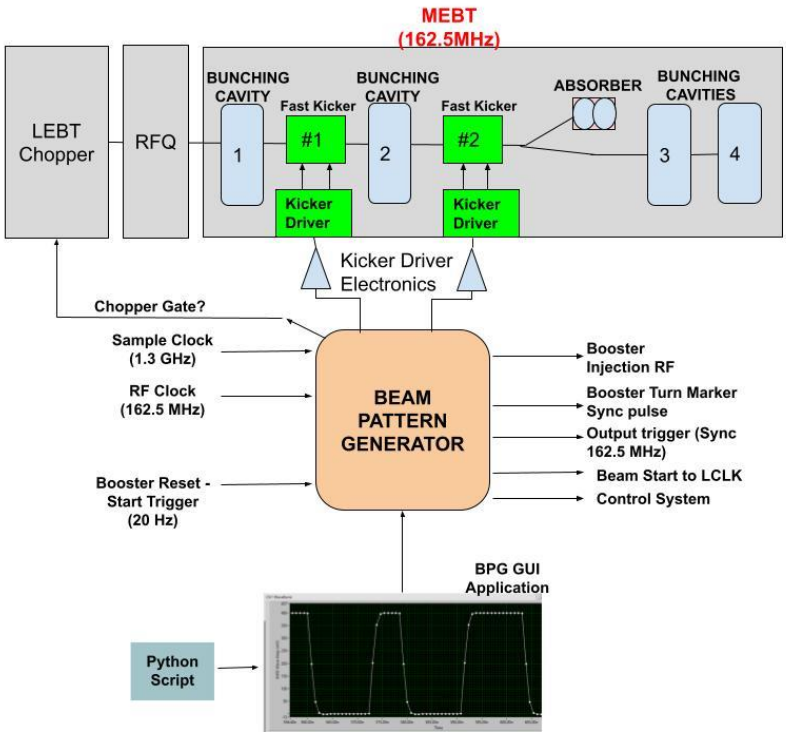

Figure 0.1: BPG System Diagram

The BPG and MEBT fast kicker are designed to produce a beam pattern at the output of the MEBT in any requested sequence of 162.5 MHz bunches over some time-period that is repeated at the 20 Hz machine repetition rate. This arbitrary pattern could thus contain information that span the frequency range from 20 Hz to 81.25 MHz and must maintain an extremely flat amplitude and phase response. The two Fast Kickers are constructed with a pair of spiral coils designed to match signal propagation with the 2.1 MeV beam velocity and give a transverse electrostatic kick to the beam bunch when it is to be directed into a beam absorber and not propagate down the accelerator.

The new Booster injection is more complicated because of the longer injection period, 20 Hz machine operation and requirement of synchronized beam transfers between machines. The 162.5 MHz fundamental RF and the Booster are not harmonically related which requires a beam pattern over the 550 micro seconds injection period with the exact pattern derived from intersection of 162.5 MHz bunches from the RFQ and a set acceptance angle of the Booster RF buckets at the injection energy. Two of the 82 Booster buckets will have no beam injected into them to provide a kicker gap to reduce beam loss. For the injection scheme to work the BPG must also provide an RF signal with the proper frequency and phase angle for the Booster RF to lock to during the injection period. It must also provide a revolution marker to identify the position of the gap buckets [1].

As shown in fig 4.1, Presently a Python script generates binary pattern CSV file with 1s representing “kick” and 0s representing “pass”. Each element represents a period of 1/162.5 MHz or 6.15 ns. This pattern is applied to the LabVIEW/ EPICS GUI application, which communicates with BPG chassis using Ethernet or USB interface and the BPG system generates waveform per CSV file. Key features of this application are adjustable channel delays, rising edge delay, falling edge advance, and phase flip. Both channel delays can be adjusted independently and have ~38ps of time resolution for each value of rising/ falling edge adjustment. For the final design all these software features will be integrated into an the BPG FPGA firmware and the BPG EPICS IOC.

Digital Signal Processing

There are many fine timing resolution and precision requirements for the output waveforms and sampling theory tells us that these requirements can be met with the relatively low clock rate of 1.3 GSPS. This sample rate allows the generation of a 650 MHz bandwidth signal with exact timing and amplitude within the limits of bandwidth and the resolution of the DACs.

As shown in fig. 4.2 functional diagram, RF clock for the BPG system is 162.5 MHz making the Nyquist bandwidth of the beam pattern 81.25 MHz. For a time resolution of <50 pico seconds, signal is oversampled at 26 GHz resulting the Nyquist bandwidth of 13 GHz and a timing

resolution ~38 pico seconds (1/26 GHz). To get a timing resolution of ~38 pico seconds, all signal processing is done at a virtual rate of 26 GSPS which allows the desired resolution [2].

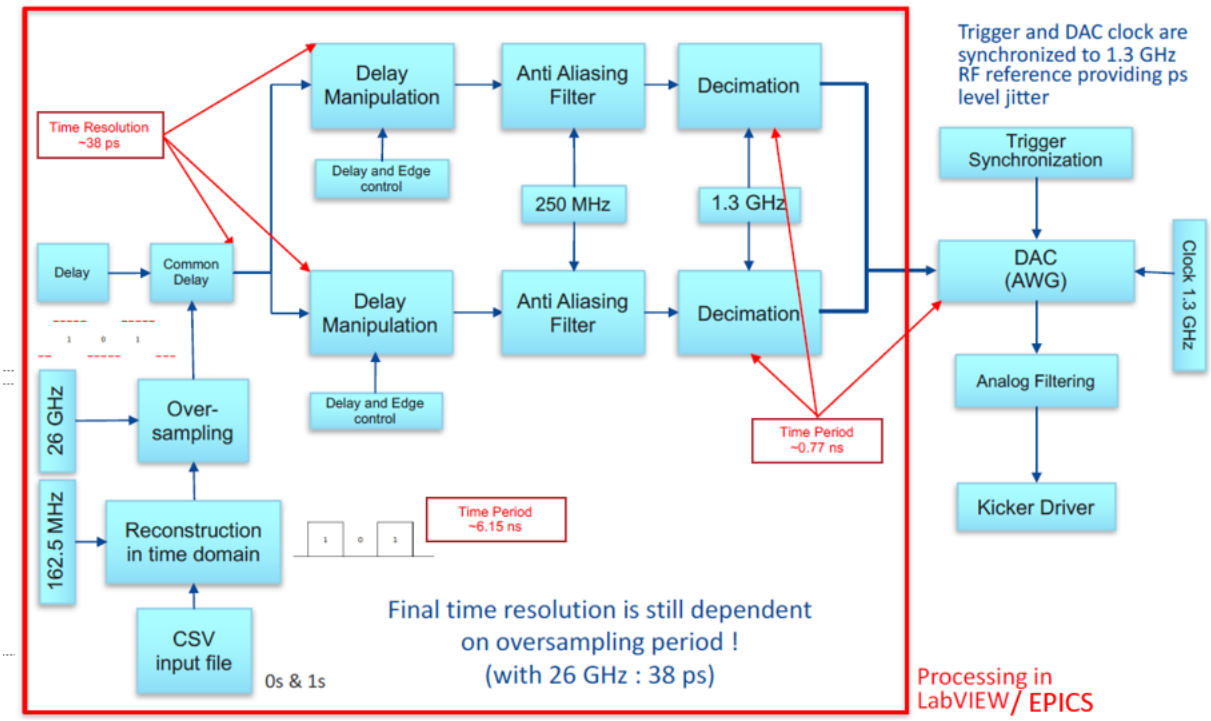

Figure 4.2: Functional Diagram

Final signals are digitally filtered to below the 650 MHz Nyquist frequency, then down sampled to 1.3 GSPS. The AWG is running at 1.3 GHz clock. The output of the calculated waveform channels must be less than the Nyquist bandwidth of 650 MHz. These signal arrays are loaded into AWG waveform memory and the output of the DACs are run through an analog reconstruction filter. As shown in functional diagram, 250 MHz anti-aliasing filter is used to eliminate higher frequencies. An analog anti-aliasing filter reconstructs the waveform while limiting the bandwidth to 350 MHz. While bandwidth limited, the resolution of ~38 pico seconds and amplitude information is faithfully preserved in the analog signal output.

Synchronization

Synchronization of RF signals, BPG outputs including the base clock and triggers to the Linac timing system are critical to machine operations and to understanding how the required precision is achieved for other functions of BPG. An external trigger from any external source, e.g. a non-RF based clock system, used as input in a synchronizing circuit will create an output trigger that is precisely aligned with the 162.5 MHz and the 1300 MHz RF. Sub 1300 MHz period alignment is done so that the trigger maintains the setup and hold time requirements of the AWG input circuit. The AWG has output triggers that can now go back to the distributed clock system and any other system that needs precision timing. With this synchronization system the outputs of the

AWG channel are stable with respect to the RF and all other AWG channels to the level of the jitter specs of the AWG which is on the order of pico-seconds [2].

Injection and Capture

The present 400 MeV injects beam for approximately 40 microseconds into zero RF volts in the Booster where it decoherers and coasts until it is adiabatically captured with 800kV RF. The beam momentum is defined by the Linac and the beam radial position is a function of this momentum and the B-field in the machine according to the equation:

$$-\frac{dR}{R} = \frac{1}{\gamma t^2} * \frac{dB}{B} \text{ or } \frac{dR}{R} = 0.0337 * \frac{dB}{B}$$

Where R = Beam radial position,

B = Magnetic field,

γ_t = Beam momentum at transition energy for the Booster

The PIP-II era injection has many fundamental differences from present operations that must be understood in both the details of implementation but also in the ramifications that will affect day to operations and tune-up. The big changes are going from 400 MeV to 800 MeV kinetic and the switch to bucket-to-bucket transfers with the latter raising many new issues. Now with the frequency held fixed:

$$-\frac{dR}{R} = \frac{1}{\gamma^2 - \gamma t^2} * \frac{dB}{B} \text{ or at injection } \frac{dR}{R} = 0.0281 * \frac{dB}{B}$$

The BPG must be designed to be flexible to accommodate a slightly variable Booster injection frequency during a pulse, must be able to switch waveforms in the sub microsecond time scale to react to first turn Booster BPM measurements

Booster interface

Figure 4.3 shows Beam Pattern Generator interface with PIP-II Linac timing system and the Booster LLRF system. As shown, the BPG receives Booster reset signal from Time Line Generator, and reset trigger from timing system ACLK. During the Injection period, the BPG system will provide an RF signal with the proper frequency and phase angle for the Booster LLRF system. The Booster RF will lock to this RF signal. The BPG will send beam event and injection frequency to LCLK-II frontend and the Booster will receive beam start signal from LCLK-II clock. The BPG system will also provide a revolution marker for the Booster to identify the position of the gap buckets.

The BPG system will provide synchronization between PIP-II Linac and the Booster by producing an appropriate reduced beam bunch pattern that enables bucket-to-bucket transfer to the Booster RF at 46.46MHz (84th Revolution Harmonic).

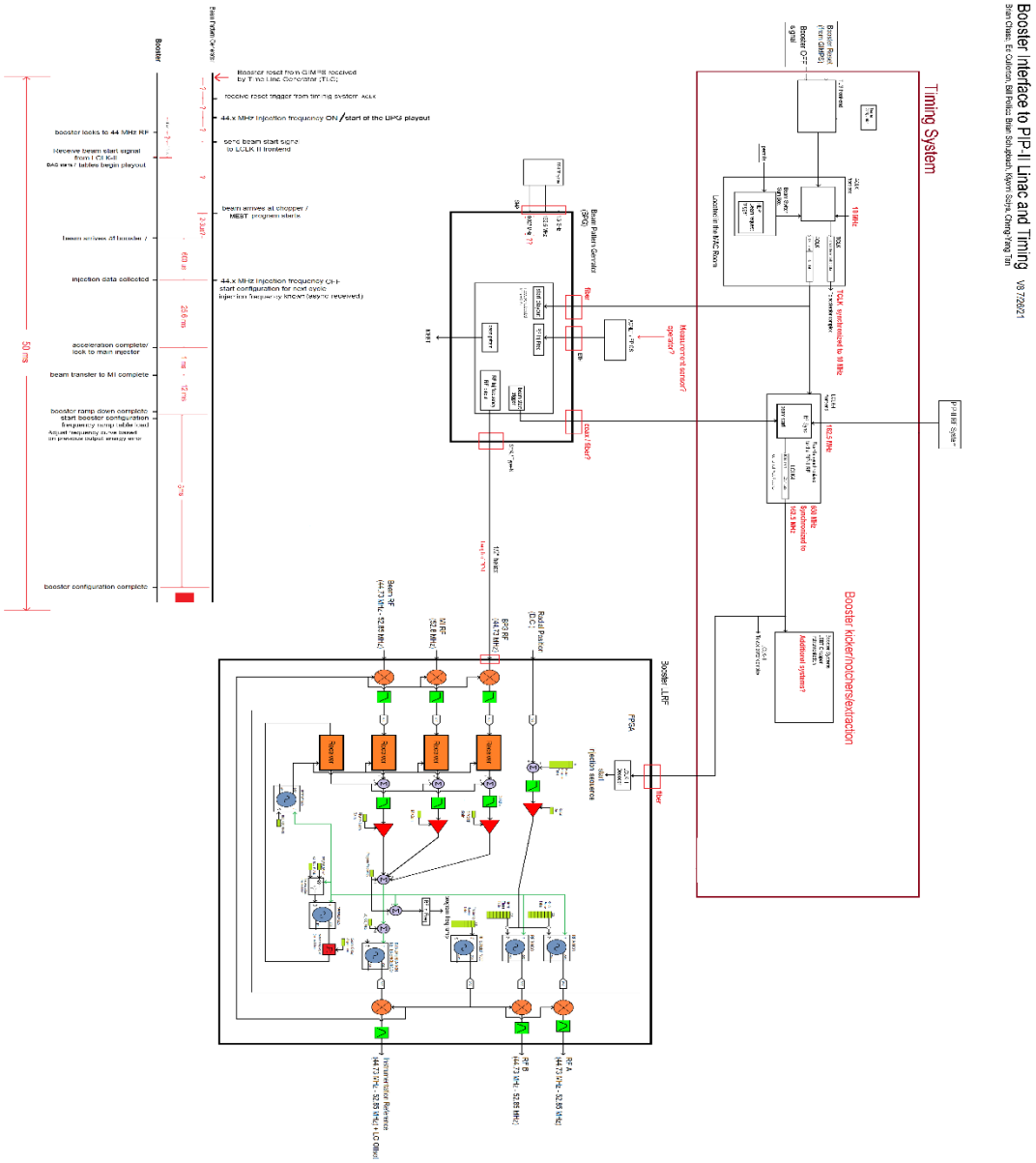

Figure 0.3: Booster and PIP-II Linac Interface [6]

Hardware

The BPG chassis includes four printed circuit boards as shown in fig 4.3.

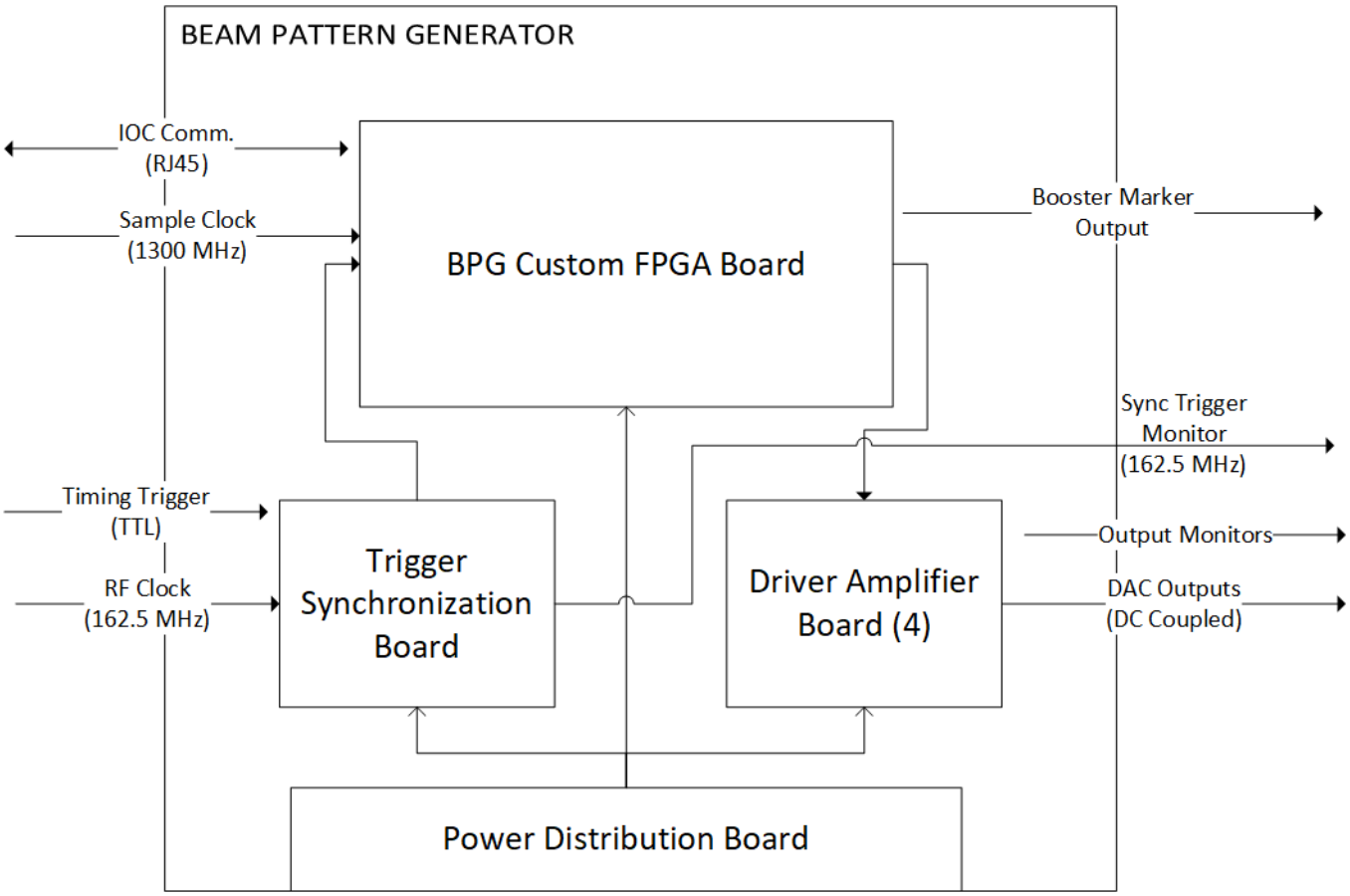

Figure 0.4: Block Diagram

BPG FPGA board

New custom FPGA architecture will be developed to facilitate 4 waveform output channels and IOC communication. It will have following features:

- Generates waveforms for fast kickers, synchronized to 1.3 GHz sample clock
- Supports 75ms of beam chopping waveforms
- (4) channel, > 1.3 GS/sec/chan, min. 12-Bit D/A resolution
- (6) channel, > 1.3 GS/sec/chan, 14-bit A/D resolution
    - 4 ADC channels for kickers, 1 for each coil
    - 1 ADC channels for Wall current monitor
    - 1 spare ADC channel
- DC Coupled into 50 ohms
- Programmable segmentation size, trig, looping, etc.
- (4) TTL marker outputs

Drive amplifier board

- Translates 750 mVp-p AWG output into 0-1.3V signal for kicker drive electronics
- Single ended output into 50 ohms

Trigger synchronization board

- Receives trigger from timing system, samples to the 162.5 MHz RF clock
- Contains adjustable delay line to ensure timing meets setup and hold times

Power distribution board

- Power supply for BPG FPGA board, drive amplifier board and trigger synchronization board

REQUIREMENTS

Performance

Table 0-1

Requirement #	**Requirement Statement**
T- ED0013972-A001	The BPG system shall calculate total waveform duration based on all requirements from all target machines under the supervision of a "Timeline Generator" and in concert with the MPS.
T- ED0013972-A002	The BPG system generated arbitrary pattern shall maintain extremely flat phase and amplitude response as needed to achieve the jitter requirement across random patterns, over the frequency span from DC to 300 MHz range.
T- ED0013972-A003	The BPG system should generate the stable waveforms for all four output channels with peak-to-peak jitter being sub 100 pico-seconds.
T- ED0013972-A004	The BPG system shall have a very high timing resolution requirement (~38ps), needed to precisely align the kick waveform with the beam.
T- ED0013972-A005	The BPG system shall generate waveforms for fast kickers, synchronized to 1.3 GHz sample clock

T- ED0013972-A006	The BPG system shall support 75ms of 1.3 GSPS waveforms in memory
T- ED0013972-A007	The BPG system shall have at least 12-bit D/A resolution for four(4) analog output channels with sampling rate ≥ 1.3 GSPS/channel and should be DC coupled into 50 Ohms.

T- ED0013972-A008	The BPG system shall have 6 ADC channels with 14-bit resolution.
	• (6) channel, ≥ 1.3 GSPS/channel
	  ○ 4 ADC channels for kickers, 1 for each kicker element
	  ○ 1 ADC channel for Wall Current Monitor
	  ○ 1 spare ADC channel
	• DC Coupled into 50 ohms

Operational

Table 0-2

Requirement #	**Requirement Statement**
T- ED0013972-B001	The BPG system shall provide channel to channel delay, individual channel falling/ rising edge adjustment capabilities with resolution of ~38 ps.
T- ED0013972-B002	The BPG system shall drive the fast kickers as per beam pattern input binary file, channel delays and pulse width adjustment parameters.
T- ED0013972-B003	The BPG system shall provide an RF signal with the proper frequency and phase angle for the Booster RF to lock to during the injection period.
T- ED0013972-B004	The BPG system shall provide a revolution marker for the Booster to identify the position of the gap buckets.
T- ED0013972-B005	The BPG system shall provide an output trigger, precisely aligned with the 162.5 MHz and 1300 MHz RF.
T- ED0013972-B006	The BPG system shall have provision to drive the LEBT Chopper

T- ED0013972-B007	The BPG system shall be able to flip the phase direction for individual channels.
T- ED0013972-B008	Performance and testing data shall be available in a database for the BPG system equipment.

Physical Characteristics

Table 0-3

Requirement #	**Requirement Statement**
T- ED0013972-C001	The BPG system's equipment shall be designed to be installed in standard 19" wide racks. The chassis shall be 3 RU, designed for mounting in a 19" rack based on EIA-310.
T- ED0013972-C002	The chassis shall have a depth no greater than 14". The chassis shall be able to be easily disassembled. The top of the chassis shall be able to be removed for easy access inside for debugging.
T- ED0013972-C003	All BPG RF cables shall be selected based on performance characteristics at 1.3 GHz. All BPG signal runs shall be designed to be as short as reasonably possible.

Reliability, Maintainability, and Availability

Table 0-4

Requirement #	**Requirement Statement**
T- ED0013972-D001	All printed circuit boards (PCBs) shall meet IPC2221B standard. All wiring and chassis design shall meet UL61010 standard.
T- ED0013972-D002	All BPG system non-trivial components shall have unique serial numbers.
T- ED0013972-D003	All BPG system complex subsystem components shall have model, revision, and design IDs on them (PCB boards, chassis).

T- ED0013972-D004	The BPG must have a hot spare operating in a test stand.

Environmental Conditions

Table 0-5

Requirement #	Requirement Statement
T- ED0013972-E001	The BPG chassis shall be able to operate over the temperature range of the PIP-II gallery

Transportability

Table 0-6

Requirement #	Requirement Statement
T- ED0013972-F001	The BPG system internal chassis connections shall be designed to withstand normal transport and handling acceleration and loads.
T- ED0013972-F002	The chassis shall be sturdy enough to handle transport shocks and not require special handling when being moved.

Software

Table 0-7

Requirement #	Requirement Statement
T- ED0013972-G001	The BPG software application shall have an EPICS interface and communication link with IOC.
T- ED0013972-G002	The software shall provide status indicators for communication link between BPG hardware and BPG application on high level GUI display.
T- ED0013972-G003	The software shall be able to generate pattern files based on the Booster and other target machine requests

T- ED0013972-G004	The BPG software shall be able to link pattern files for the output waveforms stored in memory based on multiple target beam needs as requested by controls
T- ED0013972-G005	The software shall provide control to enable/ disable waveforms for all BPG output channels.
T- ED0013972-G006	The BPG system must raise a flag for Machine Protection System (MPS) when the BPG chassis is not detected by the application or if the BPG is not ready to deliver the proper pattern or if there is any system failure.
T- ED0013972-G007	The controller shall use an algorithm developed at Fermilab implemented in firmware. This algorithm development is ongoing.

Interface

Table 0-8

Requirement #	**Requirement Statement**
T- ED0013972-H001	The BPG system shall have an input trigger, LVTTL signal from timing system.
T- ED0013972-H002	The BPG system shall have an input 162.5 MHz RF clock from global clock distribution system, used for trigger re-synchronization.
T- ED0013972-H003	The BPG system shall have an input 1300 MHz sampling clock.
T- ED0013972-H004	The BPG system shall receive +/- 10V Kicker monitor signals from Kicker electronics.
T- ED0013972-H005	The BPG system shall generate four waveform analog output signals with beam pattern, 0-1.3 Volts into 50 Ohms load. Four channels include Kicker drive, the Booster, and spare channels.

T- ED0013972-H006	The BPG system shall generate at least four LVTTL into 50 Ohms Marker signals for Booster, oscilloscope monitoring and spare channels.
T- ED0013972-H007	The BPG system shall generate an output trigger signal, synchronized with 162.5 MHz RF clock, to be used by the kicker system.
T- ED0013972-H008	The BPG system shall have 10/100/1000 Mbps Ethernet connection to communicate with IOC.
T- ED0013972-H009	The BPG system shall have 4 Gbps QSFP fiber connection to communicate with other sub-systems.
T- ED0013972-H010	The BPG system shall have USB serial communication available for system debug purpose.

- All external connections to the BPG chassis shall be as per described in [BPG ISD document]

Safety

- The system shall abide by all Fermilab ES&H (FESHM) and all Fermilab Radiological Control Manual (FRCM) requirements including but not limited to:

Table 0-9

Electrical Safety
• FESHM Chapter 9110 Electrical Utilization Equipment Safety
• FESHM Chapter 9190 Grounding Requirements for Electrical Distribution and Utilization Equipment
Radiation Safety
• FRCM Chapter 8 ALARA Management of Accelerator Radiation Shielding
• FRCM Chapter 10 Radiation Safety Interlock Systems
• FRCM Chapter 11 Environmental Radiation Monitoring and Control
General Safety
• FESHM Chapter 2000 Planning for Safe Operations

Any changes in the applicability or adherence to these standards and requirements require the approval and authorization of the PIP-II Technical Director or designee.

In addition, the following codes and standards in their latest edition shall be applied to the engineering, design, fabrication, assembly, and tests of the given system:

NFPA 70 – National Electrical Code
IEC Standards for Electrical Components

In cases where International Codes and Standards are used the system shall follow FESHM Chapter 2110 Ensuring Equivalent Safety Performance when Using International Codes and Standards and requires the approval and authorization of the PIP-II Technical Director or designee.

Additional Safety Requirements that are not listed in the general list above shall be included in the Requirements table in the Functional Requirements section.

Design and Construction Standards

UL61010 - Laboratory equipment
UL60950 - Computing/Telecommunication Equipment
ASHRAE - Datacenter Standards
IPC-JSTD-001 – Soldering
IPC2221 – PCB spacing and design
IPC-A-600 -- PCB acceptance and testing
IPC-A-610 -- Electronics assembly

VERIFICATION

Bench level testing

- Control systems interface
    - Verify all PVs on EPICS screens are communicating with BPG chassis appropriately. Read and write functions for PVs should be checked on bench and prior to start using BPG chassis at PIP-II.

- Software functionality
    - Key features of BPG application includes loading pattern from CSV file, adjusting channel delay, rising edge delay, falling edge advance etc.
    - All these features need to be tested on bench

- Drive Signal testing for timing, amplitude, jitter (Two tone tests)

- Check the amplitude level for all BPG output channels using oscilloscope. For the pattern, beam pass must represent 0-0.5 volts and kick must represent 1.2-1.5 volts range
- Adjust timing parameters to verify pulse width can be adjusted. Default pulse width is 6.15ns and can be adjusted with resolution of ~38ps.
- Verify system jitter in range of sub 100ps.

- Input ADC test with single tone and two-tone measurements
- Triggers and monitors
  - Verify beam pattern using oscilloscope by connecting to monitor channels

QUALITY CONTROL

- The BPG system procurements shall use Fermilab standard procurement process and shall be tested prior to assembly of the BPG system.
- Visual inspection of all circuit boards will be completed prior to use to build BPG chassis.
- The BPG system shall comply with the LLRF Quality Control Plan (Document # TBD)

APPENDIX A – *(NOTES, BACKGROUND, DIAGRAMS, CALCULATIONS, ETC.)*

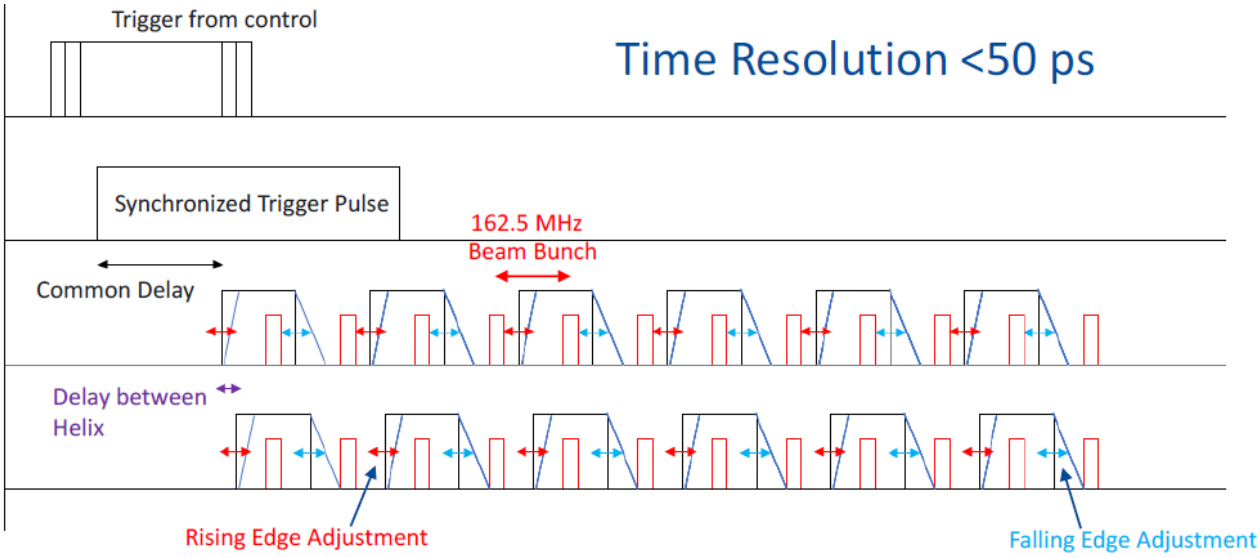

Figure 7.01: Timing

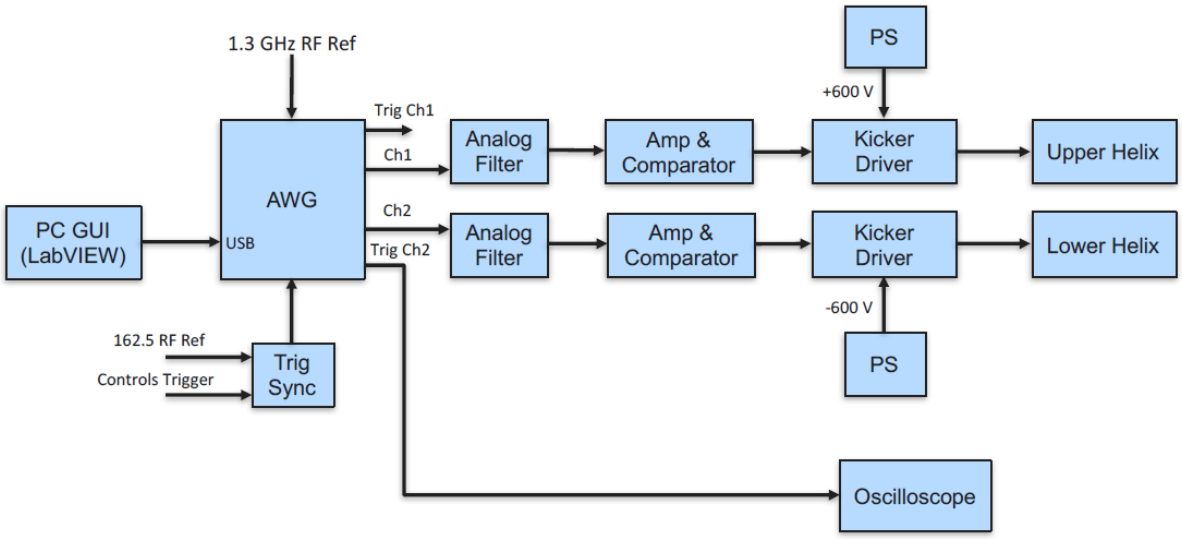

Figure 7.02: Chopper System Implementation