Midterm Report

Studies of the trigger performance of the ICARUS T600 detector at Fermilab

08 – 29 – 2022

Riccardo Triozzi

Supervisors:

Angela Fava
Donatella Torretta

Imaging Cosmic And Rare Underground Signals

SBN Program

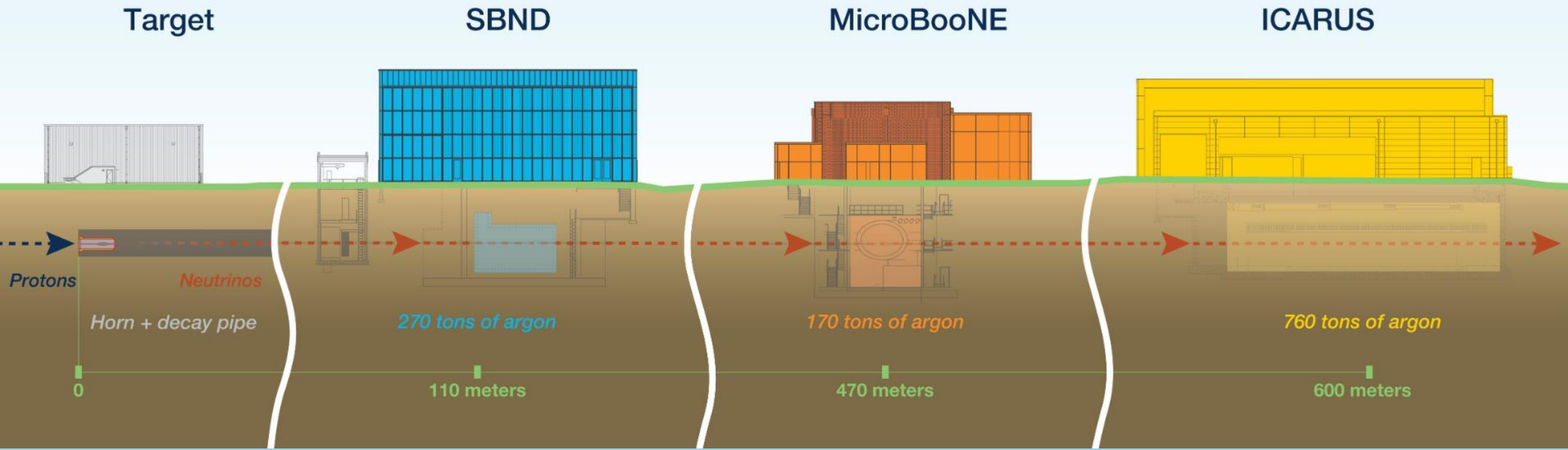
The SBN Project

- Three Liquid Argon TPC (**LAr-TPC**) detectors at increasing baselines on the Booster Neutrino Beam (**BNB**)

- **ICARUS**, at 600 m from target, on short baseline is the far detector and will collect neutrinos also from the **NuMI** beam (off-axis)

Goals:

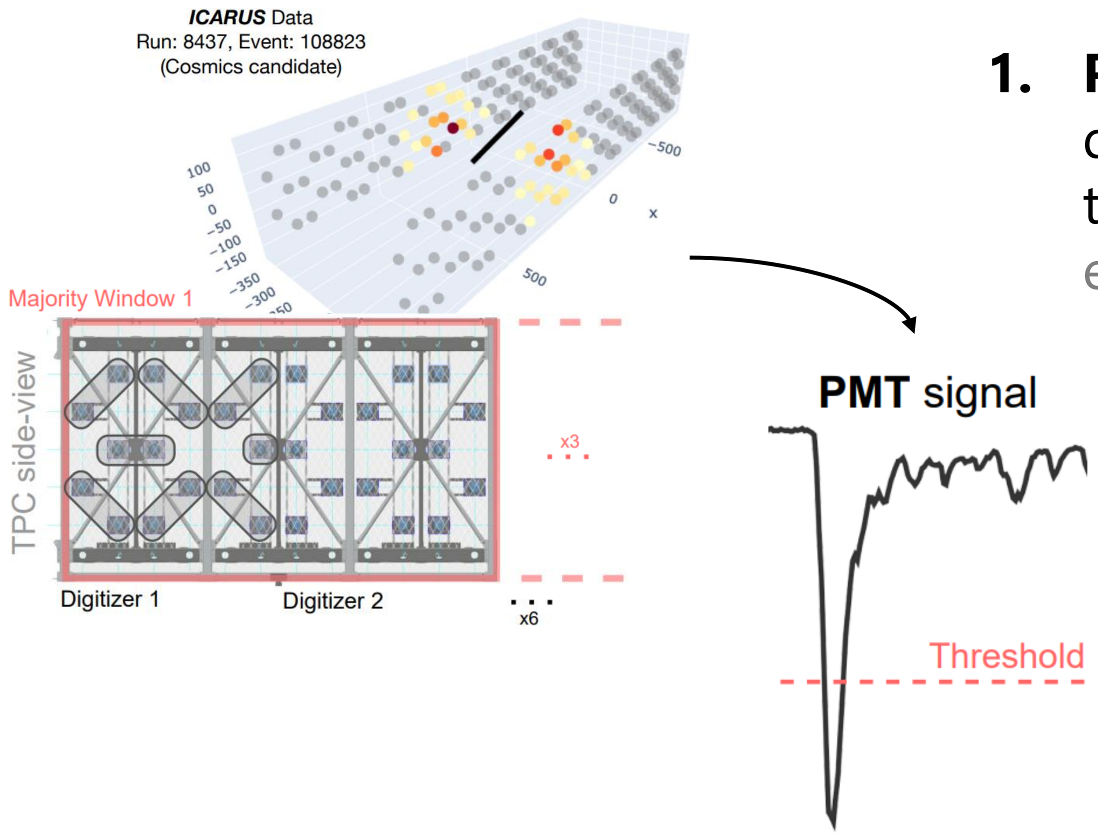
- Test the allowed parameter space of past anomalies at $>5\sigma$ with BNB
- Test the Neutrino-4 oscillation hypotesis with disappearance of ν_μ from BNB and ν_e from NuMI
- Study ν(~3 GeV)-LAr with NuMI for DUNE



The ICARUS T600 Detector

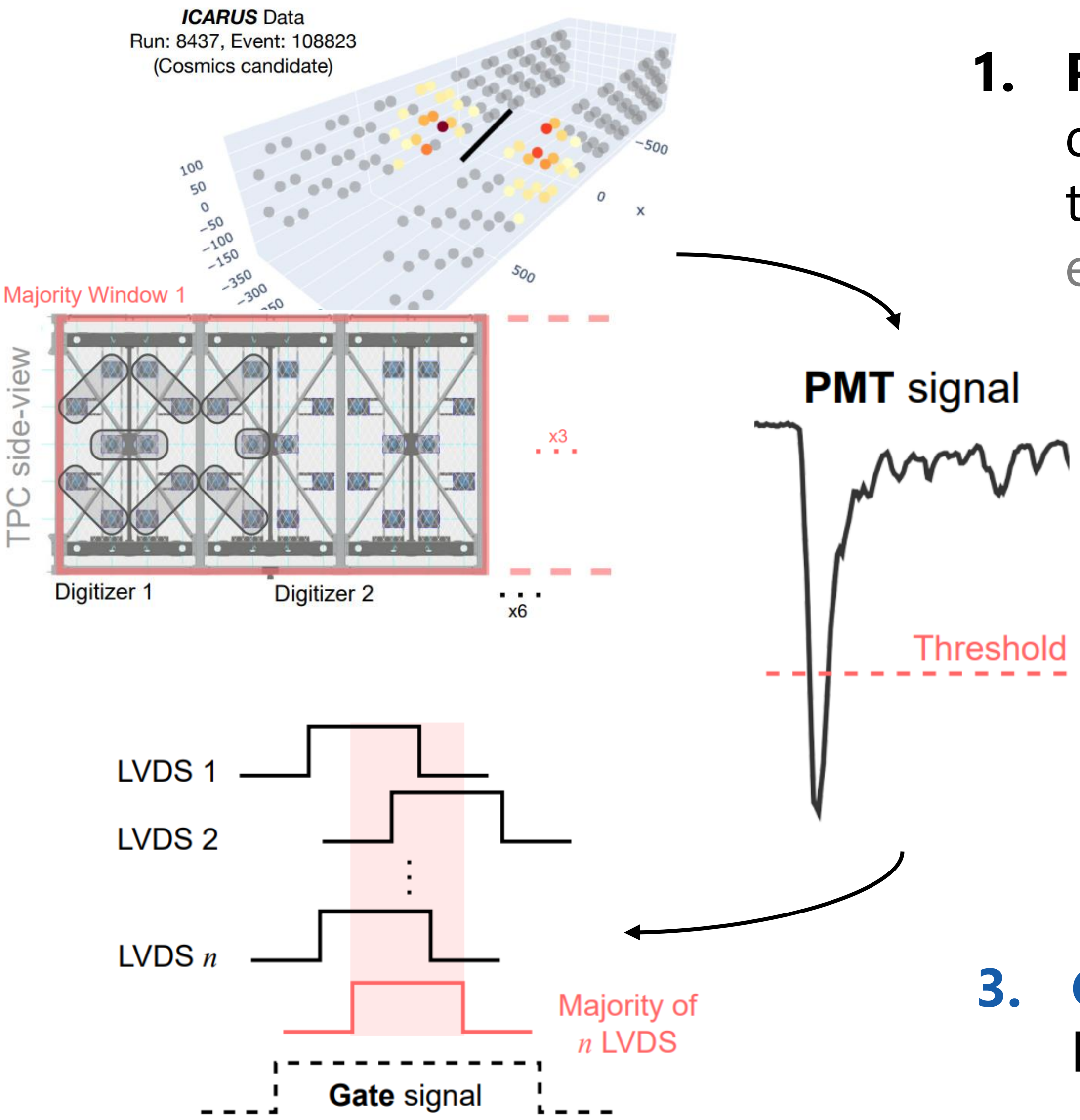
- LAr-TPC high granularity self-triggering detector with 3D **imaging** and calorimetric capabilities, ideal for ν physics
- Two **cryostats**, each with 2 **TPC**s with a common central cathode (nominal configuration: HV = 75 kV, E = 0.5 kV/cm and 1.5 m drift length)
- Ionization charge continuously read *non-destructively* by 3 wire planes
- Scintillation light read by a system of 360 8” **PMT**s (180 per cryostat) for timing and triggering

The ICARUS T600 Detector: trigger working principle



1. **PMT signals** are digitized at 500 MHz and discriminated with a 400 ADC (i.e., 8 photoelectrons) threshold, generating **LVDS** logical outputs (one every pair of adjacent PMT, combined in OR)

The ICARUS T600 Detector: trigger working principle



1. **PMT signals** are digitized at 500 MHz and discriminated with a 400 ADC (i.e., 8 photoelectrons) threshold, generating **LVDS** logical outputs (one every pair of adjacent PMT, combined in OR)

2. FPGA processing based on a **majority logic**: at least 5 LVDS signals in front facing 6 m-sections along the longitudinal direction (30 PMTs x 2 sides) to produce a majority trigger primitve

3. **Global trigger**: trigger primitive coincident with the beam gate (e.g., 1.6 µs for BNB)

The ICARUS T600 Detector: trigger working principle

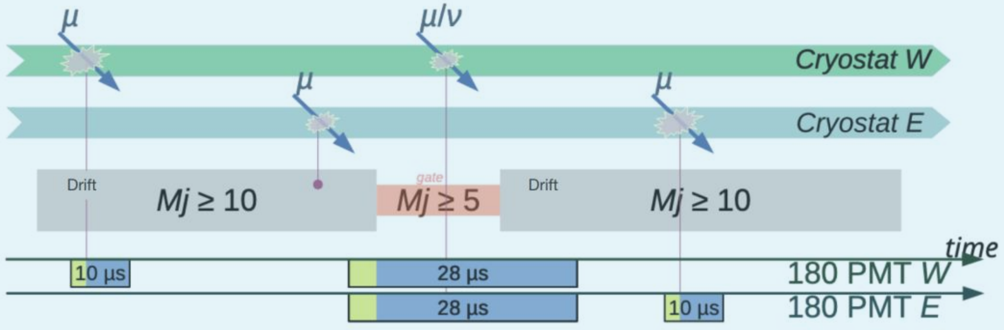
In presence of a **global trigger**, readout of **TPC** (for 1.5 ms), **PMT** (500 MHz sampling frequency) and **CRT** is activated:

- **Beam Trigger**: gate signal synchronized with beam spill, recording PMT waveforms in the 28 μs around the trigger time to fully cover the spill region

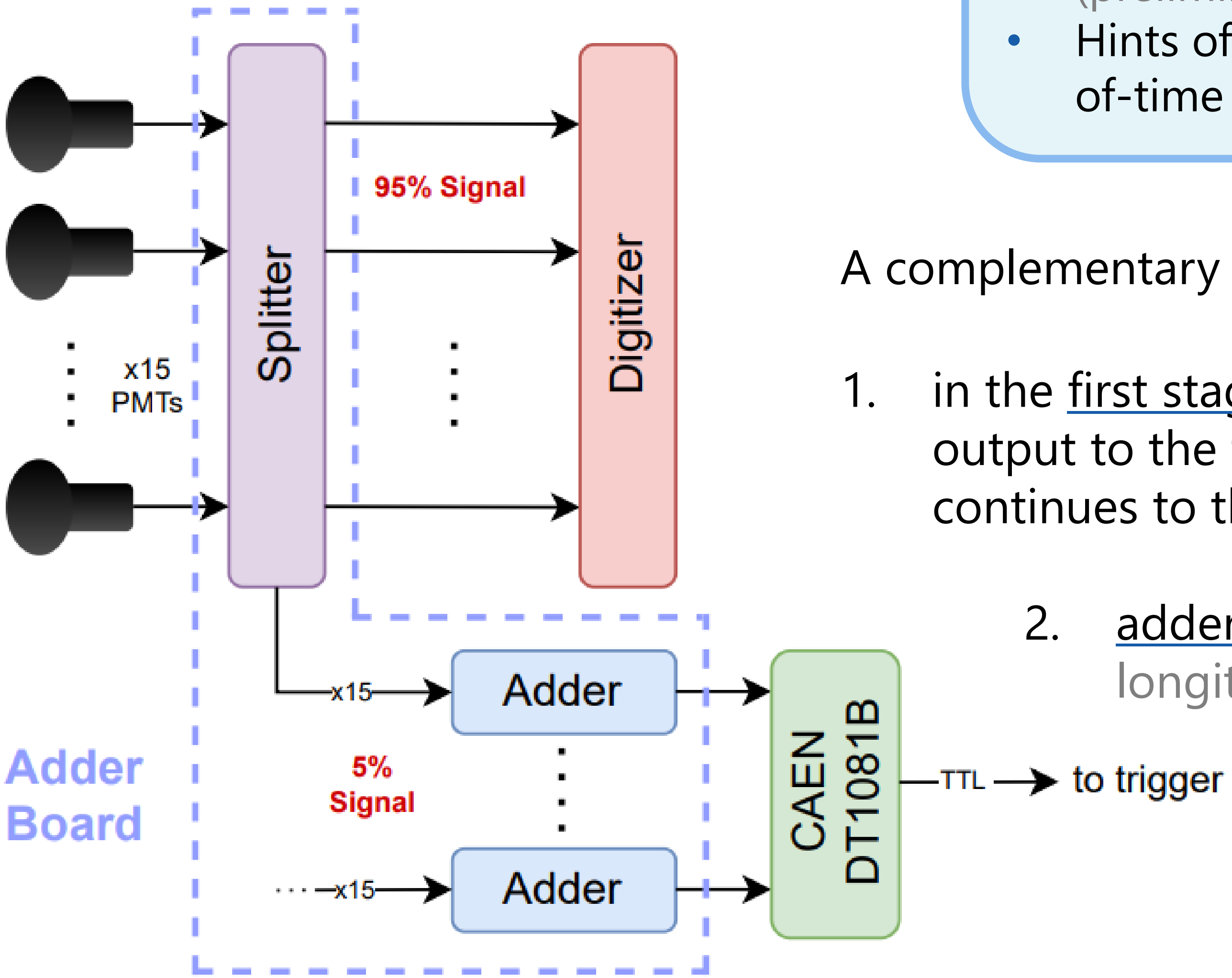
Main physics trigger for ICARUS

- **Out-of-time PMT Trigger**: shorter 10 μs acquisition windows of PMT waveforms, collected in presence of a majority-10 trigger primitive outside of the beam spill in a 2 ms window around the global trigger

Allow recording of all scintillation light activity related to Cosmic Rays (CRs) during the TPC drift time (key to cosmic brackground rejection)



Adders Trigger System



Motivation:

- Global trigger **efficiency** is >97% at E > 300 MeV (preliminary analysis on MC and collected data)
- Hints of lower efficiency in CRs detection for out-of-time PMT triggers

A complementary system was proposed, based on ***adder* boards**:

1. in the first stage of the board, the PMT signal is **split**: 95% is output to the front panel (and sent to the digitizers), 5% continues to the adder stage
2. adder stage: analog **sum** of 15 PMTs (3 m in the longitudinal direction)
3. each analog sum is **discriminated** with an external module and sent to the trigger system

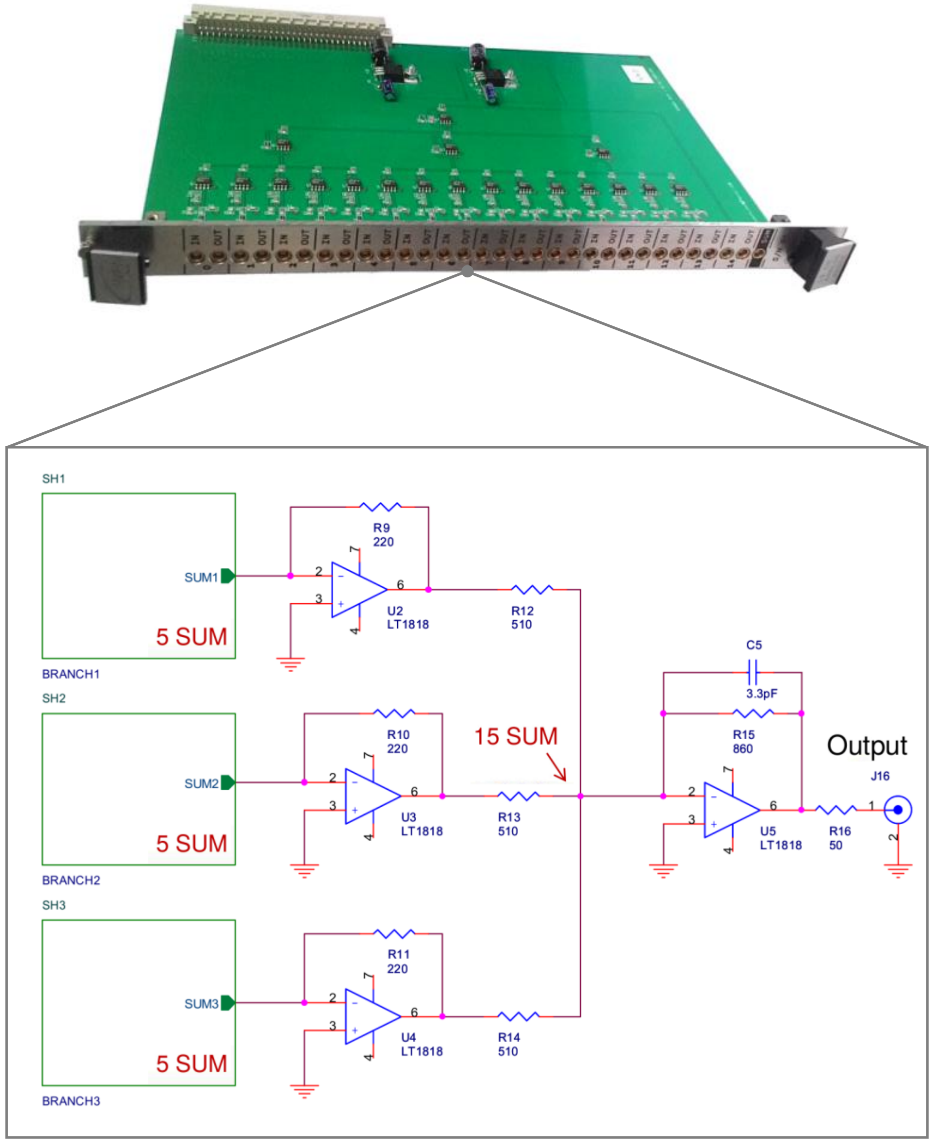
Adders Trigger System

Advantages:

- could help identify events with small detector occupancy (e.g., cosmic tracks close to the corners of the detector)
- can be combined with the majority trigger

My tasks:

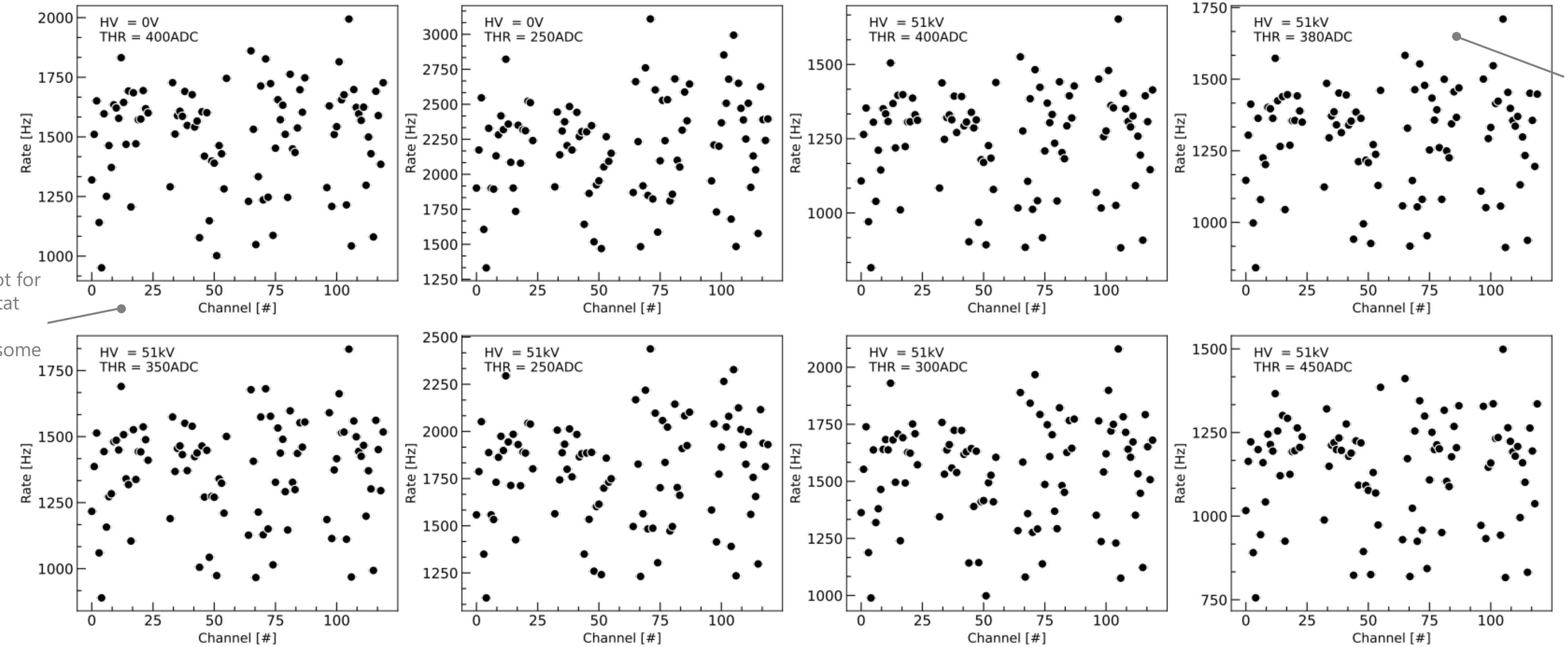
- check that there is no drop in performance w. r. t. the existing trigger system
- charactherize adder signal to define the optimal discrimination threshold
- investigate how to process the signal and how to combine the adders with the majority trigger system



LVDS Rate Measurements

Get **LVDS counts** every 10 seconds for 5 – 10 minutes, i.e. sets of 30 – 60 measurements per channel (done via LabView software running on the FPGA)

various configurations of High Voltage (**HV**) and LVDS discrimination **threshold** were tested



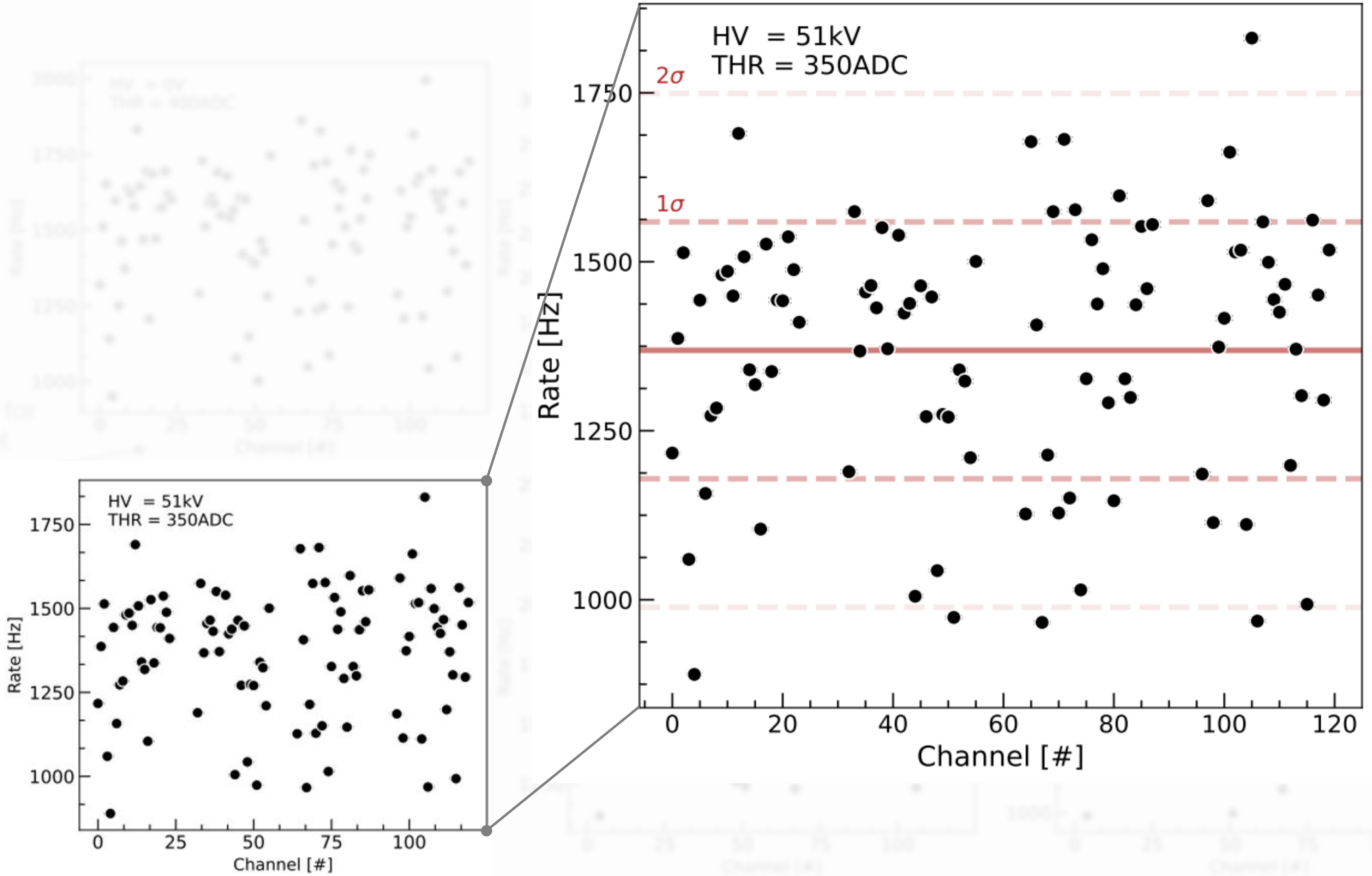
Example of plot for the **west** cryostat (96 non-zero channels) and some of the tested configurations

Uncertainty on y is the **standard error** and is contained within the marker

LVDS Rate Measurements

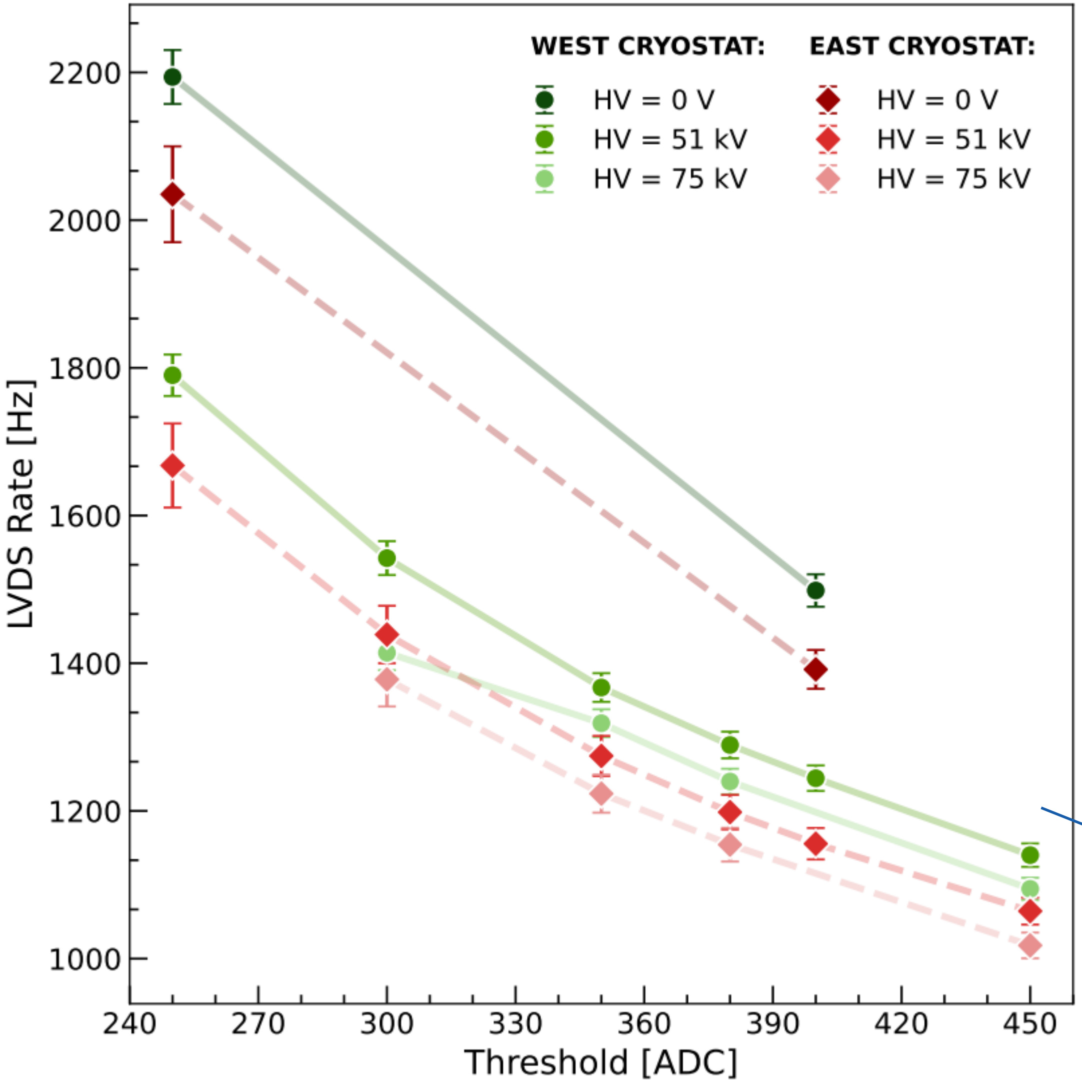
Get **LVDS counts** every 10 seconds for 5 – 10 minutes, i.e. sets of 30 – 60 measurements per channel (done via LabView software running on the FPGA)

various configurations of High Voltage (**HV**) and LVDS discrimination **threshold** were tested



- Rate data of different LVDS channels is always within 3σ w. r. t. the mean
- For each threshold and HV configuration, the **mean** between all LVDS channels will be considered (uncertainity is the standard error)

LVDS Rate Trend: different drift field configurations

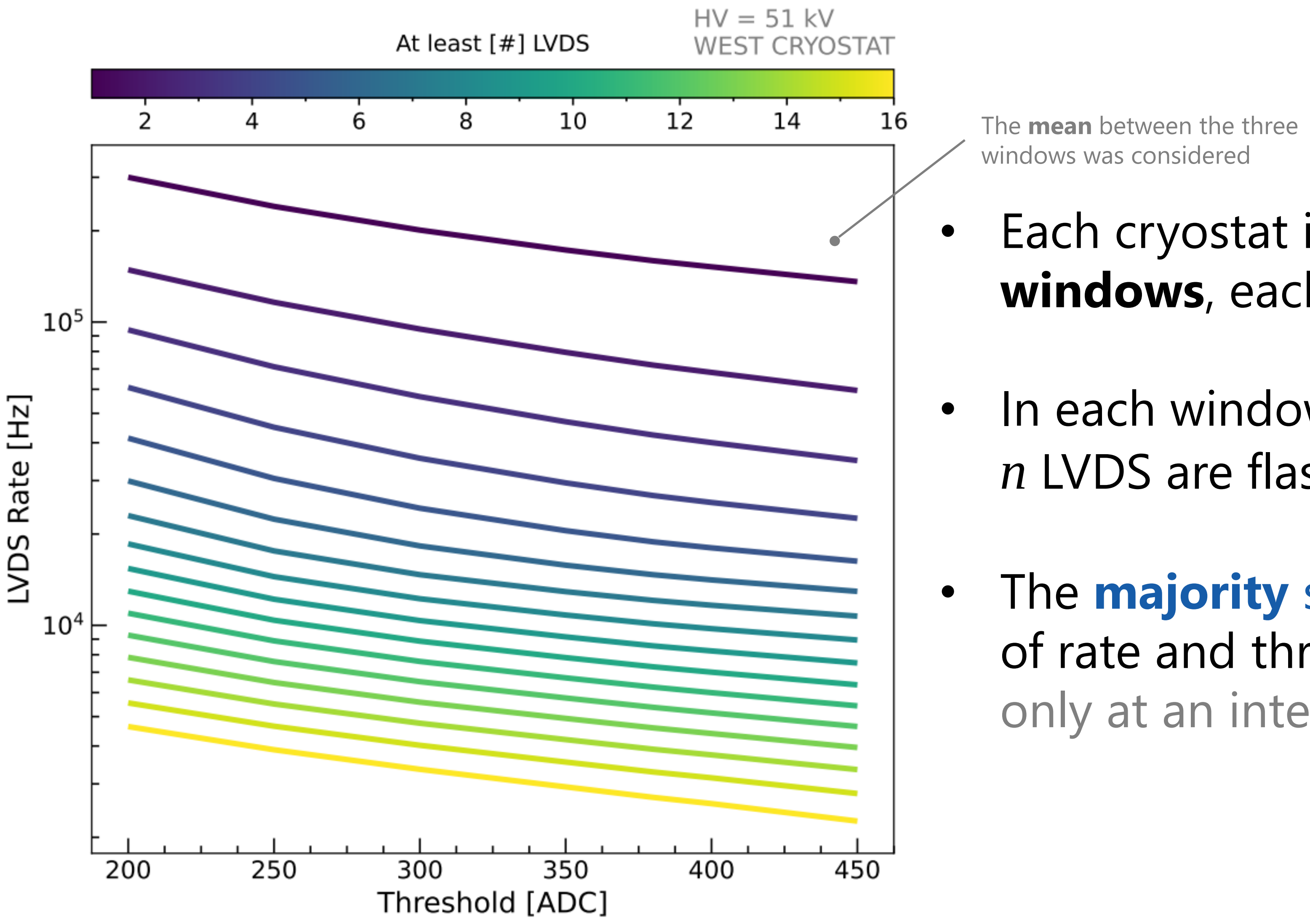


- Rate trend as a function of the LVDS discriminator **threshold** (usually equal to 400 ADC, i.e. 8 photoelectrons)

- Data taking with three **drift field** configurations (HV = 0, 51, 75 kV)

LVDSs (hence PMTs) of the west cryostat have a rate 5 – 10% **higher** w. r. t. the east cryostat

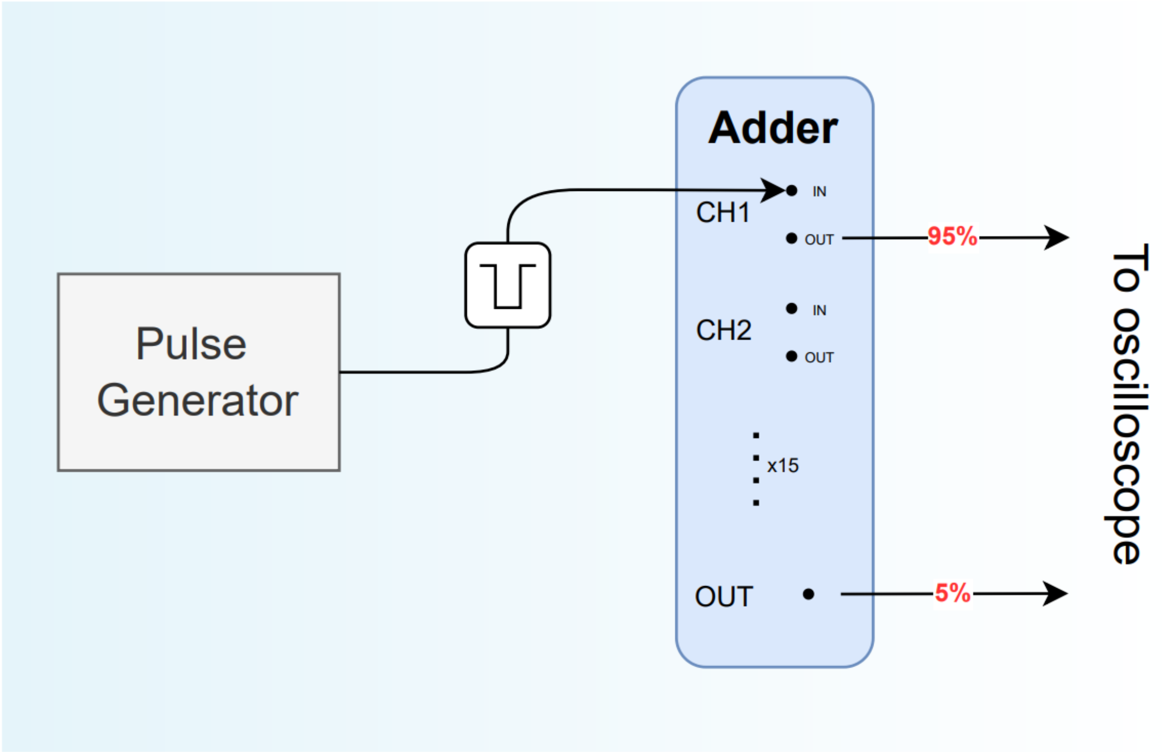
LVDS Rate Trend: different majorities



- Each cryostat is divided in three no sliding **windows**, each with a majority pattern
- In each window, counter goes off when at least n LVDS are flashed (n ranges from 1 up to 16)
- The **majority** system was studied as a function of rate and threshold (as of now, data was taken only at an intermediate drift field, HV = 51 kV)

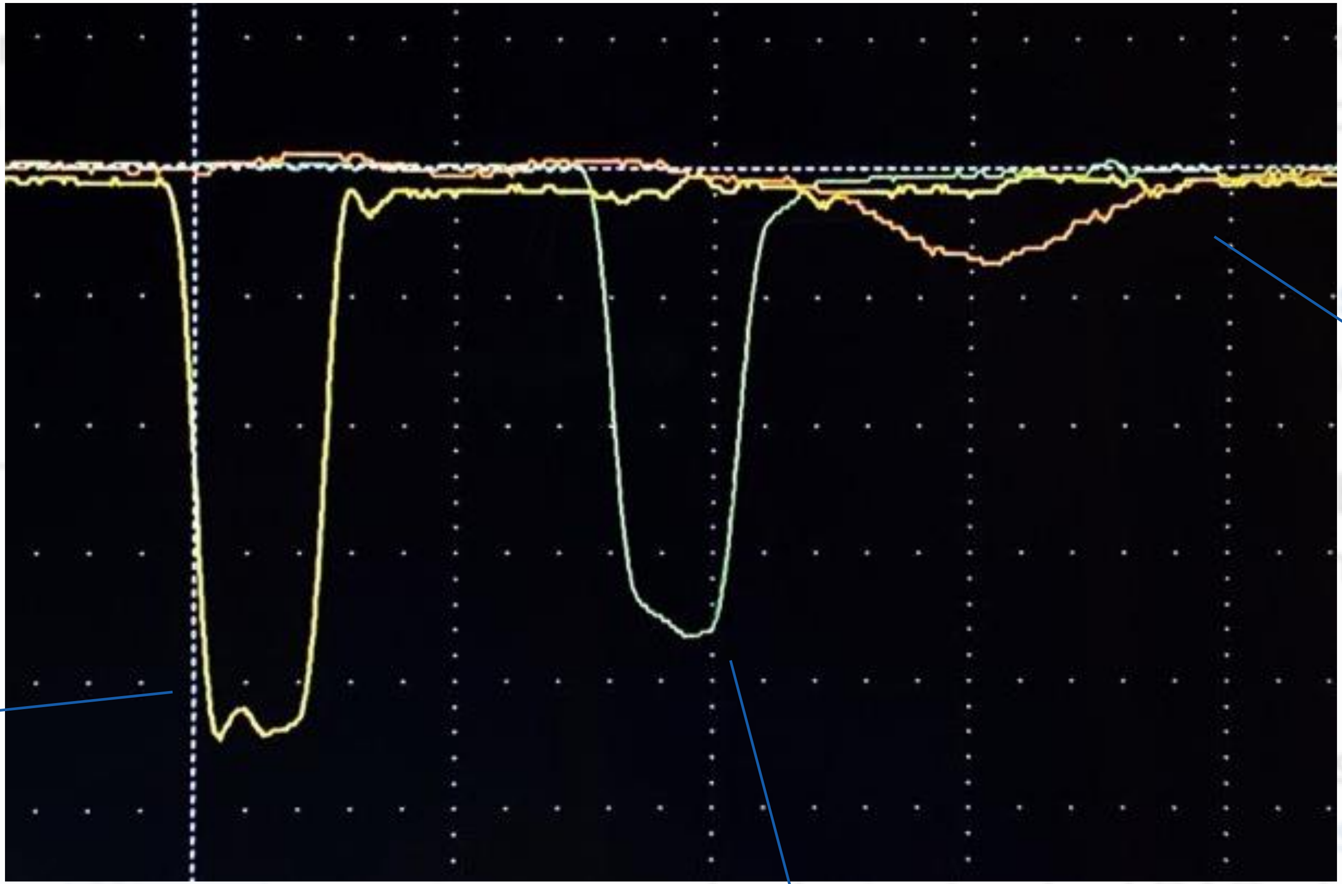
Adders: preliminary tests

The functionality of all channels was verified for **all the boards** (24 boards, 15 channels per board) with a pulse generator and an oscilloscope:



- tested with a **negative pulse** (1 V amplitude, 1 MHz frequency, 99% duty cycle)
- input, channel output and board output signals were checked on an oscilloscope and **compared**
- signals ampltidues for the same channel don't add up to 100%, more tests are needed (e.g., check via standard DAQ of the PMT waveforms with the laser calibration system)

Adders: preliminary tests



Channel input has an amplitude of ~ 850 mV

Channel output is around 80% of the input signal (~ 675 mV amplitude)

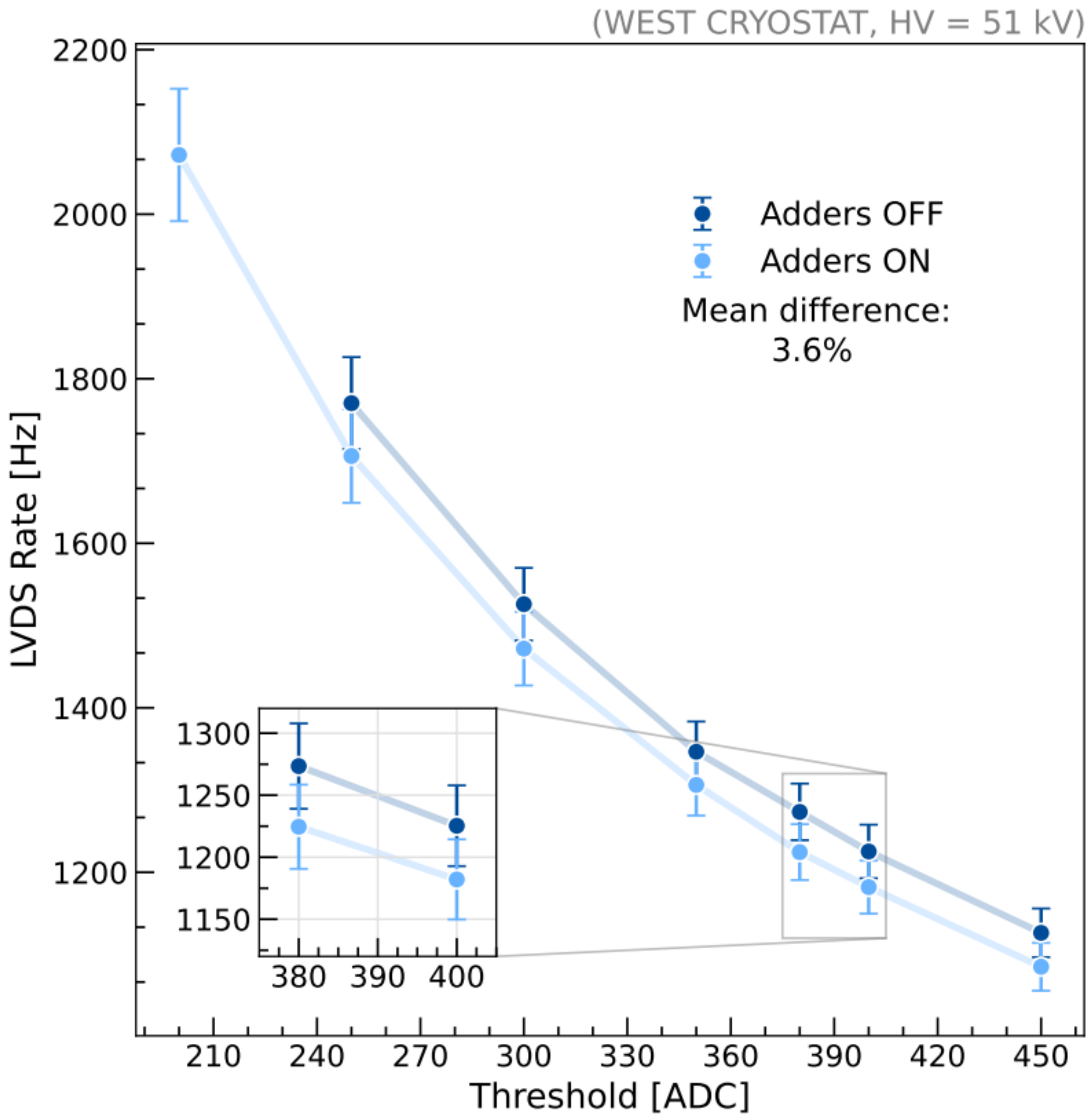
Board output is around 5% of the input signal (~ 40 mV amplitude)

LVDS Rate Trend: after the installation of adder boards

- LVDS rate data was collected as a function of the LVDS discrimination **threshold** for four **adders** (corresponding to the 60 PMTs of the first majority window)

- The LVDS rate **decreases** by ~ 4% w. r. t. the previous configuration

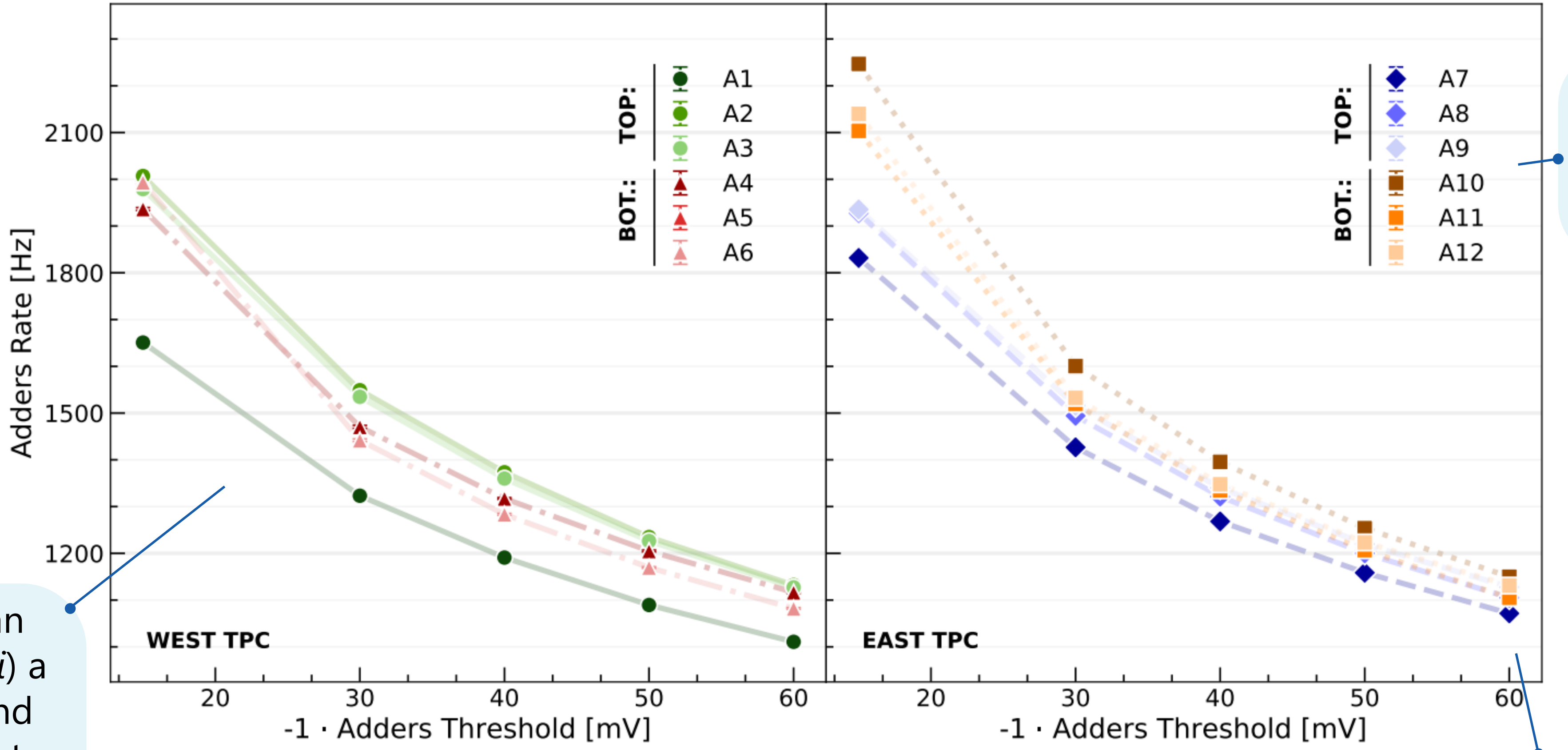
- To achieve the same rate with the adder configuration, we may lower the nominal **threshold** from 400 ADC to 380 ADC



Adders Rate Trend: different discriminator thresholds

- **Fully** cabled and tested all the west cryostat's adder boards (overall, 12 out of 24)
- Tested the adders rate trend as a function of the adder discrimination **threshold**:

(WEST CRYOSTAT, HV = 51 kV)

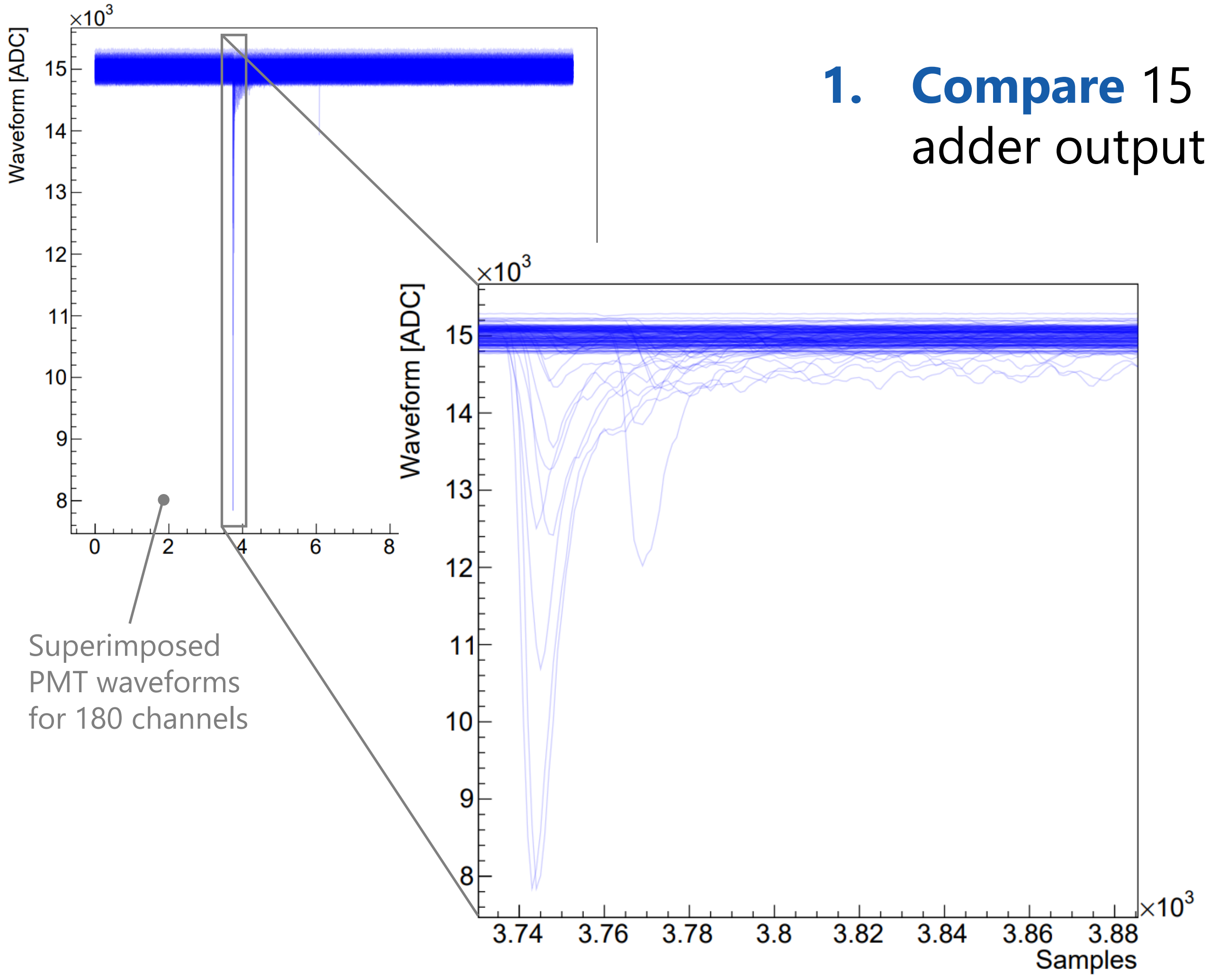


Groups of adjacent adder boards show **similar** rates

A1's **low rate** can be explained by (*i*) a PMT being off and (*ii*) PMTs being at the edge of the TPC

A7 has a **lower rate** w. r. t. A8 and A9, due to PMTs being at the edge

Foreseen activities



1. **Compare** 15 PMT waveforms to the corresponding adder output signal
2. Characterize the adder output waveform (baseline, amplitude, rise time, …) and compare **distributions** to the PMT waveform's ones
3. Understand how each PMT **contributes** to an adder's signal
4. Estimate the **optimal** discrimination **threshold** from the waveform analysis

Thank you!