DAPHNE at CERN

Integration and Status

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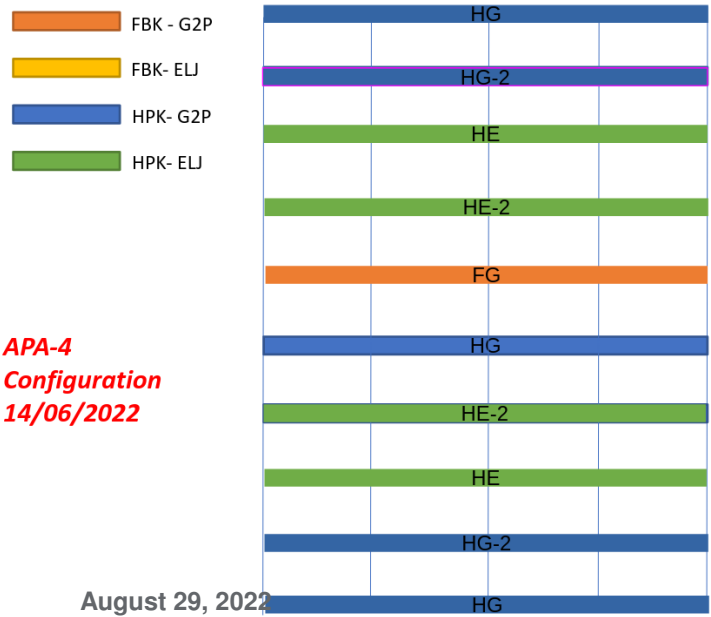
August 29, 2022

UNIVERSIDAD EIA
Ser, Saber y Servir

DUNE

Introduction

- 2 activities are running in parallel at CERN concerning DAPHNE.
  - DAQ integration
  - Stand alone readout from coldboxes
- For sure we will need more than 4 DAPHNEs at CERN for ProtoDUNE II. The PD modules are unevenly distributed in APA 4. (Channel 5 is the only FBK Module)
- In the standalone setup, we use GbETH in the entire readout of the cold boxes (APA 1, 2, 3, 4) because, on the warm side, the cables don't reach the mini racks on top of the NP04.
- Timing interface has to be integrated again due to the upgrade they are making.



APA-4 Configuration 14/06/2022

DAQ Integration

- I'm preparing a new version of the timing Unitary Test using the enclustra board and a new protocol for the endpoint.
- Slow Control and DAQ slow communication: Hardware is already working using the Raspberry Pi OPC-UA server. (This is still the most probable solution due to the bugs of the OPC-UA in the STM)
- The OPC-UA server will be used for DAQ communication with DAPHNE using a different namespaces for each.

Activities

We are not prepared to check the system version of the readout with FELIX on the last Coldbox.
The new CRC will be tested this week using the old timing endpoint.

APA 2 PD characterization

VI curves have been taken using different methods

- Long time measurement.
- We obtain big error measuring the Breakdown Voltage this way.

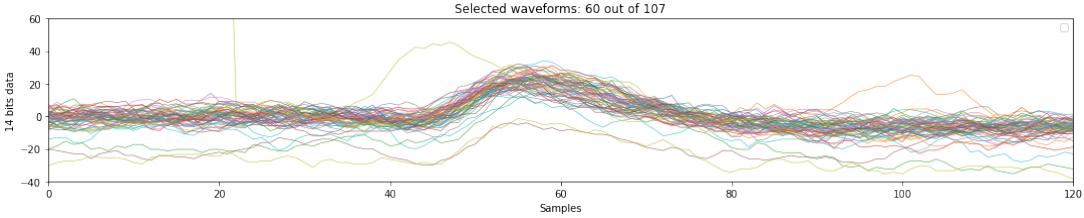
Characterization Using the Gain

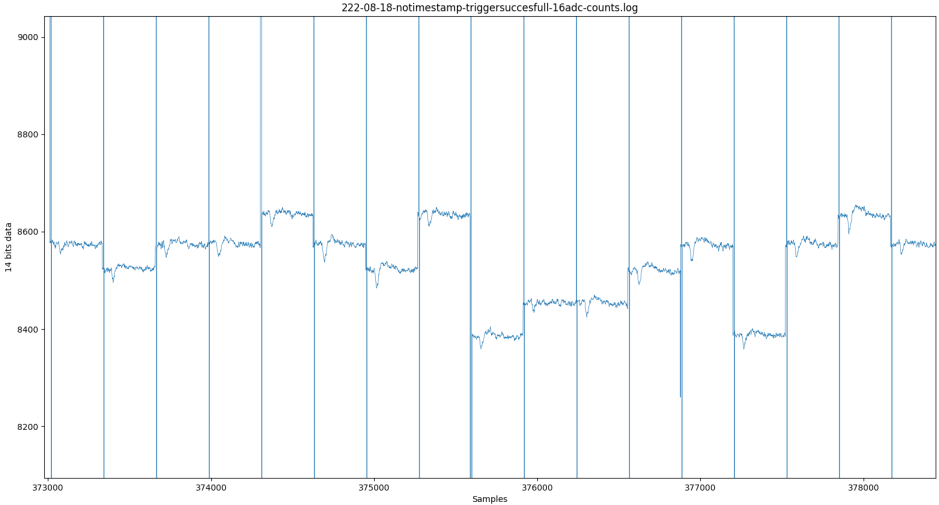
- We are planing to take different runs using different Voltages.
- We are able to calculate the Breakdown Voltage from the histograms.

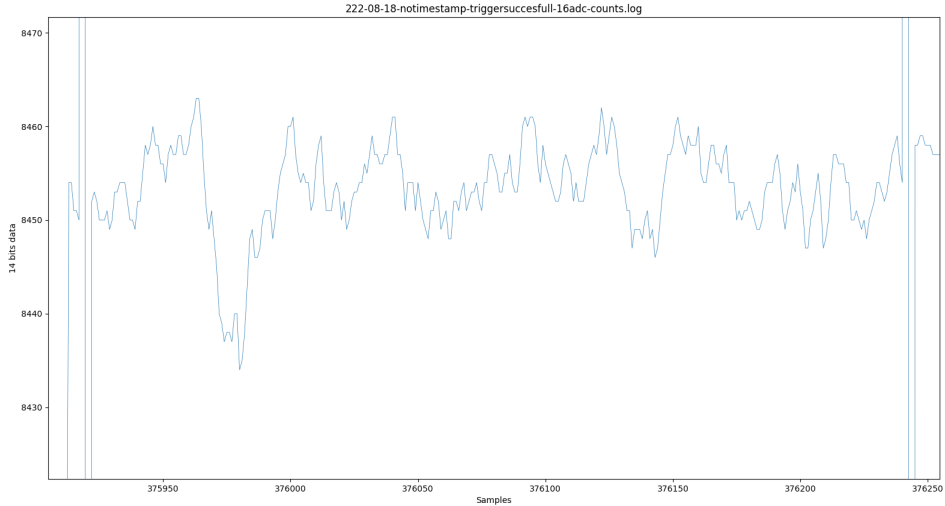
Self trigger in Coldbox. Single PE

We've achieved the self trigger at the 16 counts level.

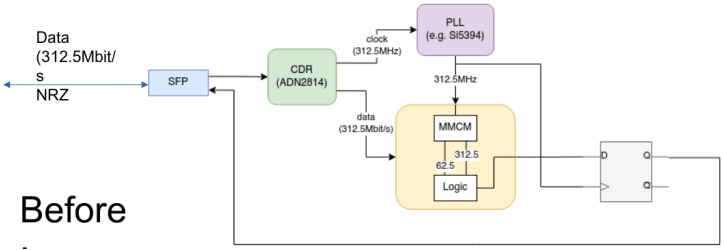
- We are using a moving average algorithm.
- This project is using same resources as the previous versions.




222-08-18-notimestamp-triggersuccesfull-16adc-counts.log
9000
8800
8600
8400
8200
14 bits data
373000
374000
375000
376000
377000
378000
Samples


222-08-18-notimestamp-triggersuccesfull-16adc-counts.log
8470
8460
8450
8440
8430
14 bits data
375950
376000
376050
376100
376150
376200
376250
Samples

Timing



Before

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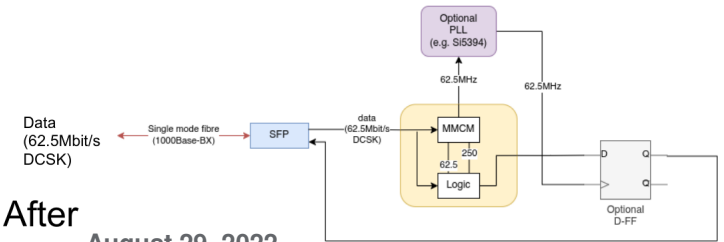
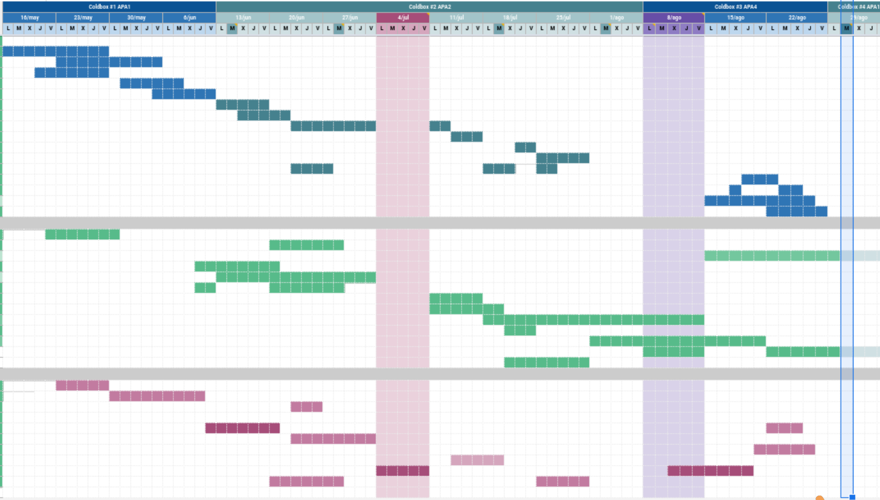


After

PD Warm Electronics Activities at CERN (Manuel)

#	TASK	DURATION	% COMPLETED
1.0	Test DAPHNEs at CERN	3	100 %
1.0.1	Prepare the first readout for the blackbox	1	100 %
1.1	DAPHNE setup for Colbox #1	2	100 %
1.2	Calibration of BIAS and Offset (Board #9)	2	100 %
1.3	APA 1 READOUT	1	100 %
1.4	APA 1 DATA ANALISIS	2	100 %
2.0	External Trigger (Zelymir fibers)	1	100 %
2.1	APA 2 READOUT 1st Cooldown	1	100 %
2.2	APA 2 Noise tests	1	100 %
2.3	APA 2 READOUT 2nd Cooldown	1	100 %
2.4	APA 2 READOUT 3nd Cooldown	1	100 %
2.5	APA 2 Noise tests	1	100 %
2.6	APA 2 DATA ANALISIS	1	100 %
3.0	APA 4 READOUT	1	100 %
3.1	APA 4 Noise tests	1	100 %
3.2	APA 4 Self Trigger (Concept test)	2	70 %
3.3	APA 4 Grounding Tests	1	100 %
2	**DAQ Integration**		
2.0	Raspberry Py Server (Slow Control)	1	100%
2.1	Timing Intefgration First UT	2	100 %
2.2	Timing Intefgration Second UT	2	70 %
2.3	Preparation TOP NP04 DAPHNE V2 with Xavier	2	100 %
3.0	Triggering Scheme	8	70 %
4.0	Felix Loopback Test	2	100 %
4.1	FELIX Fake sender	3	100 %
4.2	FELIX streaming test	6	100 %
4.3	CDR Corrections and streaming optimization	4	90 %
4.4	FELIX 2 transceivers test	1	100 %
5.0	Different Studies on self trigger	8	90 %
5.1	Different studies on data Streaming	8	50 %
6.0	ST Fast ETH (Work with Jonathan E.)	1	50 %
3	**Help Different Instrumentation Activities**		
3.1	PD Assembly APA # 2	1	100 %
3.2	PD Instalation APA # 2	1	100 %
3.1.1	PD Assembly APA # 4	1	100 %
3.2.1	PD Instalation APA # 4	1	100 %
3.3	Standalone Grounding	1	100 %
3.3.1	PD - TPC Noise studies	2	100 %
3.4.1	PD Instalation APA # 3 (Pipe wrong)	1	100 %
3.5	Connecting aables for bottom APAs	1	100 %
4.0	VD Instrumentation	1	100 %
5.0	DAPHNE DAQ Modifications	1	100 %

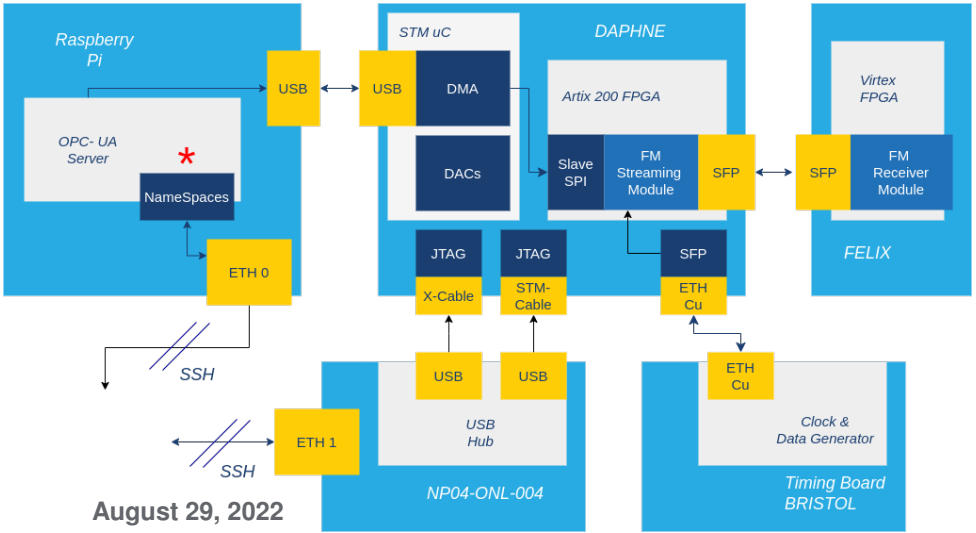


References

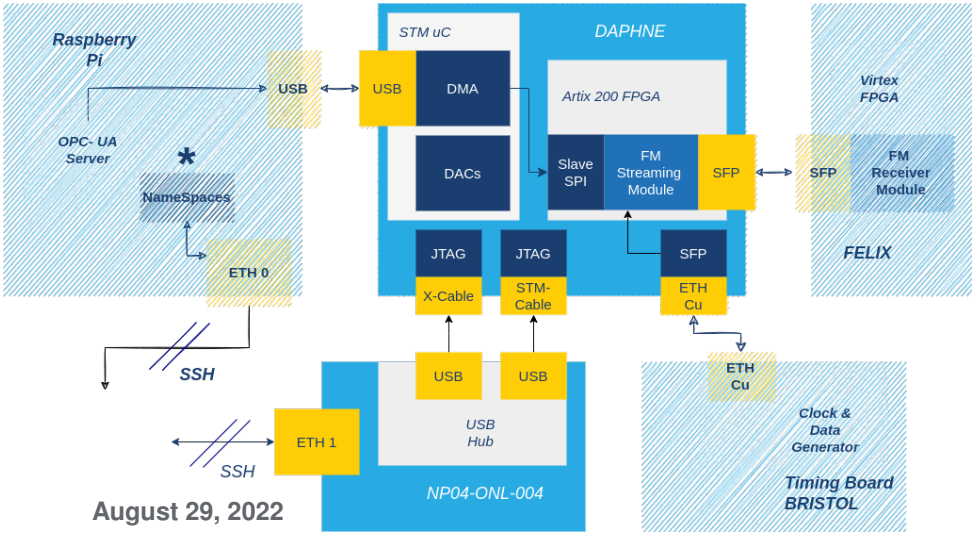
- Description of the protocol change of the timing
- New Endpoint no CDR
- Gantt Diagram, PD Warm Electronics Activities at CERN (Manuel)


DEEP UNDERGROUND
NEUTRINO EXPERIMENT

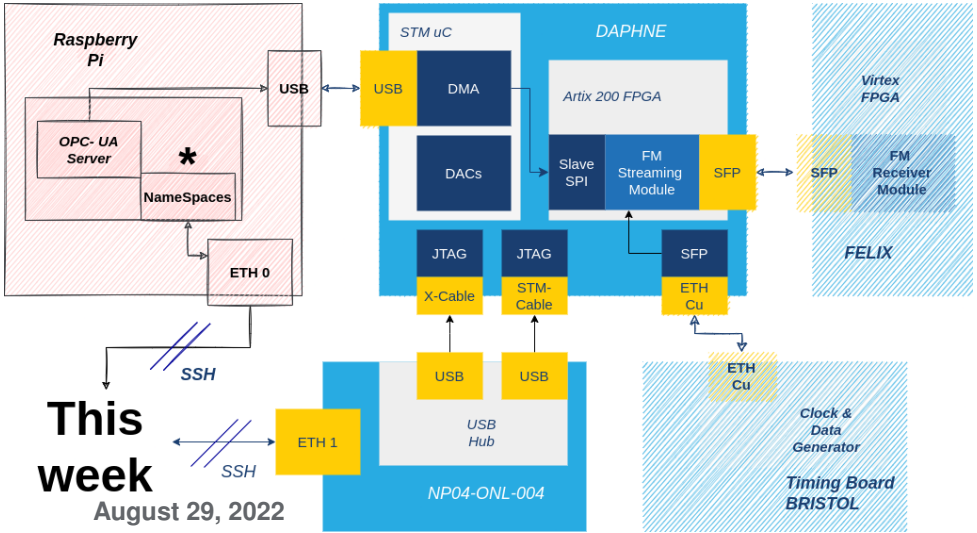
DAPHNE Connections



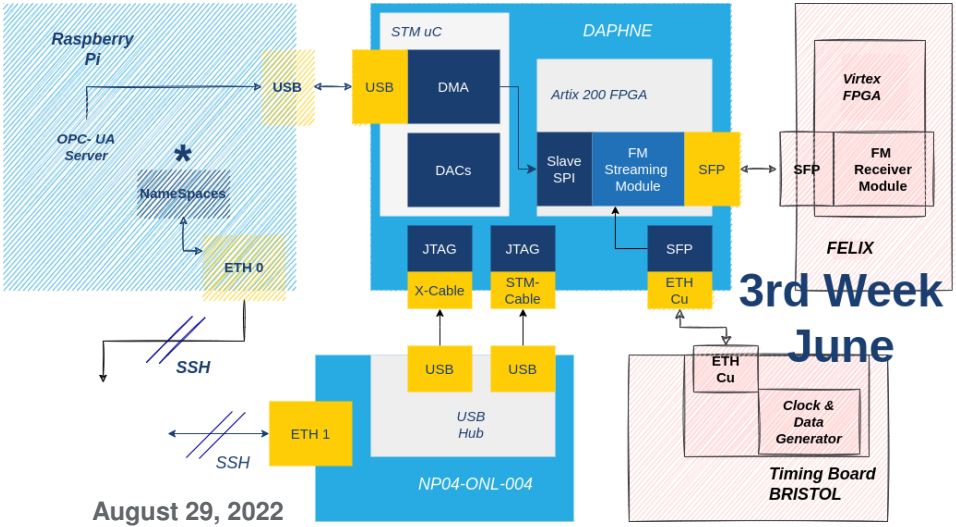
Tested Connections



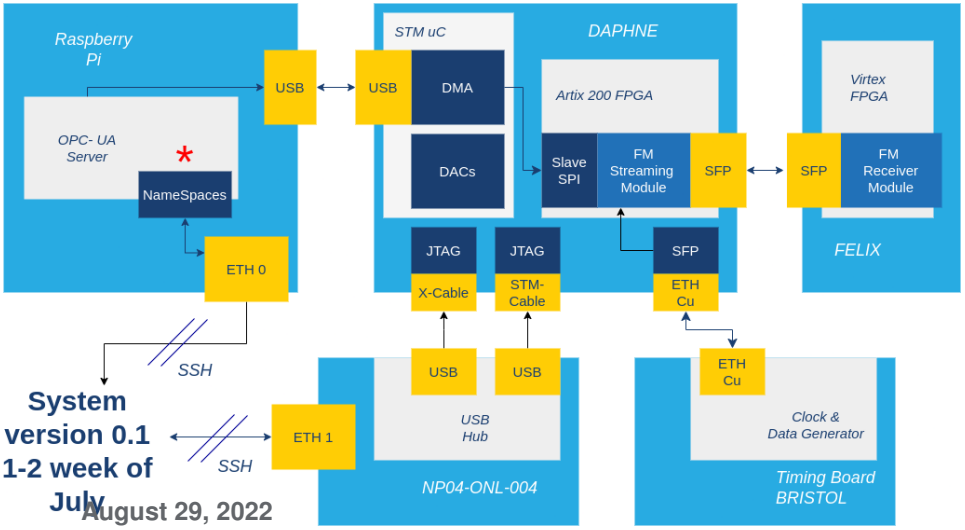
OPC-UA Server with serial Communication



Clock recovery and Readout (FM)



DAQ Loops of Control?

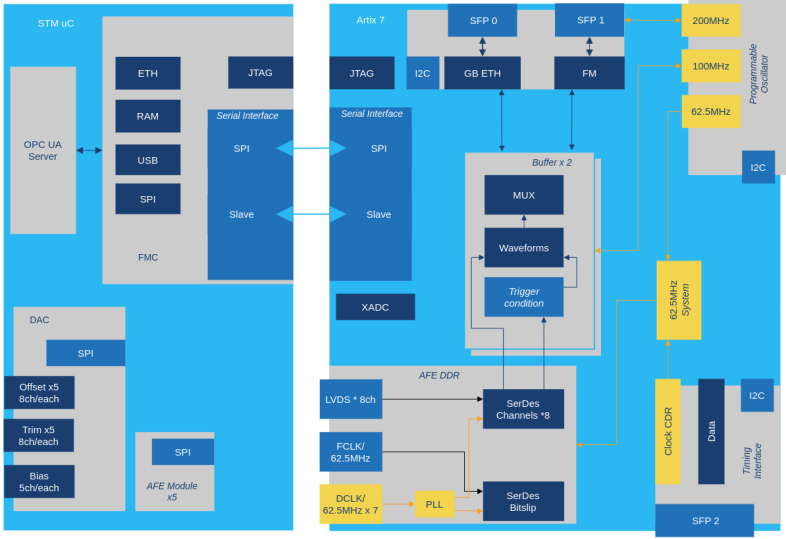


DAQ Format

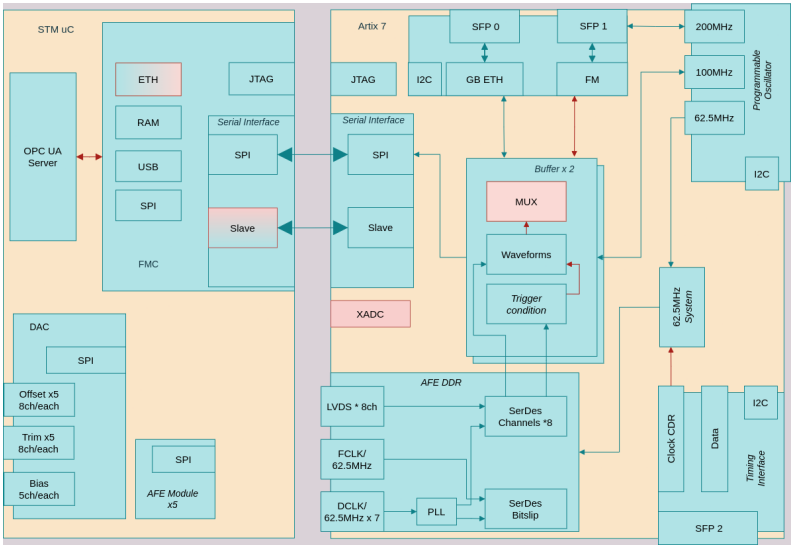
Created: 16 Mar.2021
Updated: 18may2022
Version: v2.0

	K/D	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0001	0x00								0x00								0x00								SOF (K28.1)							
1	0000	14-bit Trigger Peak height																Channel #								DAPHNE #						Data Version#	
2	0000	20-bit PDS Reserved Bits																								12-bit WF length in Words							
3	0000	Packet Counter[31:0]																															
4	0000	Timestamp Waveform [31:0]																															
5	0000	Timestamp Waveform [63:32]																															
6	0000	T(2) [3:0]				T(1) [13:0]																T(0) [13:0]											
7	0000	T(4) [7:0]								T(3)[13:0]																T(2)[13:4]							
8	0000	T(6)[11:0]														T(5)[13:0]													T(4)[13:8]			
9	0000	T(9)[1:0]				T(8)[13:0]																T(7)[13:0]										T(6)[13:12]	
10	0000	T(11)[5:0]								T(10)[13:0]														T(9)[13:2]									
11	0000	T(13)[9:0]														T(12)[13:0]										T(11)[13:6]							
12	0000	T(15)[13:0]																T(14)[13:0]												T(13)[13:10]			
13	0000	T(18) [3:0]				T(17) [13:0]																T(16) [13:0]											
142	0000	T(313)[1:0]				T(312)[13:0]																T(311)[13:0]										T(310)[13:12]	
143	0000	T(315)[5:0]								T(314)[13:0]														T(313)[13:2]									
144	0000	T(317)[9:0]														T(316)[13:0]										T(315)[13:6]							
145	0000	T(319)[13:0]																T(318)[13:0]												T(317)[13:10]			
146	0000	32-bit flex word																															
147	0000	BUSY Signal				CRC-20																				EOF (K.28.6)							
148	0001	0x00								0x00								0x00								IDLE (K.28.5)							

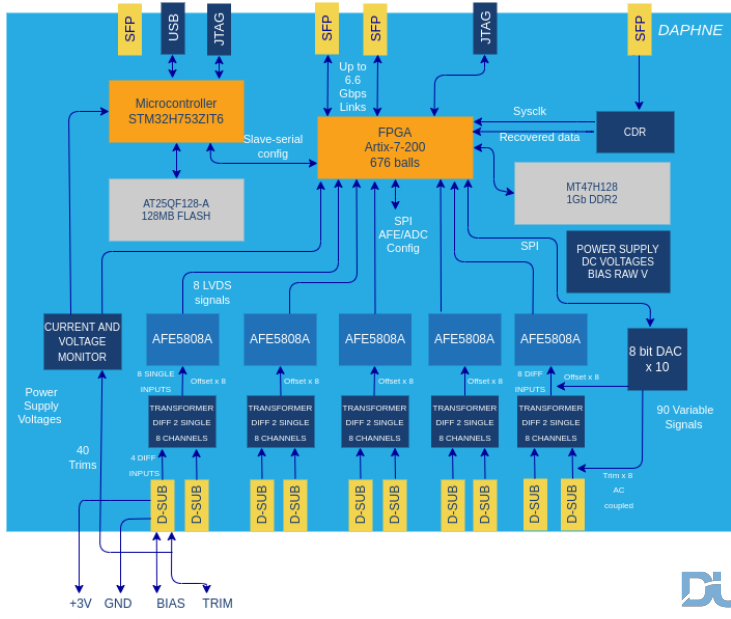
Firmware Scheme



Firmware Scheme Status



Hardware Scheme



Hardware Scheme Status