Overview of the FD1 TPC Electronics

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Lawrence Berkeley National Laboratory

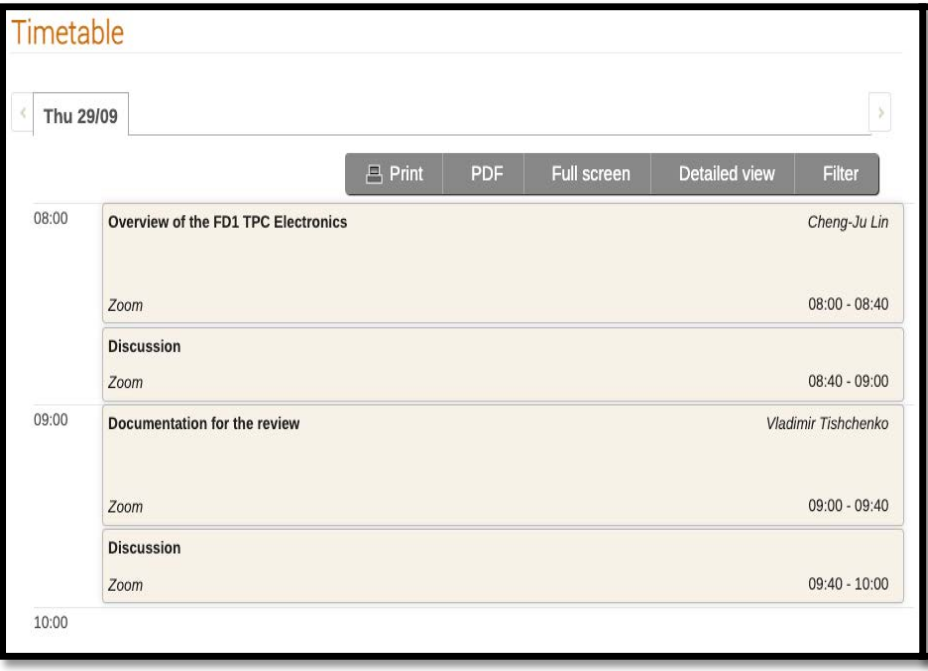
FD1 TPC Electronics Final Design Review
29-30 September 2022

Thank you for taking time to serve on the FD1 TPC Electronics FDR Committee

Your assessments and recommendations are important to us

Agenda for this Review

- Document-based review. Reviewers will have a few weeks to go over the documentation and ask questions
- Two presentations today: overview talk and another one on the documentation
- Plenty of time for discussion

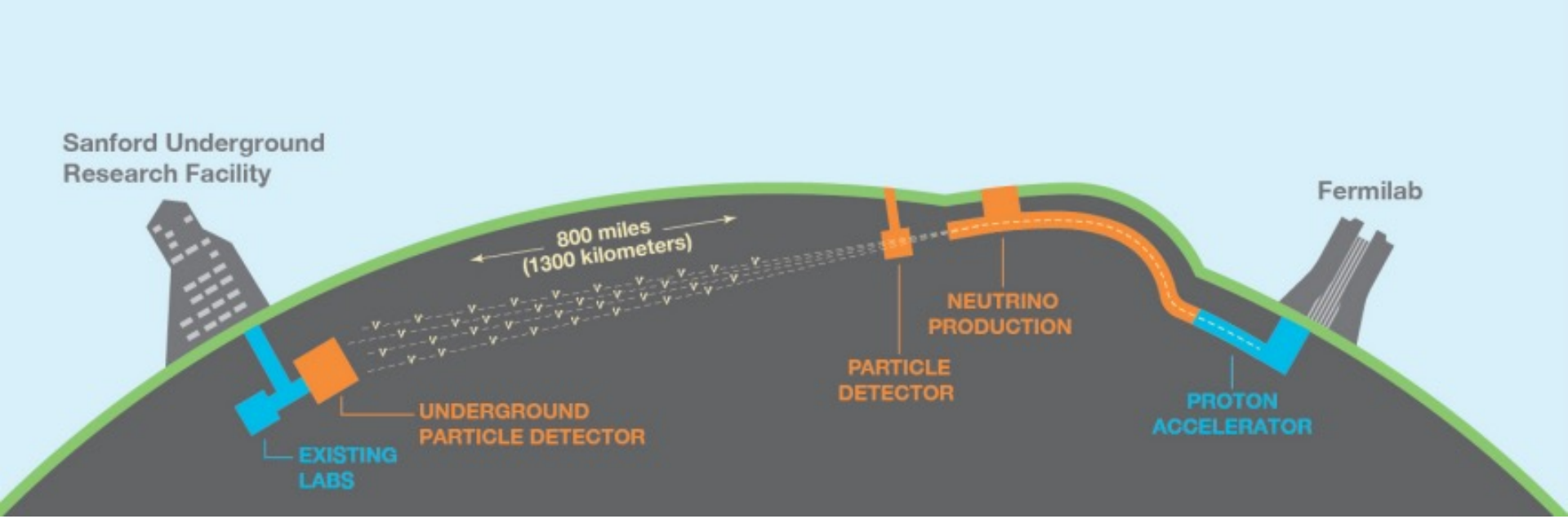


FD1 TPC Electronics Final Review Documentation:

The first two documents are good starting point for the reviewers to jump start on this document-based review.

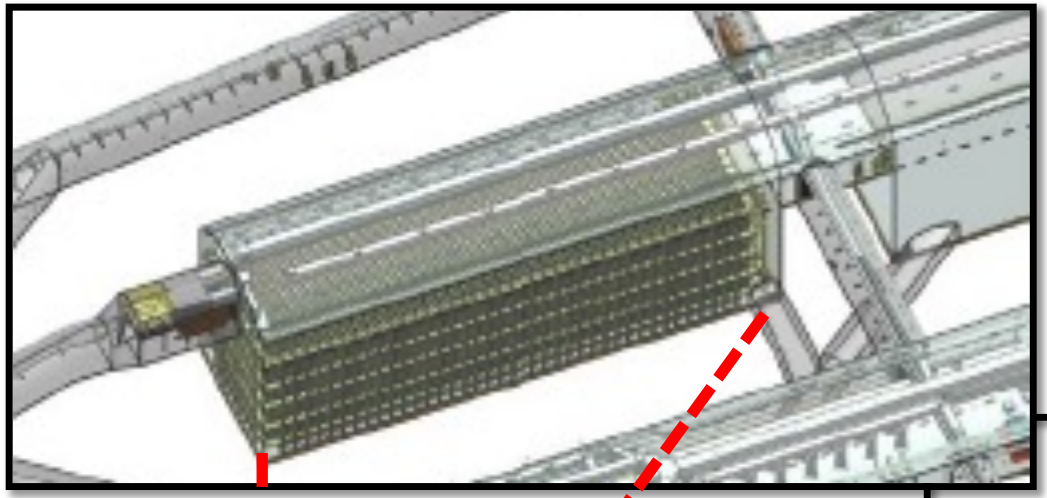
- **FD1 TDR Chapter on TPC Electronics** (https://edms.cern.ch/document/2606690): This TDR chapter has been extensively updated for the review. It's a good place for people to read about the full TPC electronics system and scope.
- **FDR support document** (https://edms.cern.ch/document/2782297): This document describes the design evolution (e.g. differences between PDR and FDR design), performance results, and QA/QC plan.
- **Complete list of the review documentation** is provided in the excel file in EDMS#2783308. Instructions on how to navigate the spreadsheet is given in the presentation ***Documentation For The Review.***

Deep Underground Neutrino Experiment (DUNE)



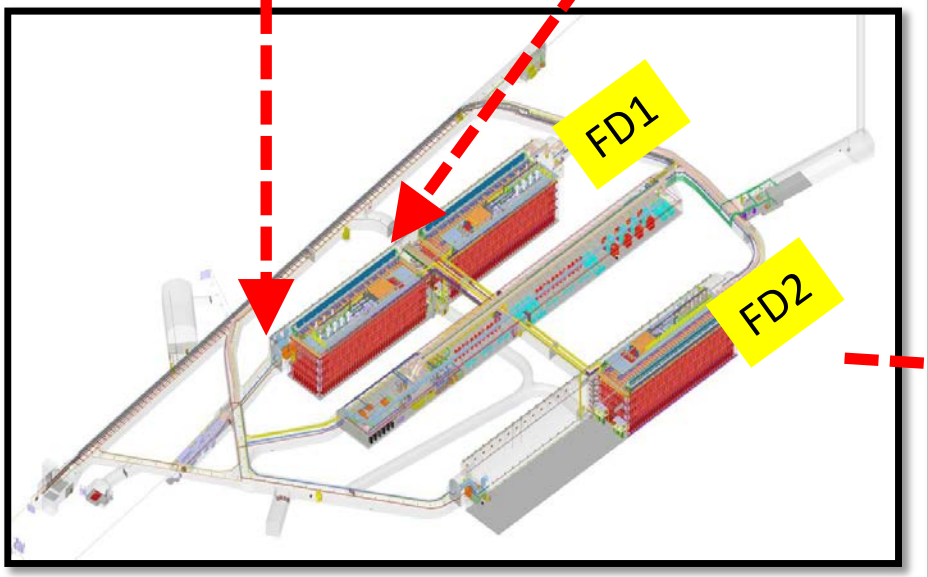
- Future flagship neutrino oscillation experiment
- Three major components: neutrino beamline, near detector, and liquid Argon far detector modules
- Broad physics program: BSM studies supernovae, solar neutrinos, three-flavor oscillation measurements
- >1300 people, > 200 institutions, 33 countries + CERN

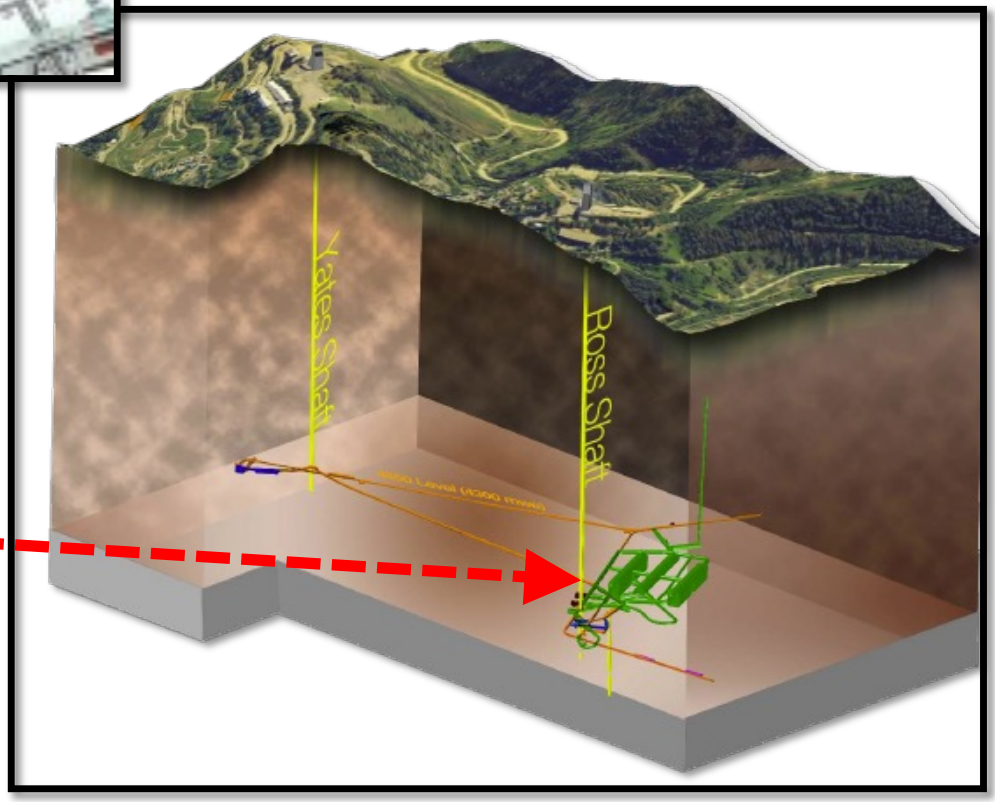
DUNE Far Detectors



Four 10-kTon (fiducial) liquid argon detectors

~1500m underground





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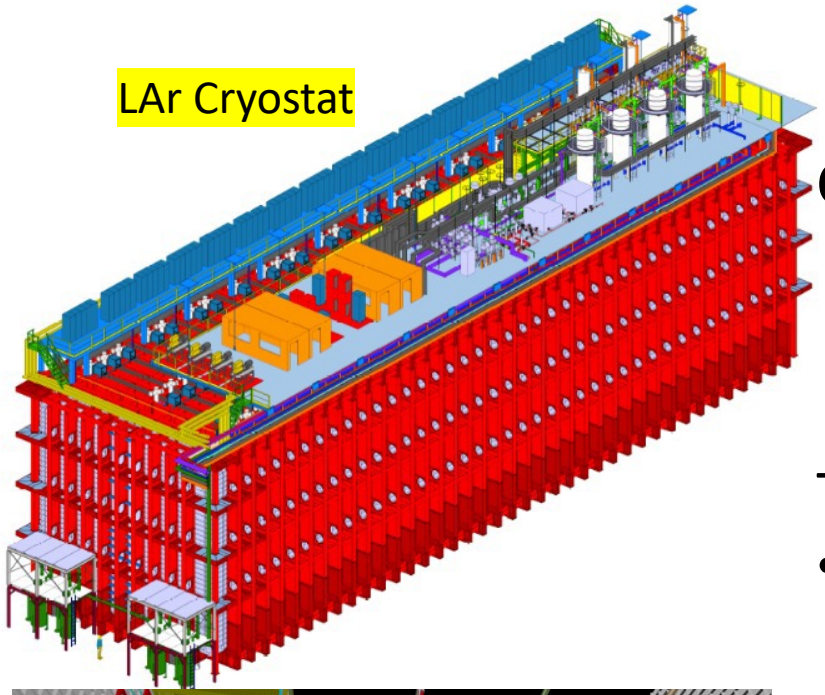
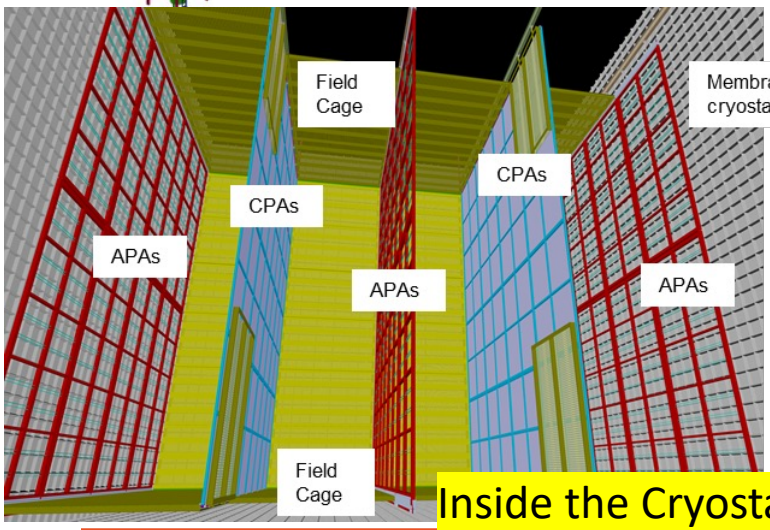
DUNE Far Detector #1



LAr Cryostat

Cryostat dimensions:

~65m (L) x 19m (W) x 18m (H)

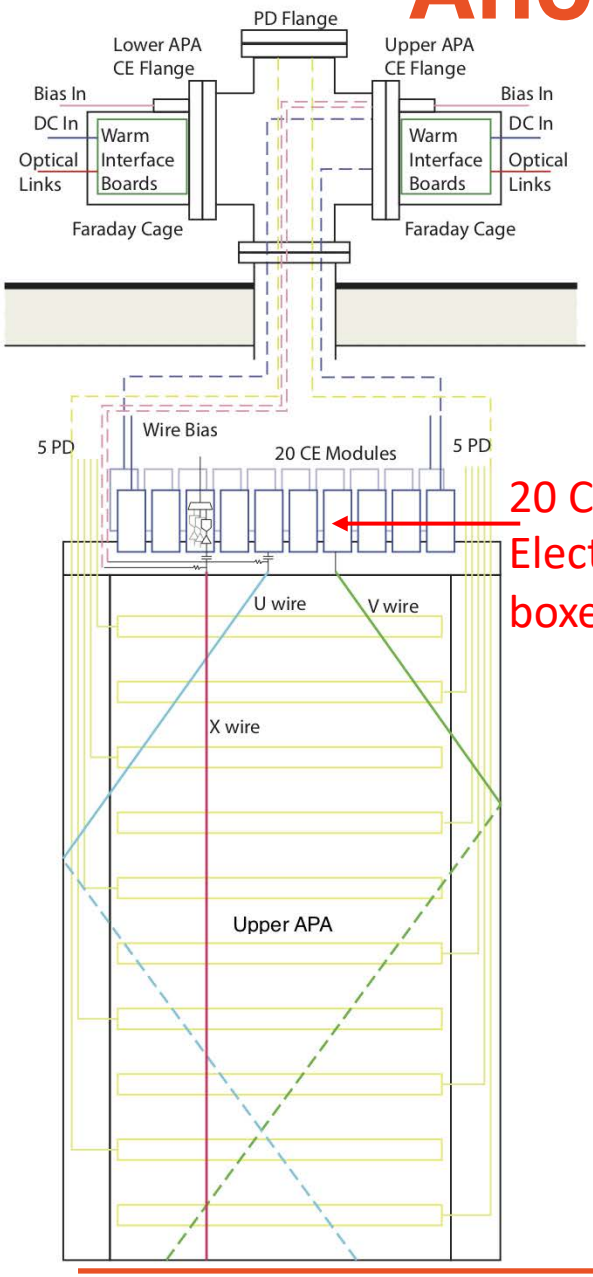


Inside the Cryostat

Time Projection Chamber (TPC) Elements:

- Anode Plane Assembly (APA). Sense wires for detecting drift electrons in the TPC
- Cathode Plane Assembly (CPA) at -180kV. Electron drift field of 500V/cm
- Distance between CPA and APA plane = 3.5m (maximum electron drift distance)

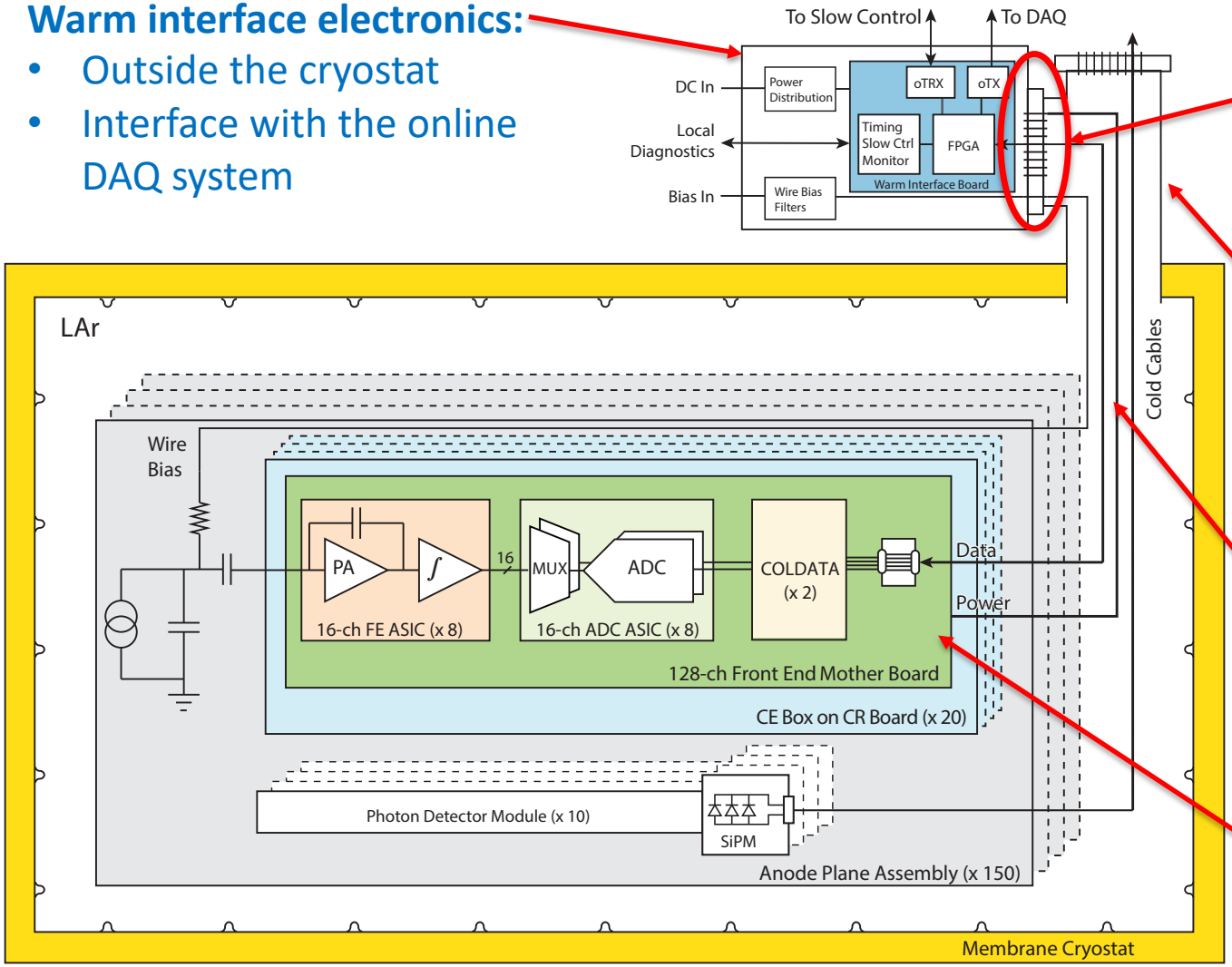
Anode Plane Assembly (APA)



- Far detector #1 has 150 APAs
- Each APA has four wire planes:
  - 960 grid wires (un-instrumented)
  - 800 U (1st induction wires)
  - 800 V (2nd induction wires)
  - 960 X (collection wires)
- Readout electronics are integrated close to the sense wires on the APA and immersed in LAr to yield the best SNR → Cold Electronics
- 20 Cold Electronic (CE) Boxes are mounted on the top of each APA and connected to 2560 sense wires

TPC Readout Electronics

Warm interface electronics:
- Outside the cryostat
- Interface with the online DAQ system



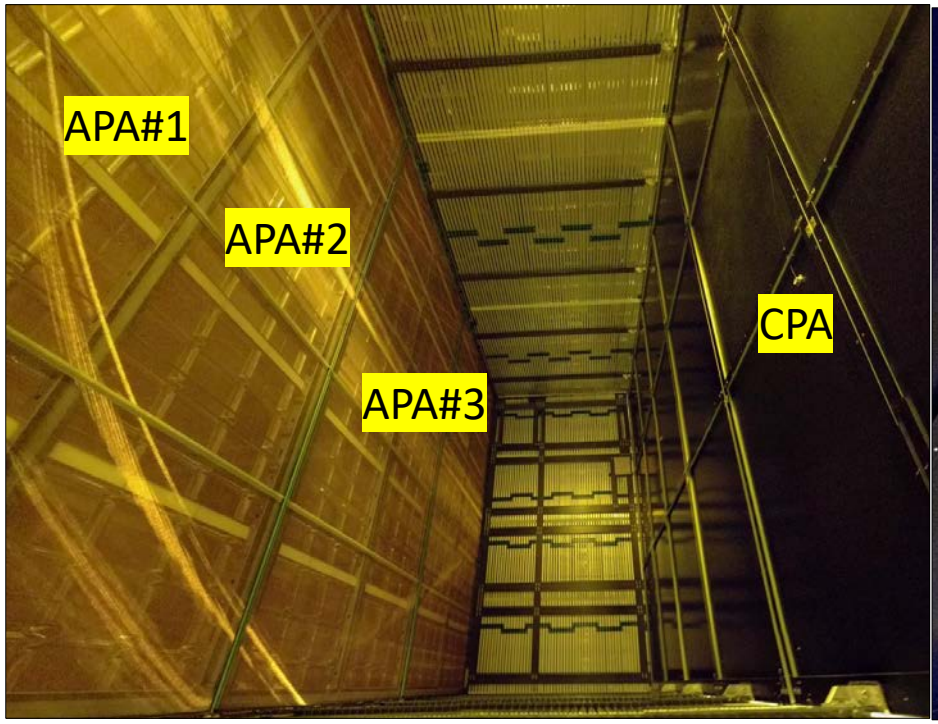
CE Flange:
- On top of the cryostat
- Connect cold cables to the Warm Interface Electronics

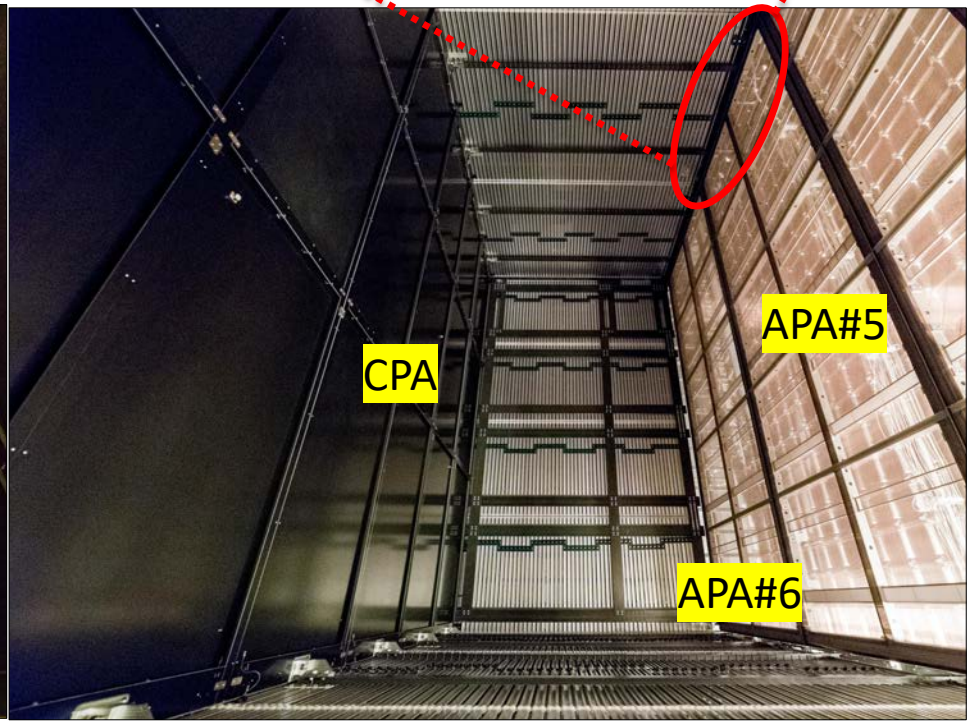
Signal feedthrough:
- 14” conflat
- Cable strain relief

Cold cables: Low voltage and data cable to Frontend motherboard

Frontend Motherboard (FEMB): 128 channels of digitized wire readout enclosed in CE box

ProtoDUNE-1 operated in LAr for about 2 years





Beam-Right TPC Volume

Beam-LEFT TPC Volume

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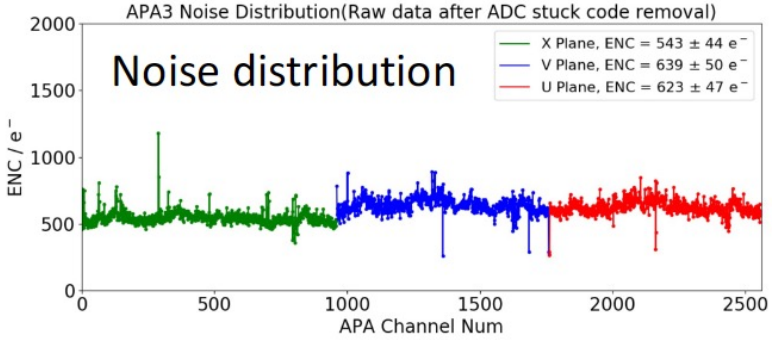
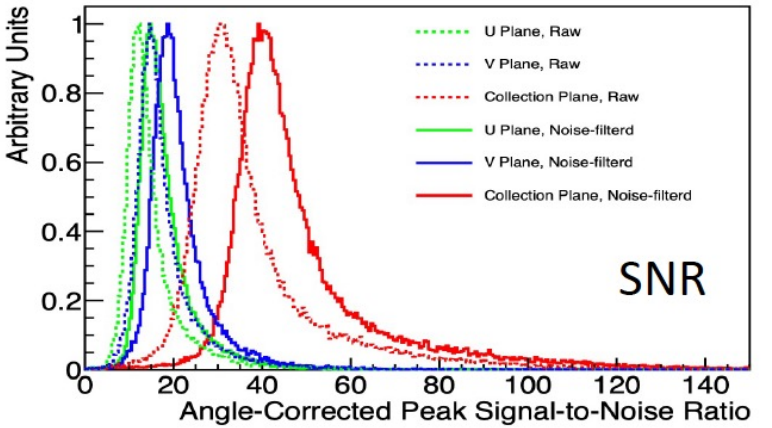
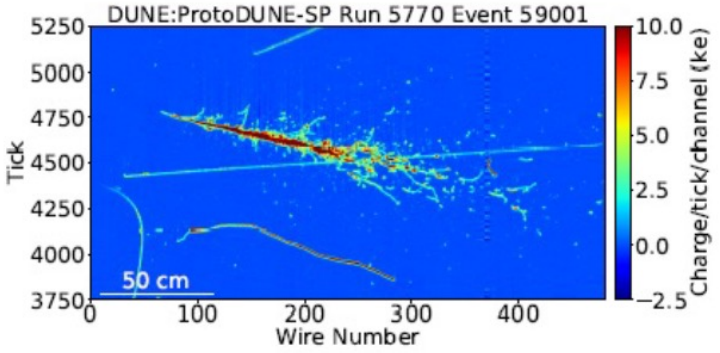
DUNE

ProtoDUNE Run-1 Performance

- **High yield**
  - 99.74% (15320 of 15360) of TPC channels are active
    - Only 4 inactive cold electronics channels when commissioning started
    - 2 more inactive cold electronics after >1 year running
- **Low noise**
  - 92.83% TPC channels are good with excellent noise performance
    - Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-
- **Good stability**
  - No measurable degradation is observed over a year
- CE is demonstrated as the promising technology towards DUNE LArTPC







A 6 GeV/c electron candidate

TPC Electronics Design Review History

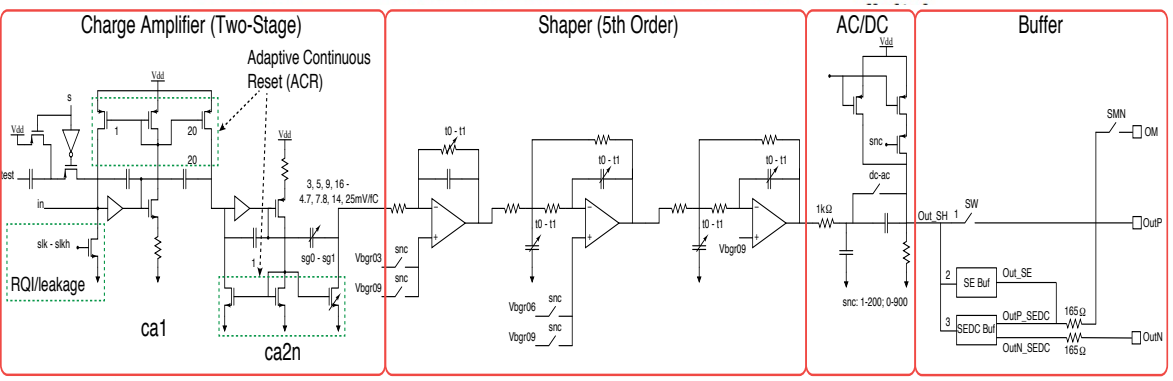
- All subsystems have gone through Preliminary Design Review
  - Mechanical structure PDR (11-12 Feb 2019)
  - ASICs and FEMB PDR (5-7 Feb 2020)
  - Warm Electronics PDR (17-March to 7-Apr 2020)
- All three custom ASICs (LArASIC, ColdADC, COLDATA) have gone through Final Design Review (21-22 Jul 2021)
- LArASIC has gone through Production Readiness Review (7-8 Mar 2022)
- For this FDR, we are reviewing everything except the ASICs

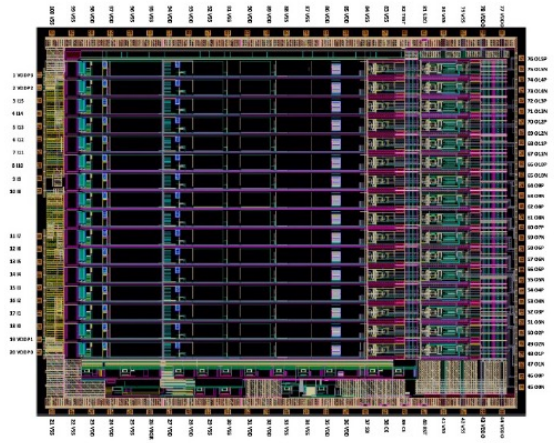
(Note: click on the review dates to link to the review page)

LArASIC ASIC

16-ch programmable charge amplifier working at 77-300K for neutrino experiments

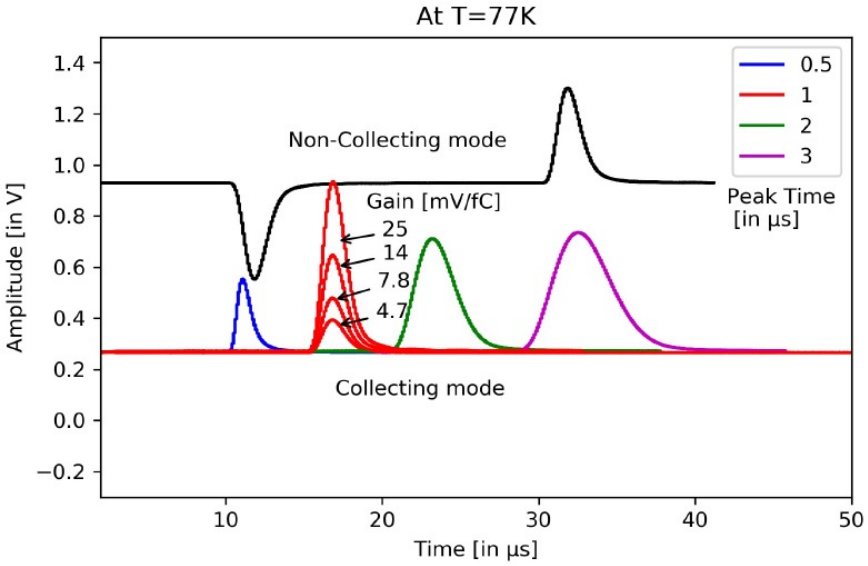
Block Diagram





Key Features

- Two-stage charge amplifier, high-order filter (5th)
- Adjustable reset quiescent current settings
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC
- Adjustable peaking time: 0.5, 1, 2, 3 µs
- Selectable collection/non-collection mode
- Rail-to-rail analog signal processing
- Bandgap referenced (BGR) biasing circuits
- Integrated temperature sensor
- Integrated 6-bit adjustable range pulse generator
- SPI interface for 144 configuration registers
- Technology CMOS 0.18 µm, 1.8V
- Leverages the existing cold models



Measured waveforms at cold

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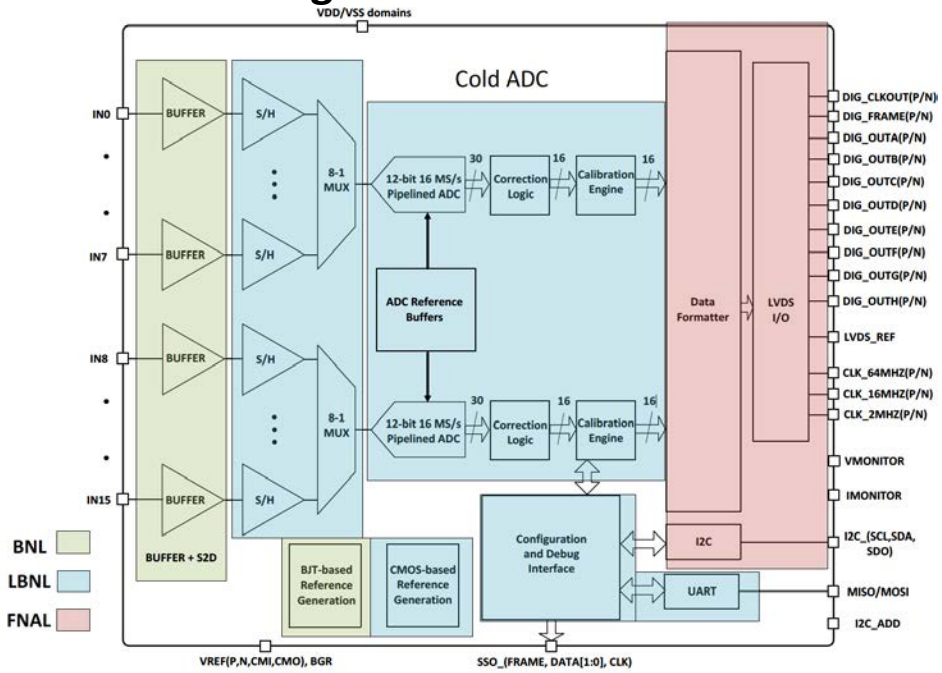
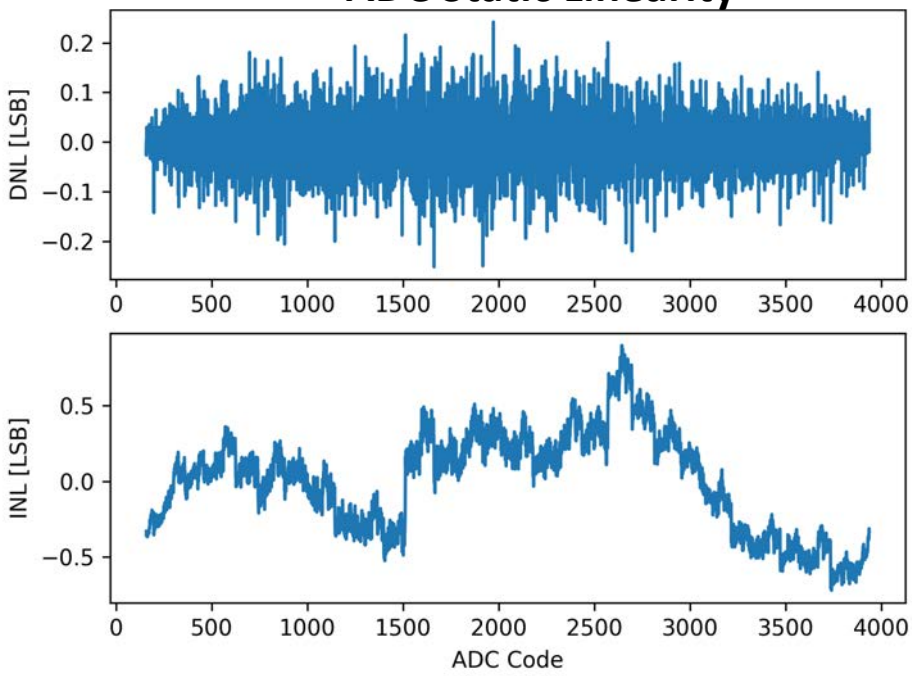
ColdADC ASIC

ADC Block Diagram



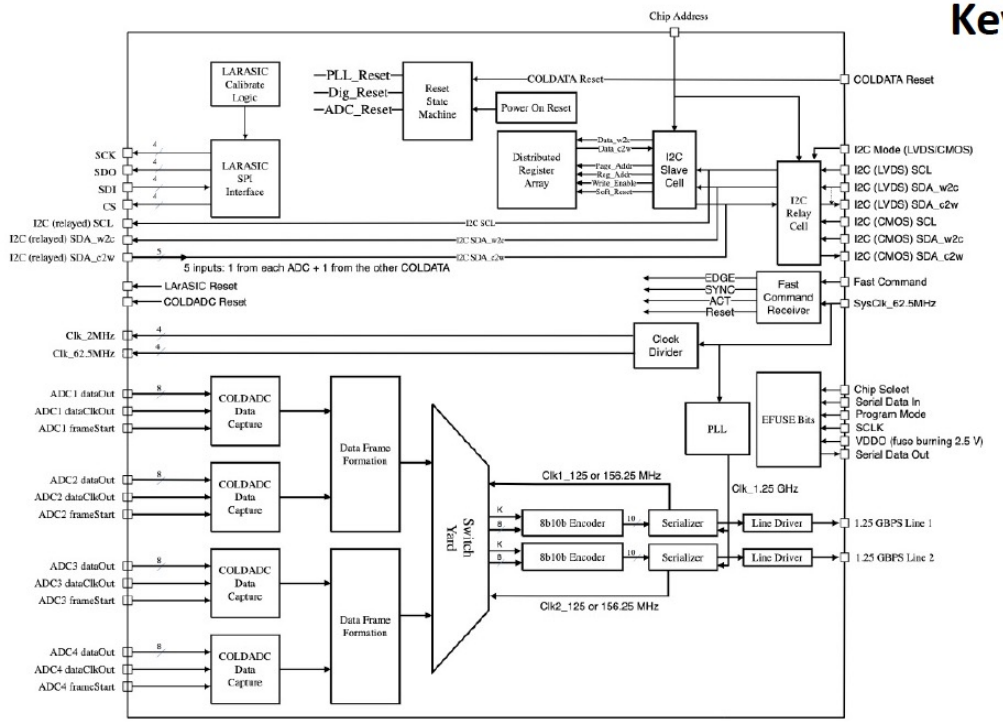
ADC Static Linearity



Key Features

- 16-channel, 14-bit 2MS/s digitizer ASIC for 77-89K
- Two 15-stage piped-line ADCs
- Low-noise and long lifetime operation in LAr
- 65nm CMOS process, 9 metal stack
- Digital self-calibration for interstage gains
- Chip size: 6860 μm x 7610 μm

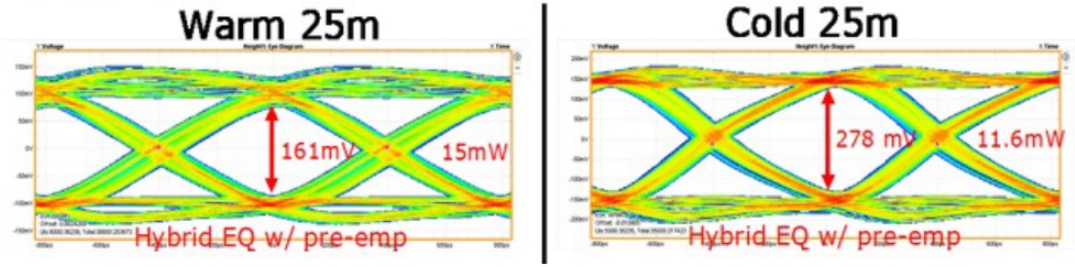
COLDATA ASIC



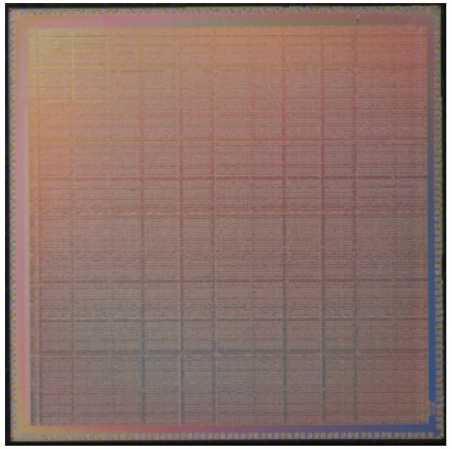
Key Features

- Design for cryogenic, long lifetime operation
- Control 4 ColdADCs and 4 LArASICs
- Accept data from 4 ColdADCs
- Format ADC data (truncate to **12 or 14** bits) & pack into an array of 8-bit words
- Combine packed arrays from pairs of ADCs into 2 output data frames
- Encode the output data using 8b10b
- Drive the output data to a WIB at 1.25 Gb/s
- Digital-On-Top design methodology
- 65nm CMOS process, 9 metal stack
- Chip size: 7730 µm x 7730 µm
- Leverages the existing cold models

BER < 10^{-15}

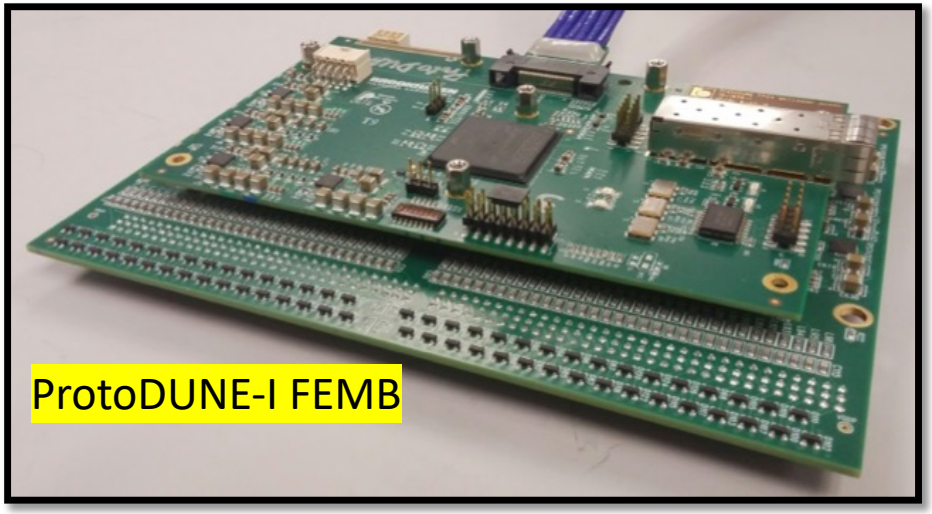


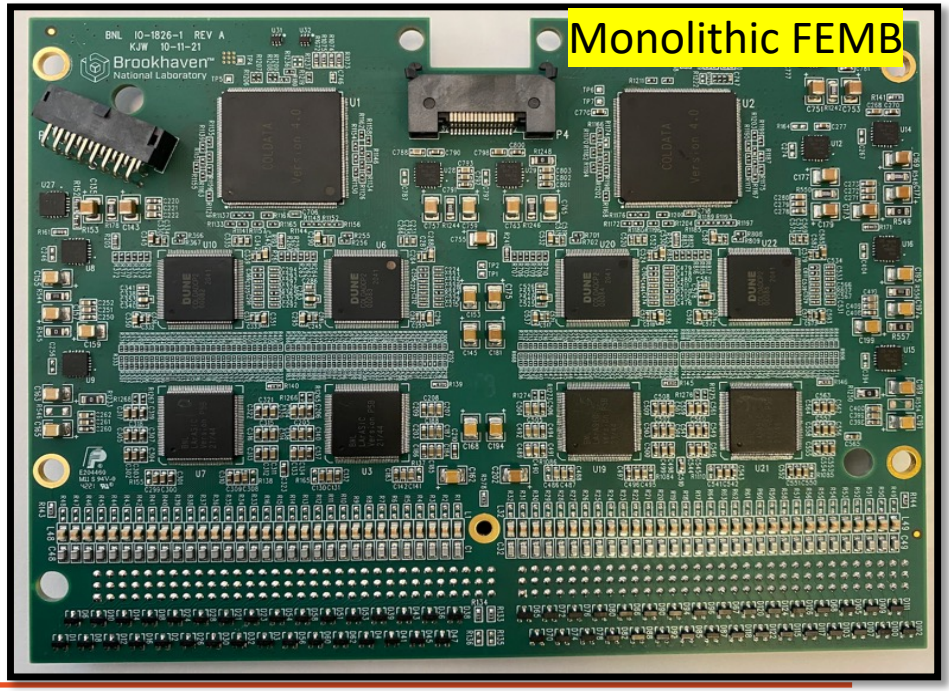
Line driver eye diagram measurement result

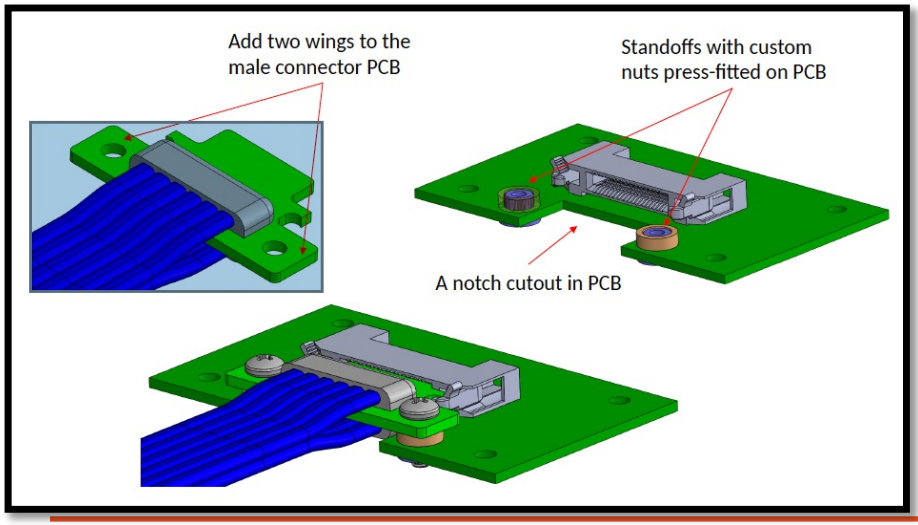


Monolithic FEMB

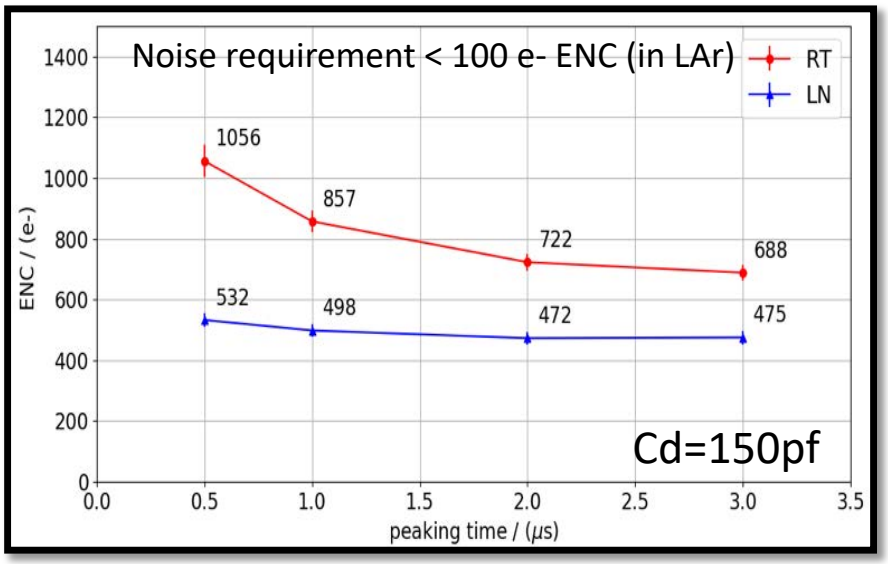
- ProtoDUNE-I FEMB uses previous generation of LArASIC, ADCs and a commercial FPGA on a mezzanine card
- ProtoDUNE-II FEMB uses final custom ASICs on a single PCB (monolithic FEMB)
- Many other changes and improvements. See EDMS#2782297 for the complete list
- Analog monitoring of channel response, bandgap reference, temperature, ColdADC reference voltages, etc.
- Improved SAMTEC cable connection based on ProtoDUNE-I lessons-learned

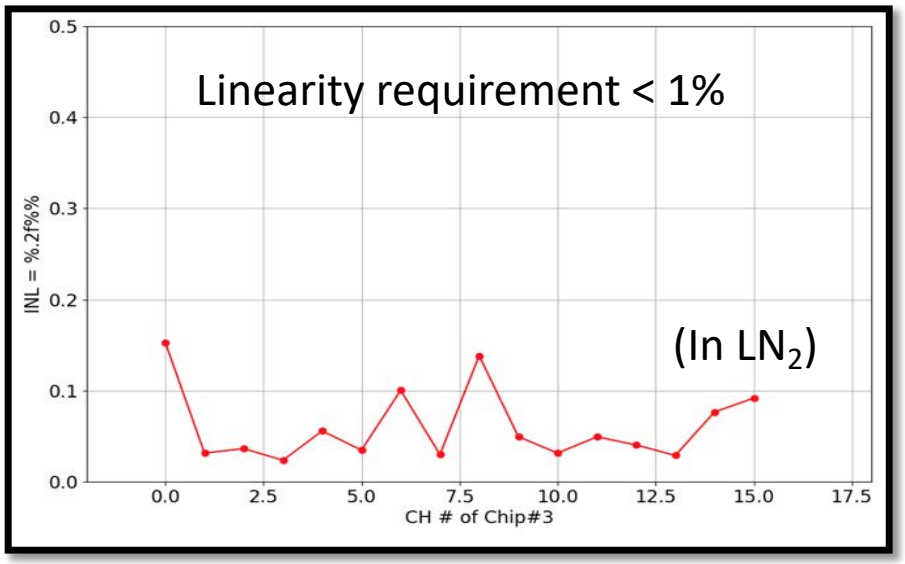


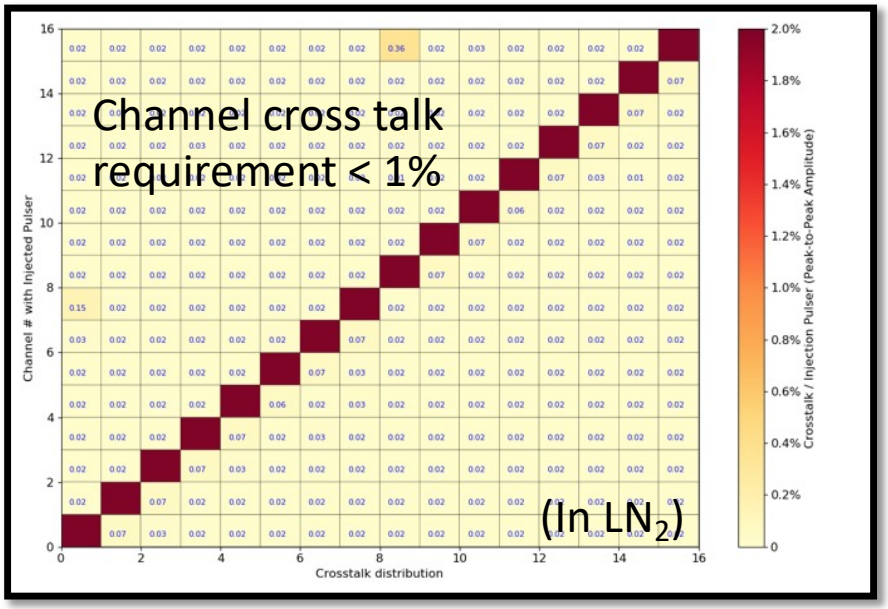




Benchtop Performance of Monolithic FEMB

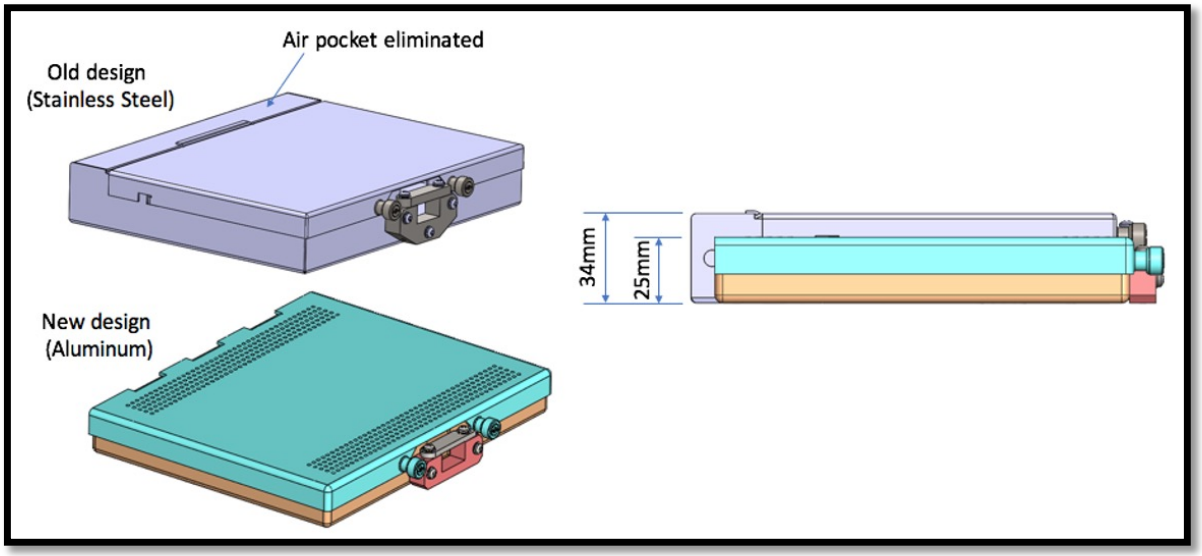


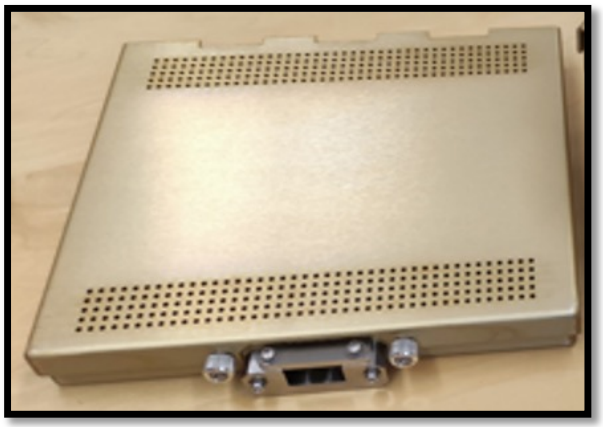




- Performance of monolithic FEMB well exceeds DUNE requirements
- Detailed FEMB QA/QC procedure in the documentation (EDMS#2782297)

New CE Box Design

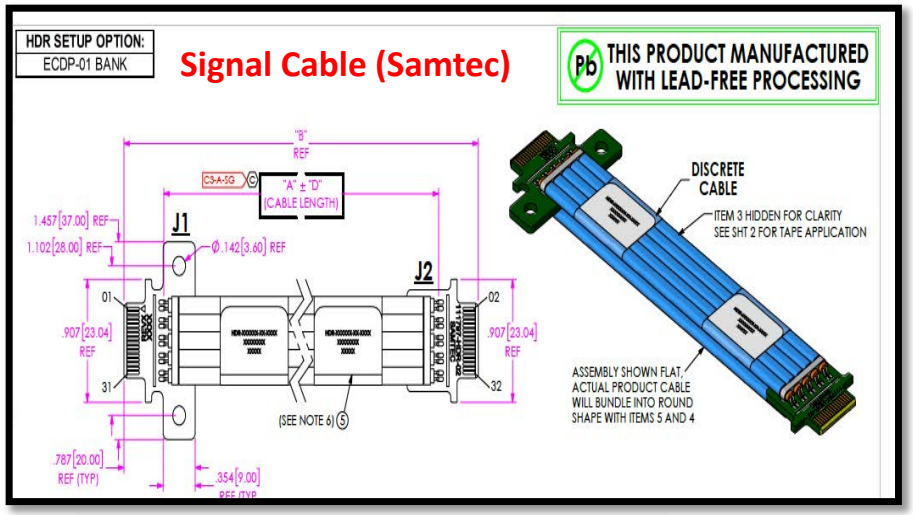




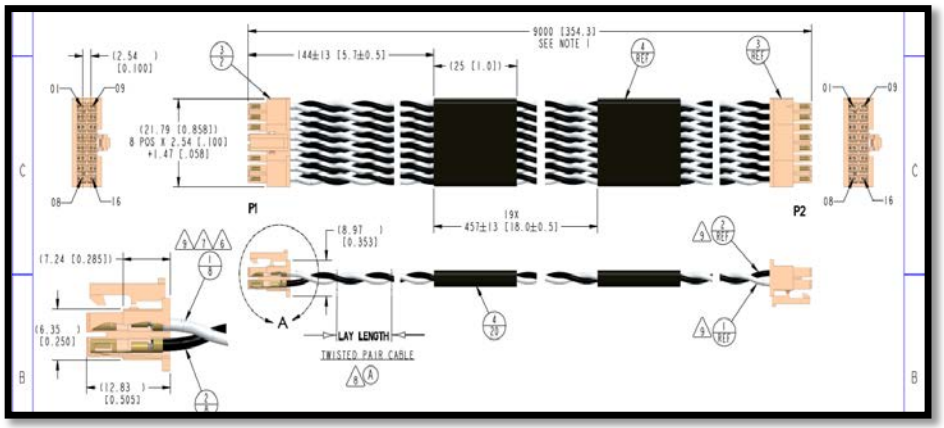
- Thinner enclosure box for the monolithic FEMB
- Change material from stainless steel to aluminum to reduce weight (~50% lighter). This change is important for FD2 since CE boxes mounted on the CRPs introduce significant stress on the structure of the CRP composite frame
- Same enclosure design is compatible for FD1 APA and FD2 CRP mounts

Cold Cables and Strain Relief

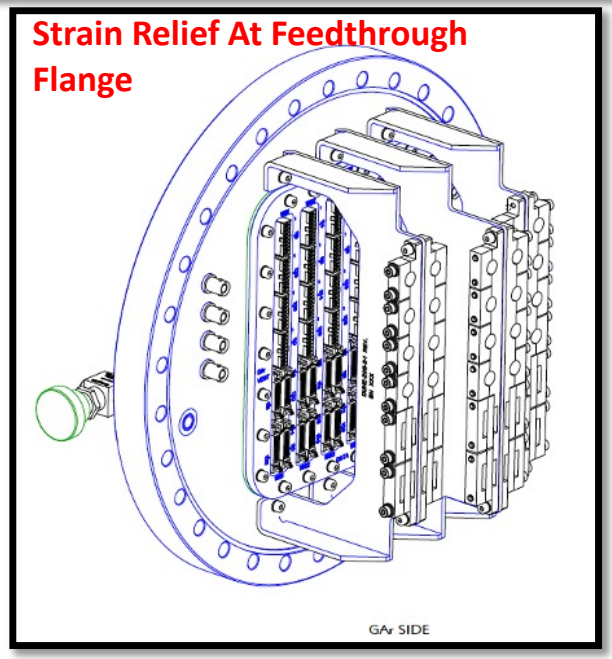
Signal Cable (Samtec)



Low Voltage Power Cable

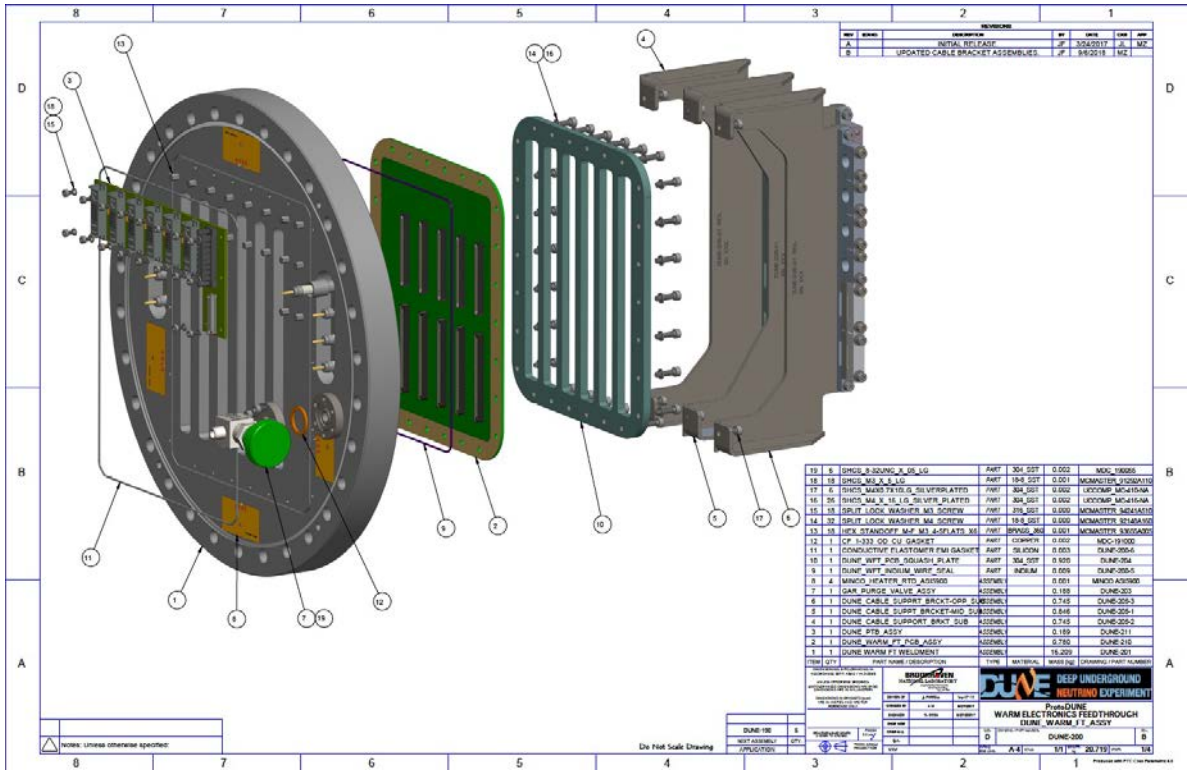


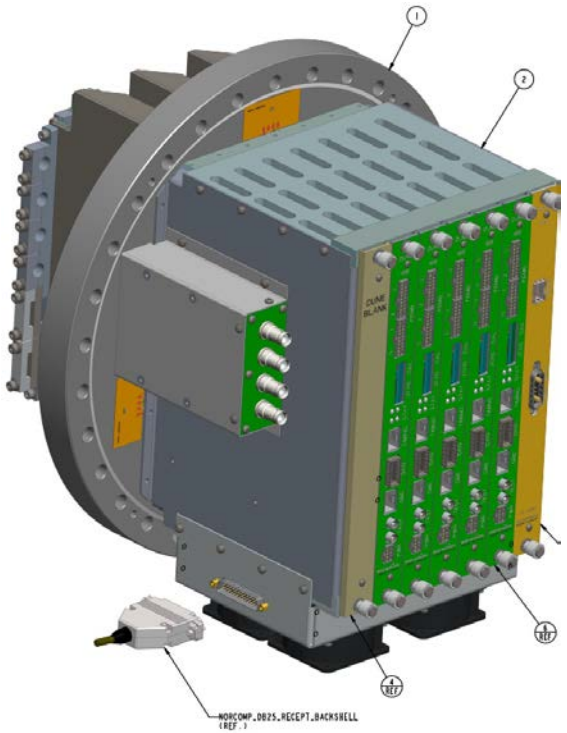
Strain Relief At Feedthrough Flange



- Fewer conductors needed for the monolithic FEMB:
  - Signal cable 12 → 10 twinax pairs
  - Power cable 9 → 8 twisted pairs
- FD1 needs 9m and 22m lengths. Will use the same length in ProtoDUNE-II
- Flange cable strain relief modified to accommodate the thinner cables

Warm Interface Electronic Crate (WIEC)



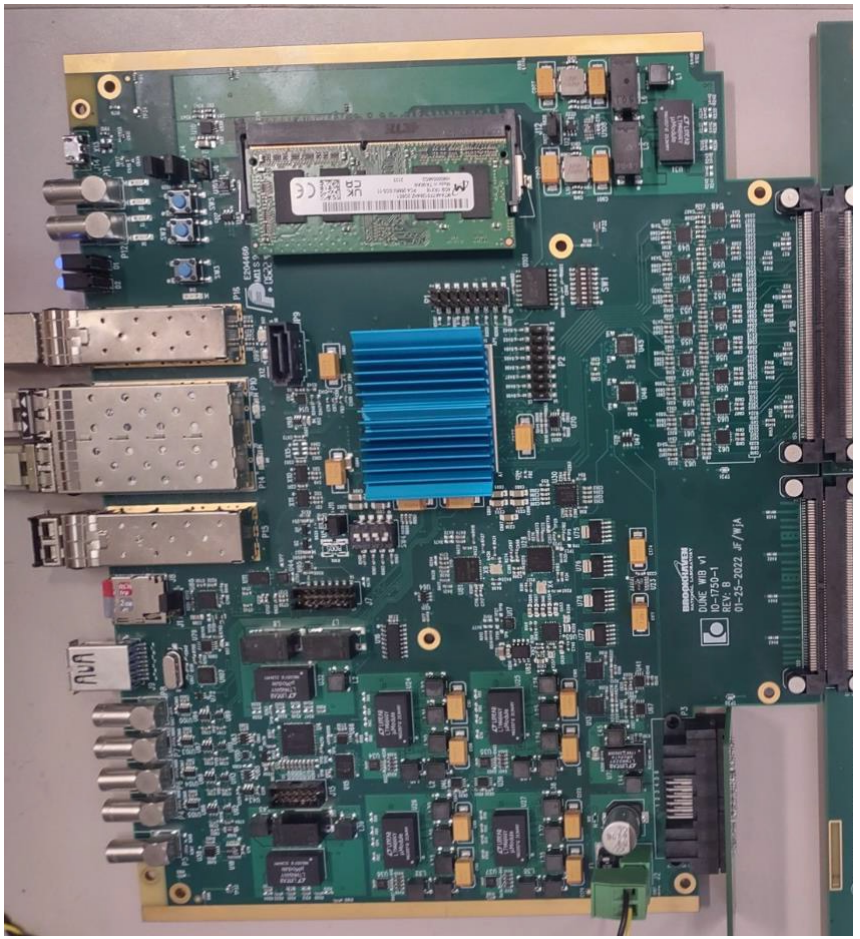


- WIEC design is largely the same as ProtoDUNE-I
- New flange board design to accommodate the new cold cables
- New PTB backplane to accommodate future PTC upgrade
- Filter box for APA wire bias voltages, FC termination, and ground plane monitor

Warm Interface Board (WIB)

- New WIB design for ProtoDUNE-II
- Replaced Arria V FPGA with Xilinx Zynq UltraScale+ MPSoC FPGA
- FEMB power scheme modified
- QSFP replaced with dual SFP
- Direct path from CDR clock to FPGA
- 16-bit DAC for calibration pulse injection to the FEMBs
- New firmware written for the FPGA
- + many other improvements
- A number of system integration tests: test-stand at BNL, ICEBERG at Fermilab, Vertical Slice Test-stand at CERN, and APA Cold Box at CERN

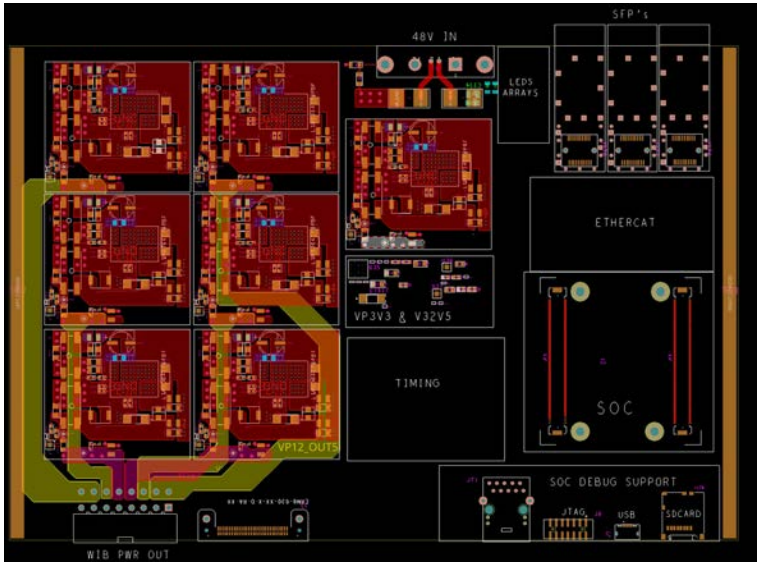
ProtoDUNE-II WIB (v3)



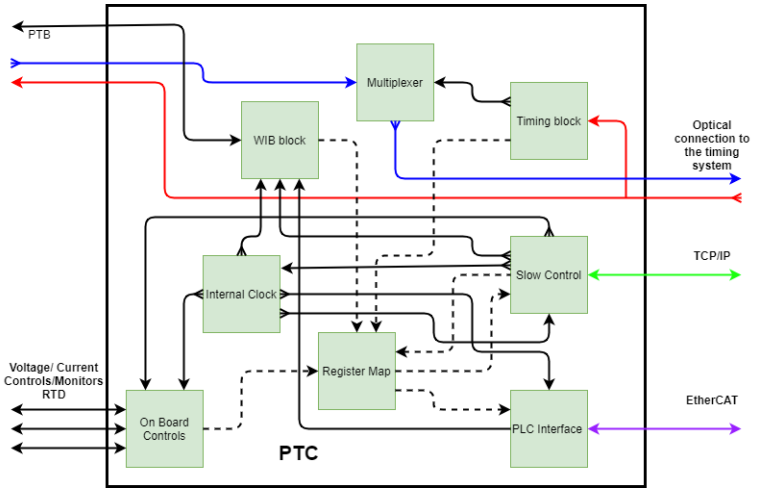
Power & Timing Card (PTC)

- ProtoDUNE-I PTC meets all DUNE requirements
- Same PTC is being used for ProtoDUNE-II
- Existing PTC simply fanout the DUNE timing signal and power to the WIBs
- New PTC is not needed for DUNE, but we are planning an upgrade now to increase the functionality of PTC
- Adding an FPGA to the PTC so it can communicate with Slow Control and DUNE Detector Safety System
- Current status: schematic design is completed, layout is about 20% complete
- Expect prototype PTCs to be available in early 2023
- Plan to integrate it for VD module-0

Layout of New PTC



Firmware Block



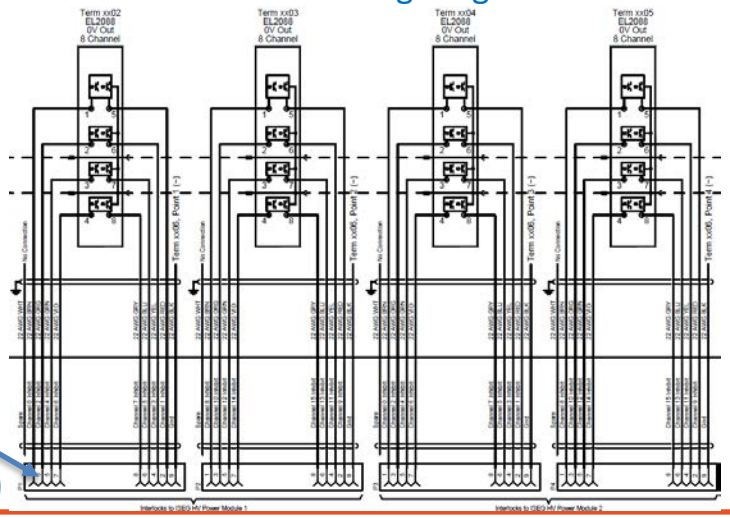
CE Hardware Interlock

- Using commercial Beckhoff PLC for hardware interlock for the fans, RTDs, HV bias, and low voltage power supplies
- Design is completed. See EDMS#2401090 for design detail, parts list, action matrix, power analysis, etc.
- Components for the prototype systems have been purchased
- Plan to first integrate the system at the ICEBERG test-stand at Fermilab
- Depending on the time scale, could also integrate the interlock in VD module-0 at CERN

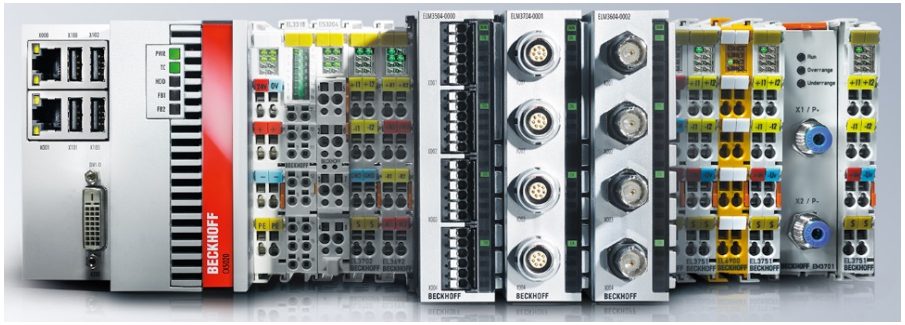
Bias HV Racks Wiring Diagram

9 Instances per rack (45 total)

ISEG Interlocks (16 channels)



Beckhoff Modules



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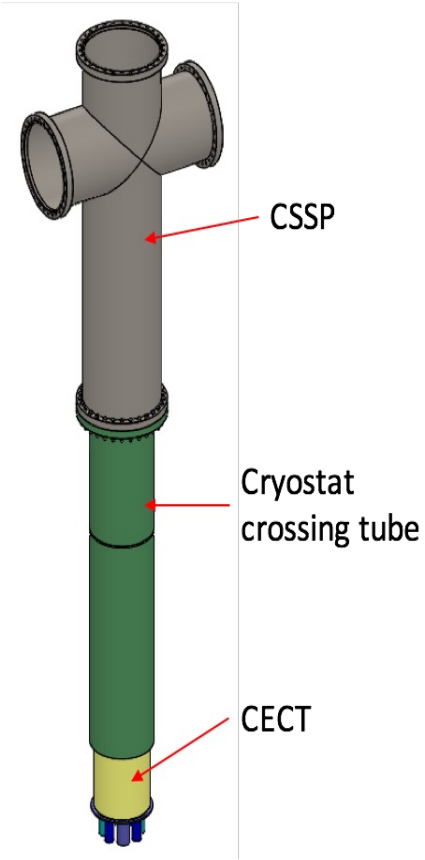
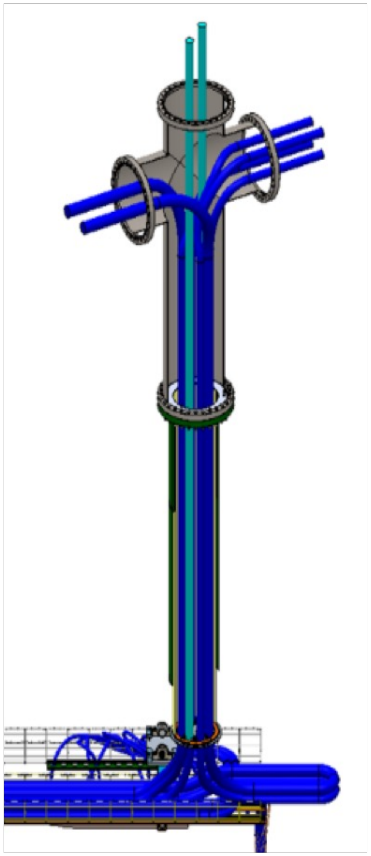
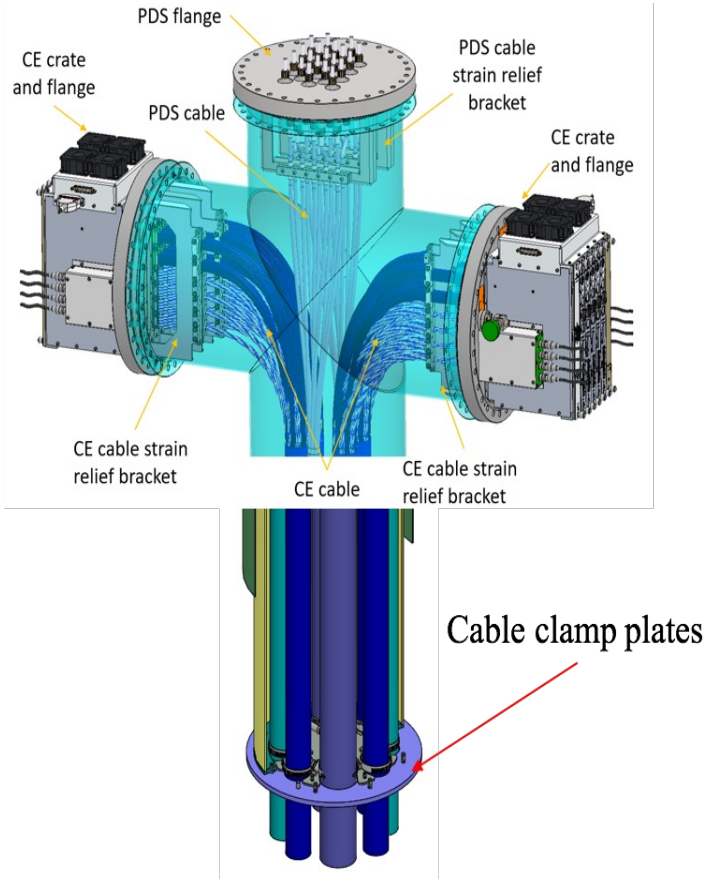
CE Cryostat Penetration and Cable Clamping Plate



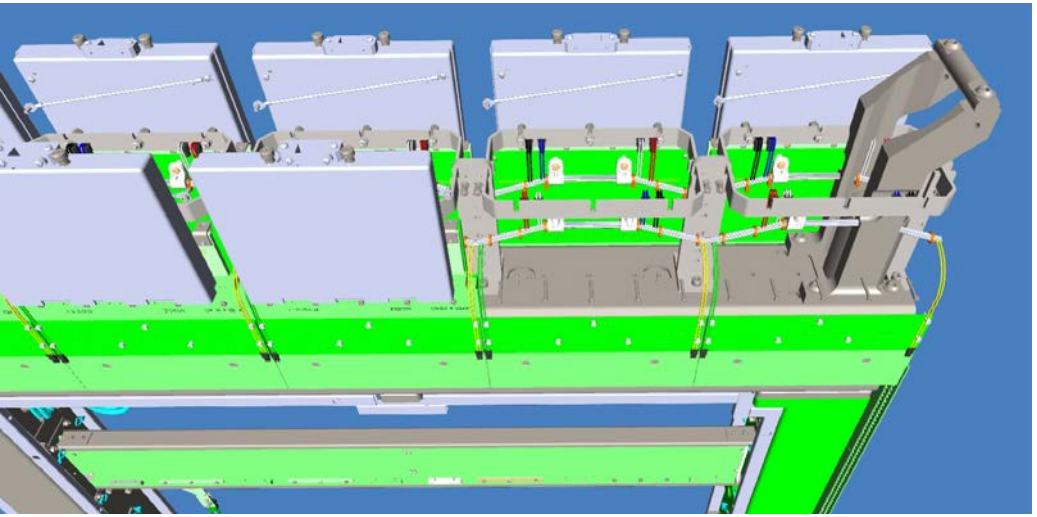




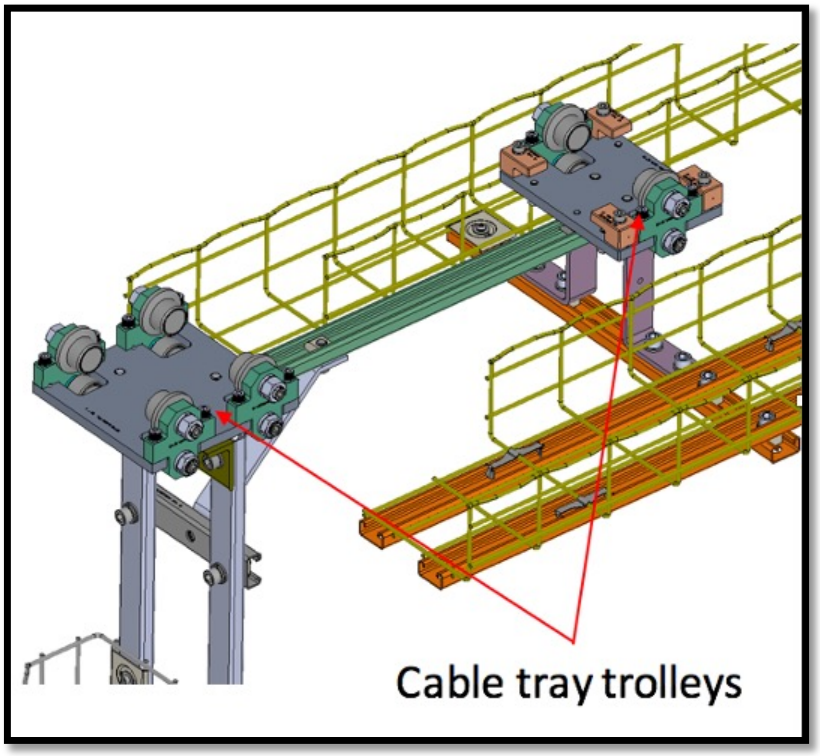
- ProtoDUNE-I design had 1 WIEC per penetration
- ProtoDUNE-II is using the same design as FD1

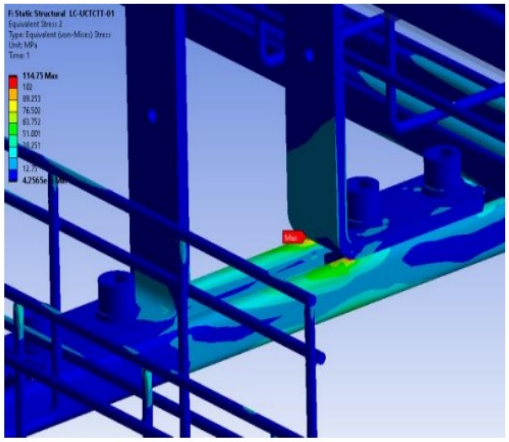
Mechanical Support Inside the Cryostat

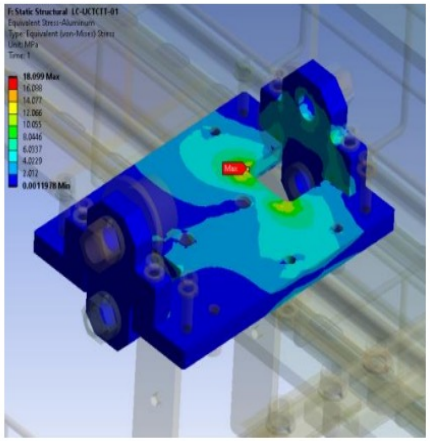
CE Box Mounting Hardware



Cable Tray Supported by DSS Beam







- Detailed structural analysis have been performed
- Compliance Office has signed off on the studies:
  - EDMS#2570048: analysis plan and results
  - EDMS#2780876: CO report

Answer to Charge Questions

- Detailed information addressing the charge questions are in the list of review documentation
- Charge # 1: Has the TPC consortium responded appropriately to recommendations from past reviews?
  - ✓ We believe we have. See the report from Technical Coordination and Review Office
- Charge #2: Are the full specifications, the design files and complete documentation of all the components of the TPC Electronics system available in EDMS?
  - ✓ We have uploaded the requirement and specification documents to EDMS
  - ✓ 3-D CAD models, parts drawings, assembly drawings, schematics, PCB layout, BOM, etc. are available in EDMS
  - ✓ Index files are provided to help reviewer navigate through the maze of drawings
  - ✓ See TDR chapter and EDMS#2782297 for standalone test results

Answer to Charge Questions

- Charge #3: Do the standalone tests of the new generation of components indicate that the design goals have been achieved? Do these design goals meet the detector requirements? Have all issues observed in previous versions of the components been addressed? Do the performance measurements obtained from test-stands meet the expected performance?
  - ✓ All benchtop test results have shown that the new generation of components satisfy DUNE requirements and our expectations
  - ✓ Important lessons and problems from ProtoDUNE-I have been addressed (e.g. cable connector flaws, issues with ADC ASIC, etc.). These issues are discussed in more details in the ProtoDUNE-I lessons learned document

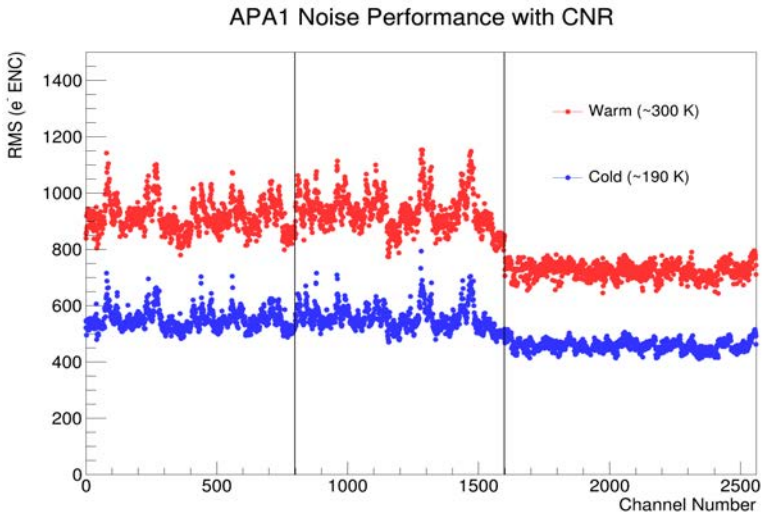
Answer to Charge Questions

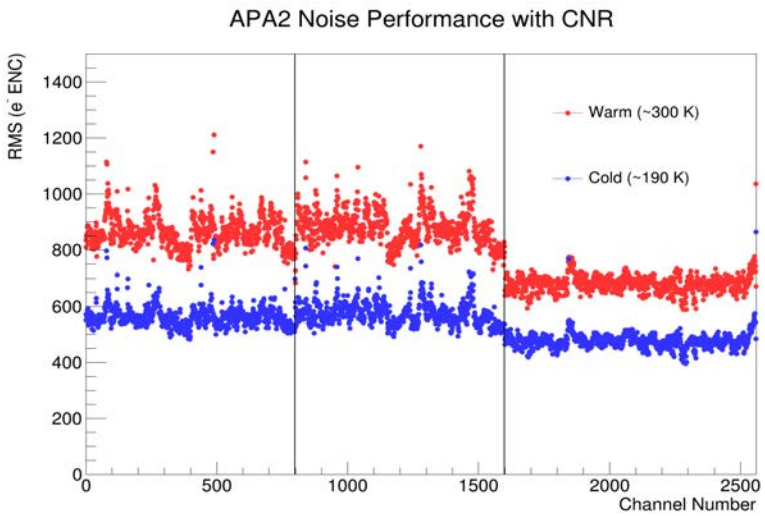
- Charge #4: What is the outcome of system tests? What are the plans and timeline for future tests?

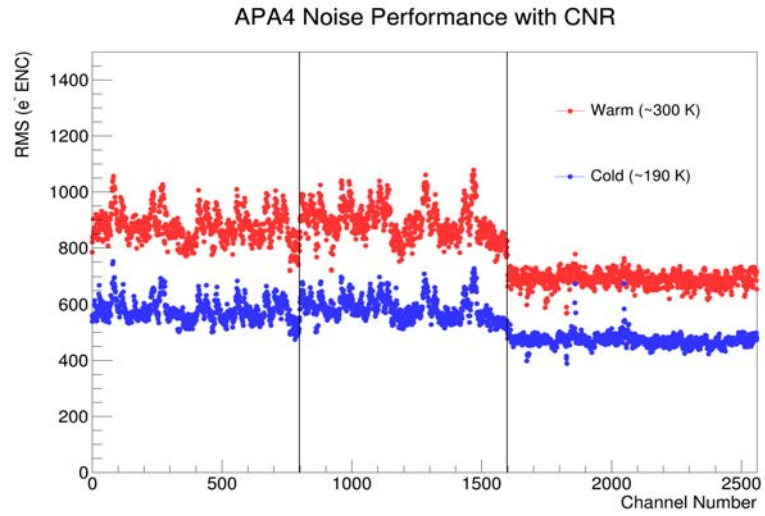
  - ✓ ProtoDUNE-II installation at CERN is ongoing. 3 out of 4 APAs have already been tested in the Cold Box with good performance. See EDMS#2782614
  - ✓ Installation of the APAs in NP04 cryostat will start soon. Expect the installation to be completed by November 2022
  - ✓ Due to LAr shortage in Europe. Testing in LAr and in beam will likely happen in the second half of 2023
  - ✓ Same electronics will also be used in FD2 tests as well:
    - ❖ CRP5A test (12 FEMBs) in LN2 next month at BNL
    - ❖ CRP4 (24 FEMBs) in LAr at CERN cold box
    - ❖ Module-0 installation early next year

Answer to Charge Questions

- Charge #4: What is the outcome of system tests? What are the plans and timeline for future tests?







- ProtoDUNE-II cold box results
- FEMB configuration: 2us shaping time; 14 mV/fC gain, single-ended input
- Noise performance exceeds DUNE requirements of < 1000 e- ENC in LAr

Answer to Charge Questions

- Charge #5: Are there any issues with the design of the TPC Electronics system that will complicate the procurement strategy and manufacturing plans for the different components

  - ✓ The main issue for us is the supply chain problem. Many of the components for our system have very long lead time (~> 1 year)
  - ✓ To mitigate this risk, we are procuring most of the components early under CD-3a (long lead procurement) cope
  - ✓ FD1 CD-3a scope:
    - ❖ All three ASICs
    - ❖ All FPGAs for the WIBs and PTCs
    - ❖ All discrete components for the FEMBs
    - ❖ 50% of the discrete components for the WIBs
    - ❖ 50% of the discrete components for the PTCs

Answer to Charge Questions

- Charge #6: Is the QA/QC plan complete and documented? Have sufficient resources been allocated to successfully execute the QA/QC plan?

  - ✓ QA/QC plans are discussed in a number of documents. See the document spreadsheet
  - ✓ We have met with PIs from university groups to discuss QC contributions. At the moment we have 3 national labs and 7 university groups committed to QC testing. All QC testing needs have an institution assigned
  - ✓ In P6, we have allocated budget for QC testing equipment, engineering and technician supports. In addition, we have contingency in the schedule and risk registry to provide more funding support if needed

Answer to Charge Questions

- Charge #7: Is the probability that tests not yet performed or not yet fully understood may require a further design iteration negligible? Is the TPC electronics consortium ready for launching the preproduction of the components?

  - ✓ We learned a lot from the prototype electronics with > 2 years of operational experience from ProtoDUNE-I
  - ✓ Recent ProtoDUNE-II cold box test results have given us confidence that we have a system that meet the DUNE requirements. It is unlikely that we will need any significant revision on the components
  - ✓ Fabrication of components for ProtoDUNE-II is ~ our preproduction run. In combination with FD2, we'll have more preproduction experiences

Answer to Charge Questions

- Charge #8: Are the Parts Breakdown structure, interfaces with other detector components, cost estimates, and schedule fully documented?

  ✓ Yes, see review documentation list for more information

  ✓ Please reach out if more detail is needed

Summary

- Since this is supposed to be a document-based review, the presentation is not exhaustive. I selectively picked a few highlights to discuss. More information is in the documentation
- Preliminary results from ProtoDUNE-II is very encouraging. So far the performance of the system has met or exceed our expectations
- If you have trouble finding documents or need other info, feel free to contact us
- Let us know if we should meet again tomorrow
- A very big thank you!!!!