List of question to the FD1 Cold Electronics System Team (v. 29-Oct-2022)

Questions related to grounding and shielding

1. Do you expect the metal box to provide shielding for the FEMB? If so, it maybe worth building a slightly thicker box. Effective shielding of 5 skin depths for Al is 2.9 mm @ 20Khz (one of the frequencies mentioned during review).

   The CE box serves two purposes, shielding and protection to ease the handling, with slightly more focus on the latter. The CE box is not designed to shield ~20 kHz noise observed during the CE/APA integration test, which needs further investigation to understand the cause.

2. The grounding document indicates several improvements for grounding the FEMB to the aluminum box and the aluminum box to the APA frame. When/where will these be tested.

   Approximately 10% of the APAs produced for DUNE will be tested at CERN in the NP04 cold box. We expect to do these tests at CERN in the NP04 cold box using APAs produced for DUNE. These tests are expected to start in January or February 2023.

3. In regard to the ~20KHz noise seen on the FEMB, have the all power rails been looked at and characterized?

   The power distribution from WIB to FEMB has been analyzed in detail. ~20 kHz is not observed with a standalone test setup including WIB + 4 FEMBs + Toy TPCs.

   There is a RC filter for the LArASIC powering. 4 LArASIC chips share a RC filter.
   R = 1 Ohm
   *C > 330uF * 10 + 22uF*(4+48) + (0.1uF*N) = 4444 uF*
   *RC time constant > 1 * 4444 = 4.4 ms*
   *Fc = 1/(2*pi*RC) < 36 Hz*
   At cold, C decreases significantly, to ~30% as at warm
   Fc(LN2) < 120 Hz which is significantly lower than 20kHz

   RC filter for ColdADC 2.25V
   *R = 0.1Ohm, C > 5*220uF + 22uF *M + 0.1uF*N*
   RC time constant > 110 us
   Fc < 1448 Hz, Fc(LN2) < 5 kHz

RC filter for ColdADC 1.10V
*R = 0.1Ohm, C > 5*220uF + 22uF *M + 0.1uF*N*
Fc < 1448Hz, Fc(LN2) < 5 kHz

RC filter for COLDATA VDDIO
*R = 0.1Ohm, C > 5*220uF + 22uF *M + 0.1uF*N*
Fc < 1448Hz, Fc(LN2) < 5 kHz

RC constant for COLDATA VDDA
*R = 0.1Ohm, C > 5*220uF + 22uF *M + 0.1uF*N*
Fc < 1448Hz, Fc(LN2) < 5 kHz

RC constant for COLDATA VDDCORE (1.1V)
*R = 0.1Ohm, C > 5*220uF + 22uF *M + 0.1uF*N*
Fc < 1448Hz, Fc(LN2) < 5 kHz

ESD comments/questions:

1. There is an extensive document written by DUNE QA team, but application of these principles should be found in specific procedures. Is there a procedure for handling/testing of the ASICs?

   Thanks to reviewers for this comment, a procedure for handling/testing of the ASICs will be prepared, taking into accounts various principles and recommendations from existing documents, including the items listed in questions 2) and 3) below. The production test of ASICs will be performed with the robotic test station, which helps minimize the handling required by humans. Nevertheless, a detailed procedure will be worked out in coordination of various ASIC test sites and specific environments before we complete the PRR for the FD1 TPC Electronics.

2. Should the use of anti-static gloves, lab coats, shoes and mats be specifically called out?
   Yes, please see answer 1). We will specify in the QC procedure document which ESD protection equipment is needed.

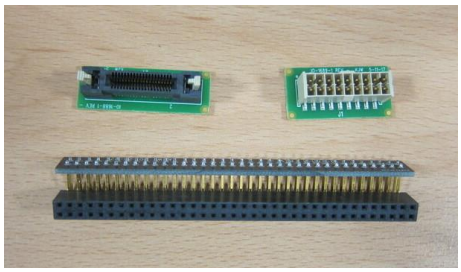
3. Do wrist straps warn user with sound/light should they become disconnected?
   Yes, please see answer 1). We will specify in the QC procedure document which ESD protection equipment is needed.

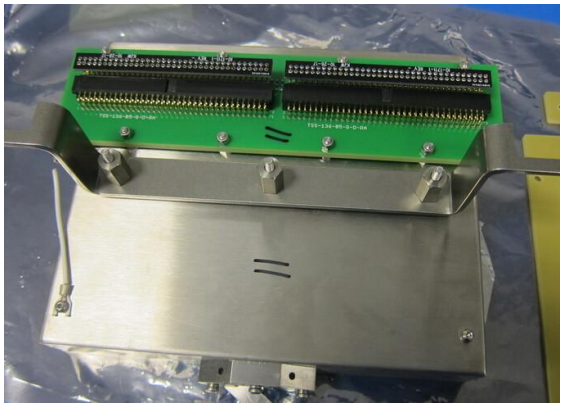
4. There is a reference to ground braid with resistor in APA handling documents [EDMS#2782612]. What is resistor value?

   ~1 MOhm. The value is specified at the beginning of the document.

5. Please describe the design requirements and specification of the “PSL terminator board”?

   We assume the reviewer is referring to the CE adapter board. The CE adapter board is a relatively simple design – a 96-pin rectangular connector soldered to a small printed circuit board. Its purpose is to terminate the inputs of FEMBs.





6. APA handling document [EDMS#2781612] seems to reference specific people and specific APA?

   References to specific people and specific APA have been removed.
   Please see updated procedure in EDMS # 2781612 (2781612_APA_Handling_CERN_ColdBox.pdf)

7. When using anti-static bags for long term storage, is a desiccant used?

   For the long term storage we are planning to use resealable antistatic bags with desiccants. We are also considering installing humidity indicator cards in storage containers, if applicable. A detailed procedure will be finalized before the PRR.

Questions and comments related to the FEMB (from CE_FDR_Document_docx)

1. "There are several options for the calibration pulse injection available on the FEMB design." Why is this needed? How has it been used so far?

   Different options are only needed for the lab debug tests. So far, the default configuration is to use the LArASIC built-in calibration injection, which satisfies the needs of charge calibration. In addition, an external calibration pulse can be injected through a connector on the WIB front panel for lab test and debug test on rare occasions.

2. What is the selected power distribution option? (page 9 of doc)

   Option 1 is the default configuration and has been used so far. No performance difference was observed for two options in the lab tests.

3. 100 monolithic FEMBs have been produced so far. Were there any problems (i.e. reworking necessary)? Has this production been done with a single company taking care of both the PCB production and the assembly or with separate companies? Were there specific QC tests for the PCB (e.g. coupon with all types of vias, metallurgy analysis, …)? What is planned for the production?

   The production experience of 100 FEMBs has been reported in the TPC electronics consortium meeting on 06/27/2022, some reworks are needed.
   https://indico.fnal.gov/event/54970/contributions/243967/attachments/156578/204421/CE%20QC%20Status_V3%5B1%5D.pdf

   Production of FEMBs is handled by two separate companies:
   - *PCB fabrication: Palpilot with PCB fabrication house China Fastprint.*
   - *Assembly: AA-tech, an assembly house located in Long Island, NY.*
   - *BOM is handled by the BNL team.*

   The PCB fabrication house provides Certificate of Quality Compliance, which includes Final Product Inspection Report, E-test Report, Micro-Section Analysis Report, Surface Plating Thickness Test Report, Impedance Test Report, Solderability Test Report, Ionic Contamination Test Report, Thermal Stress Test Report, Tin Sample, Impedance Sample, Test Board, and AB Test bar.
   The Assembly house performs ICT (In-Circuit Test) to check opens or shorts on the PCB boards before they are placed into assembly, and provides the Assembly Certificate of Compliance report.

   Final production will follow the similar approach to have PCB fabrication and assembly handled independently, and BOM is handled by the BNL team.

4. Is there an explanation for the noise plot of fig. 29 (FEMBs connected to the APA and substantial variation of noise from one channel to the other)?

   The noise plot uses raw data without any coherent noise filtering, one can easily see ENC difference between induction planes and the collection plane due to different wire capacitance. Variations among different channels are observed from the CE/APA integration test, besides contributions related to detector configurations, coherent noise needs further investigation to understand the cause.

5. What is the voltage drop on the power cables from PTC to FEMB?

   The voltage drops measured at room temperature from the WIB to the PTC are 60 mV (9-m cable) and 130 mV (22-m cable). The voltage drop at LAr is expected to be about 20% of the one at RT.

6. Is it envisioned to have a burn-in procedure for the FEMB or is it assumed that a functional test at room temperature and one at LN2 temperature is enough to put in evidence possible weakness (e.g. breaking vias)?

   Thermal cycling is considered as a more stringent procedure than the burn-in test to identify weak points from the production process and eliminate the infant mortality.

7. “PCB fabrication and assembly will be performed by external companies that meet the quality standard required by DUNE and the responsible institution. A trial run of a small amount must be performed before the large purchase.” What are the mentioned quality standards?

   Both PCB fabrication and assembly vendors are ISO9001 certified. PCB fabrication needs to follow the IPC-6012 standard, and PCB assembly needs to follow the IPC-A-610 standard.

Questions and comments related to the warm electronics

The overall system description as well as the tasks associated to each of the CE components is clear (TDR update).
The two requirements documents (WIB and PTC) seem both at best in a sketch/draft form, with no separation of requirements and specifications, no numbering, no distinction of nice-to-have and essential features, no illustration of tests that will allow validating the req/spec, etc...

WIB:

1. The WIB requirements/specifications document does not seem up to date wrt the DAQ interface document (e.g. still refers to SC as part of the DAQ consortium, out of date references, ...).

   The document was last updated in January 2022. Thank you for reminding us about the reorganization of DUNE consortia. We have now updated the WIB requirements document to reflect such transformation. Changes in DUNE structure have no effect on the WIB hardware requirement. The updated version has been uploaded to EDMS#2341138.

2. The WIB requirements doc repeatedly refers to a firmware/software document that will be written but is not available for this review.

   The WIB firmware requirements document is located in the same EDMS folder as the WIB hardware requirements document, https://edms.cern.ch/document/2341138/ (see the file https://edms.cern.ch/file/2341138/3/WIBFirmwareDocumentv1.pdf). Sorry for not referencing it in the FDR documentation. We now have added the link in the hardware requirements document as well.

   While I don't think that firmware or software will have an impact on the hardware choices of the system (all critical paths in the FW have already been exercised at the HD coldbox, with the new version of hardware), it would be good to have a tentative timeline of when effort will be devoted to finalising the complete firmware and software designs.

   The WIB firmware and software are fully functional now, but they will continue to evolve. For example, we are currently changing from the original DUNE timing system protocol, which uses a clock data recovery chip, to the new protocol which does not require a clock data recovery chip. We are planning to switch from 8b10b encoded output to FELIX at 9.6 Gbps to 10 GbE output as soon as we receive Ethernet firmware from the DAQ group. We also envision adding rudimentary data quality monitoring.

3. The weight of the WIB may not exceed 5 kg. Should this read WIEC?

   No, there is no mistake here, the weight limit is for a single WIB. The number comes from engineering analysis in https://edms.cern.ch/file/2086498/1/Engineering_Note_Cryostat_Penetration_1_docx_cpdf.pdf . The cold electronics flange, x-shape spool piece, cryostat flange, etc. are mechanically strong to support the weight of ten 5-kg WIBs. We weight limit for the WIB is obviously not a limiting factor in the final electronics design.

4. Uptime: if a problem occurs action needs to be taken to disable / replace or re-configure a piece of faulty hardware. In this case the physical intervention is probably the driver of the downtime. And probably it is not very relevant if re-configuration takes 1, 2 or 5 minutes?

   Yes, if the interruption in data taking is caused by a faulty hardware which requires physical intervention, a 5 minutes of extra delay time for re-configuration probably does not add much to the total downtime. However, a 5 minutes reconfiguration time on every DAQ run restart or change in operating settings will be a very unwelcomed and prohibitive feature.

5. Filters of the fans need to be regularly maintained. Hence it should be probably specified what the regular maintenance intervals are and that the filters should be adequately dimensioned. For this of course a realistic estimate for the expected level of dust is needed. Does this also meen that the WIEC is a closed system with a well defined air inlet and outlet (so that all incoming air is filtered)?

   Correct. Section 8 of the Hardware Requirements document says that "We will perform measurements at SURF in a location where we expect the dust level to be similar to that of DUNE" which will provide required inputs for the determination of maintenance intervals. Yes, the WIEC is a closed system.

6. Data manipulation/reformatting and transmission to DAQ must be performed without corrupting or losing the data. Occasional soft errors (aka bit flips) are generally not a problem. A rate for the maximal tolerable error rate should be specified. "Occasional" is very open to different interpretations.

   The sentence stating, "Occasional soft errors (aka bit flips) is generally not a problem" will be removed. The rate of such errors should be so low as to be indistinguishable from zero.

7. Are there further requirements on the clock like phase noise and jitter?

   There is a requirement that the WIB clock jitter be less than 180ps (SP-ELEC-31). This is because the ADC sample clock is derived from the 62.5 MHz clock from the WIB. The maximum allowable jitter in the sample clock is related to the desired ADC ENOB of 11 and assumes a signal bandwidth of 410 kHz (corresponding to the .5 microsecond shaping time of LArASIC). This will be added to the WIB V3 specification document.

8. A maximal tolerable bit error rate on the data links should probably be agreed upon. It is obvious that a successful link can only be developed in collaboration between sending and receiving ends.

   This could be done as a modification to the CE/DAQ interface document.

9. Does the electrical specification for the link between the PTC and WIB exist? The section 20.1 does not say much.

   Please let us know which specific links that you would like to trace and we can provide additional documents. Differential signals are LVDS with 100 Ohm impedance controlled traces. Single ended signals are LVCMOS with 50 Ohm impedance controlled traces. For I2C communication, the SDA line is implemented with open drain logic for bidirectional data flow.

10. You exclude the possibility of sending data from the DAQ to the WIB. Should you not leave this option opened and in future upgrades you might want to go to more fancy protocols with some kind of acknowledge or re-transmit requests. (if this will not happen, there is not much effort wasted in also having the other direction communication channel routed to the FPGA).

    The WIB has duplex links to the DAQ system through two SFP+ modules; the physical links from DAQ to WIB exist.

    A one way communication from WIB to the DAQ system is sufficiently robust as demonstrated in the ProtoDUNE with FELIX based DAQ system. No communication from DAQ to WIB is needed, since all WIB-related configurations are through CCM. To implement a two-way communication with the DAQ through a data link, an additional fiber plant will be needed, which is not foreseen.

    If DAQ moves to the 10 GbE based system, more complex protocols may require communication from DAQ to WIB. The CE consortium will rely on development and demonstration of such a system by the DAQ system first, before considering any commitment about this.

11. Why do you need to be able to measure the length of the cables between the WIB and the FEMB?

    The data from various FEMBs attached to the same WIB and to different WIBs need to be synchronized (aligned in time) in order to facilitate tracking. The bottom-mounted FEMBs are connected to WIBs using 22m cables; the top-mounted FEMBs are connected to WIBs using 9m cables. The difference in cable delay is approximately 74ns. While this difference could be corrected for using a constant, it is straightforward to measure the cable delay and use the measured number to align data in each WIB in a way that ensures system-wide synchronization.

12. The WIB PCB files are pdf files in black and white: not easy to review (e.g. it is impossible to follow traces, look at trace lengths, …). Some differential pairs are not length compensated. Would it be useful to equalize the lengths?

    Let us know which specific differential traces that you want to look at and we can provide additional documentation. All the differential traces should be matched to themselves to within required specs.

PTC Related questions:

1. The PTC requirements doc erroneously assumes an interface to the DAQ (its SC component). The SC is not part of the DAQ.

   Thank you for reminding us. We will update the document.

2. The PTC requirements document (introduction) refers to the PTC interfacing to the DUNE Detector Safety System's PLC. I think it would be more appropriate to refer to the DUNE CE safety system, since at the moment there is no overall DUNE DSS design.

   We agree. We will refer to our system as the Cold Electronics Safety System (CESS).

3. The PTC board satisfying the requirements outlined in the document has not been exercised yet, therefore the PTC board used in PD-SP is still the baseline: nevertheless, the latter satisfies the basic needs for DUNE, but not the set of requirements outlined in this document. So, do we have a baseline or not?

   The new PTC will facilitate our use of Beckhoff controllers in a detector safety system and it is our baseline. The existing PTC satisfies all DUNE requirements. It will be used in ProtoDUNE-II (HD) and also in FD1 if the performance of the new PTC does not meet expectations. A successful final design review is supposed to indicate design maturity of 90%. We believe that our design maturity exceeds this standard.

4. The minimal efficiency for DC-DC buck converters is not quantified.

   The minimal efficiency is 85%.

5. The maximum current to be sent to each WIB by the PTC is not quantified.

   The maximum current to be sent to each WIB by the PTC is 6 A.

6. The maximum voltage ripple on the voltage regulators is not quantified.

   The maximum voltage ripple on the voltage regulators is ~10mV rms.

7. The dimension of fuses between LV power supply and PTC is not quantified.

   There are no fuses between the LV power supply PL506 and PTC. The protections are set at the PL506 by software channel configuration. These settings and limits of the

channels can be set in the Slow Controls as well the action. At the present, the current limit is set at 10 A and the action is "switchoff the channel".

8. A thermal fuse is foreseen between LV power supply and PTC, but the temperature limit is not quantified.

   We plan to remove the "thermal" requirement on the fuse from the requirement document.

   The LTM8046 starts to derate around 50C. Jack Fried's temperature measurements on PTCv3B indicate that some of them run that hot. The confidence in estimating the PCB or air temp on PTCv4 is low at this stage, so it's hard to predict a limit. PTCv4 will have at least 3 board-mount temperature sensors in different locations, as well as the ability to monitor the FPGA die temp via Xilinx's on-board measurements. This should give enough information about whether any PTC components are running too hot.

   Whether or not there is enough cooling is a separate – and important – question. Our understanding is that the crate is capable of 30 CFM airflow. A more conservative number is being used in the Xilinx Power Estimator (XPE) for the FPGA temperature estimation.

9. "The PTC shall multiplex the return signals from the WIBs and transmit them back to the timing system." Is "de-multiplex" meant here? Are many signals transferred over a single communication line to the timing system here?

   The WIB MUXs timing signals coming back from WIB. Each WIB has a point-to-point link back to PTC for transmitting to the timing master, as in Fig 1(a) below.

   Fig 1(b) shows an updated firmware diagram, illustrating that this functionality is in hardware, not FPGA.

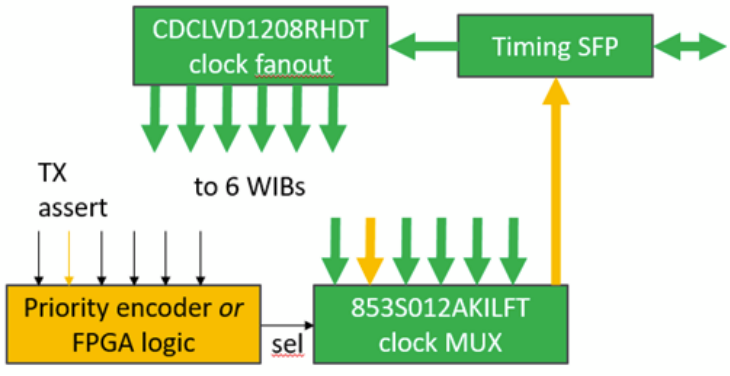


Fig 1(a)

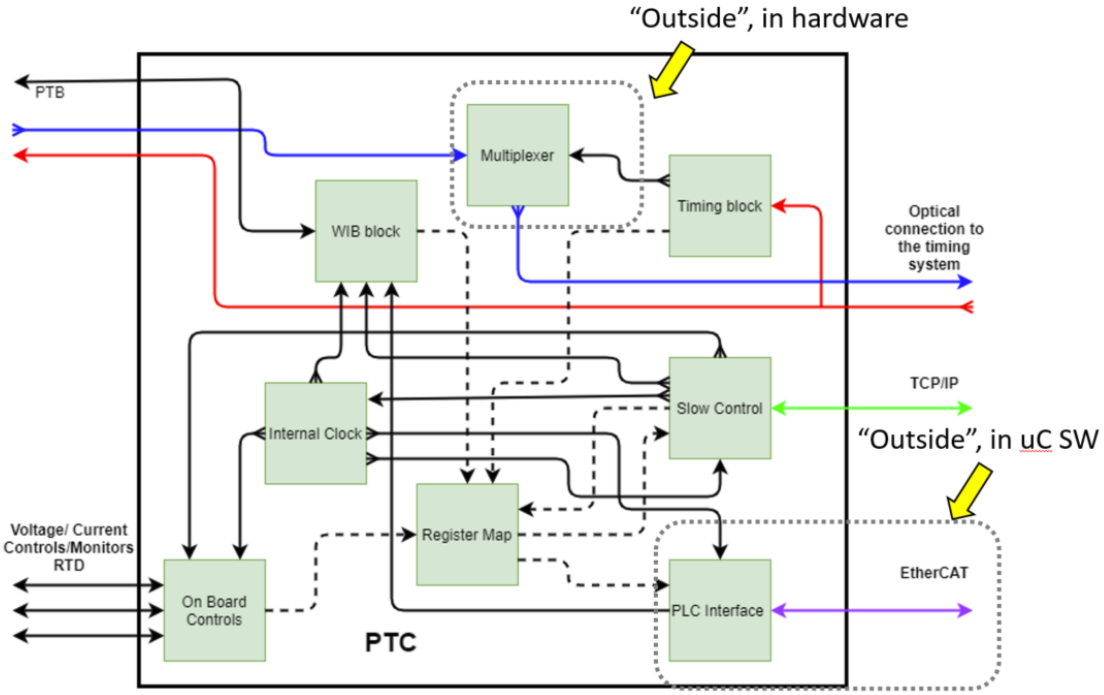


Fig 1(b)

10. "It is not clear at this point whether these operations require that the PTC be synchronized with the master clock (i.e. that the PTC itself is an additional timing end-point), or whether the PTC can operate asynchronously from the timing system and only …". When will this be finalized?

    We do not foresee a need to synchronize any operations with the Bristol timing system. However, the FPGA can decode the timing stream and extract time stamps if needed.

    The requirement to transmit some kind of timestamp is a decision for the DSS group.

11. "Need to understand whether the FPGA in the PTC is involved in this and whether there needs to be a delay in the broadcast of the information back from the WIB to the timing system to allow for this priority handling." When will this be finalized?

    This comment is from pp3 of the Requirements v2.00, and refers to the operation of priority encoding the TX return data from WIBs to the timing master) We are using the same scheme as PTCv3B, which fans out the timing stream to WIBs with a hardware clock fanout, and MUXs the transmission back to timing master with a hardware priority encoder based on point-to-point assert signals from the WIBs (see diagrams in Q2). There is no need to add any delays.

However, there is the possibility in the new PTC to decode the timing stream and control the MUX with the FPGA instead of with the hardware priority encoder. This could shield against potential errors where WIB keeps a TX line asserted in error. Both methods can be tested, however we note that using the latter method is likely to require a handshaking with WIBs upon powerup to determine their timing endpoint addresses.
In either case, the PTC will never allow timing information itself to be delayed by the FPGA before going to and from WIB; both schemes refer only to the handling of the SFP enable/disable for any WIB that wants to transmit back.

12. Is it planned to use an FPGA with a Zynq processor? This processor can do the communication to the outside world (e.g Slow Control) without the need of developing firmware for this. In addition it can easily handle the TCP/IP protocol which simplifies the development of the communication since high level software components can be used).

    Yes, the PTC will use a Zynq UltraScale+ system-on-chip (SoC) for prototypes. Please see the draft Specification for details: https://edms.cern.ch/document/2731292/3

13. PTC hardware address. Will you use 7 bits or 8 bits? It would be safer to have a large number of bits (16?) in view of possible upgrades.

    PTC can use an 8-bit address set by DIP switch. It will also be possible to use an on-board EEPROM to store a larger address if needed.

14. Concerning the MAC address, why not using geographical addressing as for the WIEMB and then get a TCP address via DHCP and ClientID mechanism? Then use standard network technology.

    Yes, it is preferred to generate MAC addresses based on geographical addresses. There will be an 8-bit crate address plus the 3-bit slot address, so each PTC or WIB can construct a unique address. Algorithm for constructing geographical addresses TBD.

15. “The address of each WIB in the I2C ring will be based on its location in the WIEC. [As an aside, each WIB installed in a DUNE far detector module shall have a unique identifier based on the individual 8-bit hardware address of the PTC in the same WIEC, …”. Since i2c is cheap and does not take resources do you consider implementing 2 rings for redundancy?

    What failure mode is a redundant I2C bus shielding against?

    I2C goes from PTC FPGA to WIB FPGA in a tree topology, not ring. If a WIB pulls the I2C line down in error, it is true that bus contention could occur for other WIBs. In the case of a powered off WIB, this is because WIBs have no IO buffering for the following signals: timing TX enables, crate address, spare IOs (which the I2C will be implemented with). This means a powered off WIB’s FPGA can pull down a line because Xilinx FPGAs are known to source current in a powered off state.

    There are two solutions, for prototypes ONLY:

    --Do not power off WIB for the first prototypes; only power cycle if needed, or remove from crate

    --Re-spin the PTB (power and timing backplane) to include buffers powered by local WIB 2.5V and PTC 2.5V

    Unless the redundant I2C bus is completely isolated from the WIB FPGA, the same failure could occur on the redundant bus.

    A redundant bus would require more pins on the backplane connector.

    The decision to update the backplane connector on PTB, and/or the WIB hardware, to address these limitations is the responsibility of the WIB/PTB team. The issue of these possible failure modes has been raised previously.

16. TCP/IP is foreseen as an interface to the Slow Control which is good. The PLC interface obviously talks EtherCAT. Is there also a direct connection to the Dune control system (run control)? Is this something which should be foreseen?

    The connection of the PTC to DUNE Run Control is only through configuration and operational monitoring. The DUNE DAQ Control, Configuration, and Monitoring (CCM) will access the PTC through a DAQ module called “ptcmod”, and which will be responsible for configuring the PTC, and for reporting on run-time errors, and any runtime metrics we decide are useful (though for the PTC, which is not part of the data flow in any way, there are few if any of these).

17. The OPC-UA is running on top of TCP/IP (the block diagram has a TCP/IP label attached). Another argument for having a processor in the FPGA as stated earlier.

    Agreed that a Zynq UltraScale+ can be used to implement OPC/UA – Zynq will be used (see PTC Question 12 above).

    If OPC/UA is not used on prototypes, the FPGA fabric is still available to implement other features.

18. Not clear why the communication of the PTC to the slow control (on detector ground) needs to be optical. Also the 1000Base-LX10 SFP specification seems unnecessary.

    The current system design is that DAQ is on building ground and other systems (DCS, SC, DDSS, and TPC electronics) are on detector ground. The systems are electrically isolated via fiber connections.

    The PTC can easily switch from fiber to copper by plugging a different transceiver in the PTC. In the past we observed a slightly higher noise using copper connection to the network switch. Our preference is to stay with fiber, but we are open to the option of using copper connection provided the connection doesn't introduce additional noise to our system.

19. There seems to be quite some redundancy in what is monitored via the WIBs and via the PTC. What is the rationale between these duplicated paths? WIB monitoring data are now transmitted both via the PTB to the PTC (and the PTC relays to SC and DDSS) and directly to the SC.

    The current design allows us to provide monitoring data to the SC and DDSS before the upgraded PTC is available. Our long term plan is to use PTC to transmit monitoring data, but we will work with SC and DDSS to optimize the data path. As pointed out by the reviewer, there is some flexibility on how we transmit the monitoring data.

20. Slow control monitoring rates seems very high. What is the need of providing PTC status at >10Hz?

    We will likely not readout the PTC at a high rate during normal operation. This functionality is reserved for debugging purposes.

21. Why does the WIB need to be individually powered on and off? Although there should be the possibility to individually power on and off the FEMB in the cryostat, the WIB is "just" an electronics card in a crate ?
If we have to turn off the whole crate every time we have a bad WIB (until we can replace it), we will lose a whole APA each time. Replacing things underground is not like replacing them at CERN—it will take time to get a cage and get people down there who know what they are doing. The ability to turn off subsets of the system will be important for maintaining total channel lifetime.

22. The granularity of the DDSS “enable/inhibit” seems exaggerated. A study of likelihood of faults, complexity vs simplicity should be carried out. As an example, a simple inhibit to the power supply powering a single WIEC may be more than sufficient, rather than inhibiting individual WIBs for safety purposes.
Our CE safety interlock can inhibit individual power supply channels. As stated by the reviewer, the granularity is per WIEC and per APA wire plane. The ability to switch off individual WIB can be a part of the safety interlock, but that feature is envisioned more for ease of operation (turning off 1 problem WIB instead of the whole crate) rather than for detector safety.

23. "The PTC shall communicate with the DUNE Detector Safety System (DDSS) via a 100BaseFX SFP transceiver which transmits/receives over a OM2 duplex fiber at 1310 nm with an LC connector on the PTC side and an SC connector on the other end (need to check compatibility of transceiver with the Beckhoff EK1521, which would be preferable to the Beckhoff EK1521_0010).” This specification seems wrong: OM2 supports MM (850 nm) and not 1310 nm. The interface between the DDSS PLC and the PTC is not clear. Is etherCAT really needed? This whole part misses a clear set of requirements and system analysis. It is not clear in first place why the PTC doesn’t take care of the safety interlocks within a WIEC itself with a simple slow control notification of the actions taken.

The Cold Electronics safety system is described in detail here: https://edms.cern.ch/document/2401090/2.

At the moment the official Dune Detector Safety System (DDSS) is not very well defined. There are a couple of options to communicate with DDSS via either OPC-UA server on the PTC or directly between Beckhoff system running OPC-UA. The detail will need to coordinate with the DDSS group.

PTC design team is implementing EtherCAT using a commercial Infineon XMC4300 microcontroller to be compatible with the specifications linked to above. PTC will just have a standard SFP cage so any standard SFP module can be plugged into PTC. We will verify the supported wavelength of OM2.

Table 1-
Bandwidth and attenuation comparison between different OM fiber optic cables

Multimode Fiber			Bandwidth (MHz. km)			Attenuation (dB/km)	
Nomenclature	TIA Fiber Standard	Core Diameter (micron)	Overfilled Launch (OFL) at 850 nm	Overfilled Launch (OFL) at 1300 nm	Laser Launch at 850 nm	At 850 nm	At 1300 nm
OM1	492-AAAA	62.5	200	500	Not specified	3.5	1.5
OM2	492-AAAB	50	500	500	Not specified	3.5	1.5
OM3	492-AAAC	50	1500	500	2000	3.5	1.5
OM4	492-AAAD	50	3500	500	4700	2.5	0.8

24. FPGA: while indeed the WIB's FPGA is surely sufficient for the PTC, it also is probably an overkill. No considerations on cost are made in the choices made.

    PTC cost is a major driving factor in the design. We originally chose the same FPGA as the WIB for cost reasons. If the PTC FPGA procurement is piggyback off the WIB procurement, then the unit cost of the FPGA is about $400 instead of >$1000. The main design issue is that we had trouble fitting the FPGA and all its voltage regulators on the main PTC PCB footprint. We then decided to use a mezzanine card for the FPGA. At that point, it was cheaper and faster to use a commercial FPGA card instead of designing and fabricating a custom mezzanine board. The PTC is designed to be able to accommodate different classes of the EnClustra FPGA mezzanine card.

25. All in all, it seems that the PTC requirements and specifications (let alone the design and implementation) are rushed and not thought through, for all those aspects that were nor already foreseen in the original PTC.

    Are there any other specific examples of aspects that need further addressing?

PTC specifications (EDMS 2731292):

The technical details of the timing system are correctly described, but the proposed solution is complicated to implement and has a risk of not working correctly. Below is a sketch of a possible implementation of the Timing – PTC – WIB link that is much simpler than the one proposed in EDMS 2731292 and much more likely to work:

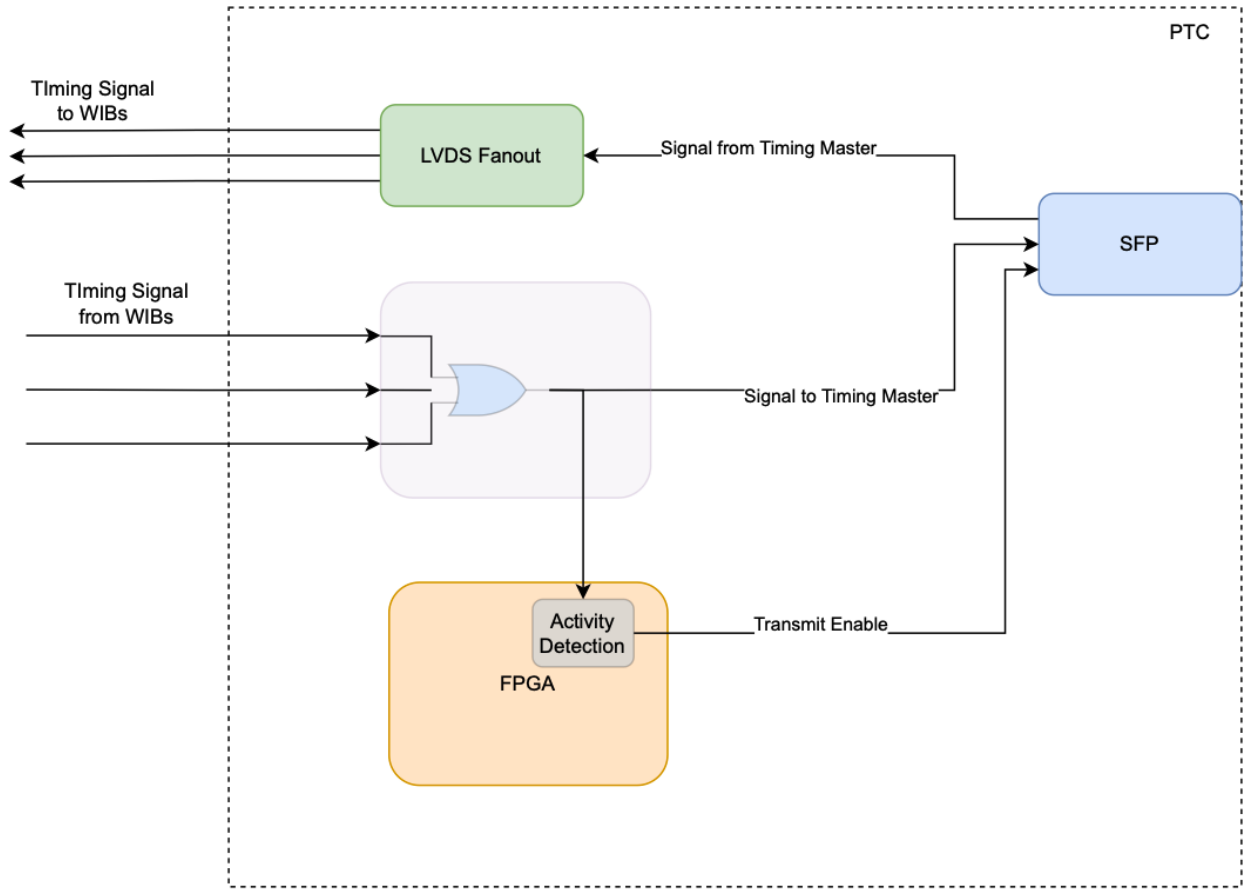


Fig. 2

The explanation of how messages are sent to/from the timing endpoints from/to the timing master is correct. However, the suggested implementation of the fanout/multiplexing of timing signals on the PTC to the WIBs isn't optimal.

1. The suggested implementation (figure 2) routes timing data through the PTC FPGA. This is not optimal.

The diagram in the draft requirements is out of date. See diagrams in PTC Question #9 for details – I believe this is consistent with the explanation in this section.

a. Accurate measurement of the round-trip delay needs the delay from/to the WIBs to/from the timing master to be symmetrical and stable. If routed through the FPGA this means the data should not be registered (fed through flip flops) inside the FPGA. Asynchronous logic is not easy to implement reliably in standard FPGAs. The delays inside the FPGA may be significant and hence may vary significantly with FPGA temperature. Also, the delays may vary every time the firmware is rebuilt unless complex placement constraints are implemented.

b. The standard timing endpoint firmware only recognizes one endpoint address. Modifying the endpoint firmware to recognize multiple addresses (for the multiple WIBs in the crate) will require effort. The timing group is happy to assist with all areas of integration, but is not enthusiastic about writing custom firmware for the PTC.

c. There is a much simpler implantation (illustrated in above sketch):

   i. Fan-out the timing data from the timing master in an external LVDS fanout chip

   ii. Use a logical “OR” to combine the data from the multiple WIBs. This works because the timing data output from a WIB that doesn’t have the Tx enabled is “0”. Feed a copy of the “ORed” data to the FPGA

   into logic that detects 0/1 and 1/0 transitions. If there are transitions, the FPGA asserts the “Tx enable” line to the PTC SFP. When there are no further transitions, after a timeout, the FPGA de-asserts the Tx-enable line. The DCSK protocol guarantees one 0/1 transition and one 1/0 transition every 16ns so the timeout can be very short compared to the SFP laser turn on/off time (up to 1ms)

Questions about electronics production

1. Is it planned to have the production of all the boards (FEMB, WIB, PTC,..) following the same model (single company managing PCB production, components ordering and assembly, or different companies) and using the same company-ies for all the boards?

   Final production will follow a similar approach during prototype and pre-production to have PCB fabrication and assembly handled independently, and BOM is handled by the BNL team.

2. Will the call for tender documents be reviewed at the time of the PRR?

   Thanks reviewers for this comment. After the FDR, we will need to work with the BNL and Fermilab procurement departments to launch the discussion of the production procurement, which includes the preparation of tender documents and following necessary regulations. It is expected that good progress in preparation of the tender documents will be made by the PRR.

Questions relating to QA/QC

1. The LBNF/DUNE Review Plan requires the QA/QC Plan to be a deliverable document. Will the QA/QC Plan information in the CE FDR document be translated in a QA/QC Plan document?

   Yes, we plan to consolidate the various QA/QC documents in a QA/QC Plan following the DUNE guidelines before the FD1 TPC Electronics PRR.

2. The LBNF/DUNE Review Plan requires a Production Site manufacturing plan for the production sites. Has it been determined which sites will be responsible for which assembly and QC activities?

   Yes, the MOU in (EDMS#2708334) summarizes the responsibilities. For example, the following institutions are committed for ASIC QC (BNL, FNAL, LBNL, UC-Irvine, LSU, MSU, Iowa, U. Cincinnati, U. Florida), UPenn is responsible for the fabrication and QC of PTC, WIB firmware is a combination of BNL, UPenn, and U. Florida, APA bias and LV power supplies are FNAL, FEMB and WIB production are BNL, etc.

   Yes, we will have the Production Site Manufacturing Plan ready before the FD1 TPC Electronics PRR.

3. There are several instances in the QA/QC Plans that use the terms “should”, “recommend” and “typical”. In these cases are the requirements optional?

   Thank you for pointing this out. We will update the final QA/QC plan to remove those ambiguous terms.

4. There is a visual inspection of the FEMB PCBs. Has criteria for this visual inspection been determined?

   All PCBs will be vacuum sealed in the bags. The inspection of the FEMB PCB has a focus to identify potential issues during the shipment and handling.

5. On the post assembly FEMB checkout, there are several items listed as typical inspection items. It is not clear if this list is all inclusive or if they are required to be used. Is this list meant to be required inspection items and are there more that should be listed?

   The current plan is to have the typical inspection items covered in the post assembly FEMB checkout. The plan will be fine tuned based on the pre-production experience.

6. The FEMB checkout test is listed after the visual inspection. Has this checkout test been put into a procedure? Have acceptance criteria been determined for these inspection items?

   Yes, this step is important before FEMB is put in the CE box assembly. The procedure described in section 2.6.2.3 will be followed, the acceptance criteria needs to be finalized once enough statistics become available.

7. Paragraph 2.6.2..4.3 of the CE FDR document discusses the Phase of test at LN2 temperature during ProtoDUNE-1. It is not clear if it is required for DUNE production. Is it the intent of this paragraph that these tests will be required?

   As has been pointed out elsewhere, we would benefit from a single QC document that is maintained as our plans evolve. We currently plan to test every FEMB in LN2 as well as at room temperature.

8. The Phase of Post-QC test for the FEMB states that a similar fast checkout procedure should be performed to finalize the QC test. Is this checkout a requirement or is it optional?

   This check out is a requirement.

9. For the leak test of the signal feed through assemblies, the CE FDR document states that ProtoDUNE-1 had been leak tested with Helium to be better than 10^{-9} mbar.l/s. Will this be the acceptance criteria for the DUNE production?

   Yes, this is.

10. For the Cold Cabling and Signal Feedthrough QA/QC, the CE FDR Document explains what has been performed to date for pressure testing and states these tests perform the basis of the QA of the signal feedthrough assembly. It does not state whether a pressure test will be required. Will pressure testing be required for the signal feedthrough assembly?

    Pressure test is part of the QA procedure to validate that the design is robust. The DUNE (same design used in ProtoDUNE and SBND) CE flange design have been validated by two high pressure tests:
    - A 120 psi hydrostatic test on an SBND flange without surface mount connectors @ BNL for LArIAT VST. (SBN docdb 6873).
    - 80 psi pneumatic test of a ProtoDUNE CE flange, a PD flange, and a ProtoDUNE-I Tee @ FNAL for ICEBERG.

11. There is mention of a walk through test of the signal feed through and WIEC assembly installation. Have the criteria for this walk through been determined?

    The final walk-through test is to confirm all communications among WIBs, PTC and PTB inside the WIEC are working as expected.

12. It is mentioned in the CE FDR Document, that the WIB boards will go through a visual inspection. Has it been determined what the criteria will be for the visual inspection?

    All PCBs will be vacuum sealed in the bags. The inspection of the WIB PCB has a focus to identify potential issues during the shipment and handling. Post-assembly visual inspection has a focus to identify obvious assembly issues as described in section 4.4.2.3.

13. The QA/QC plan for firmware on WIB is not included in the documents. Will there be a separate QA/QC Plan for the firmware or is the firmware going to be verified through the testing of the WIB?

    Firmware will be verified in system tests. Minor bugs and shortcomings in the WIB_V3 firmware were identified in the first cold box run with APA 1 and were corrected shortly thereafter. ProtoDUNE II will provide the primary verification of the WIB_V3 firmware.

Questions about mechanical drawings:

Below is a summary of review notes compiled as documentation on EDMS is viewed.

Please extend my compliments to the consortium leadership and engineering team for detailed mechanical drawings, models and documentation.

Attached are a handful of documents which include drawing markups, suggestions for clarification and a few questions. I ask that these notes be passed along to the TPC CE Consortium.

1. See Drawing Notes_kdz.pdf. Per APA pair, the cable bundles include (in addition to cables to FEMBs) cables to APA bias, cables to FC terminations, cables to GP current monitoring, etc. This reviewer was unable to find a cable bundle assembly drawing that identifies these extra cables. Can you point me in the direction of where this information is available?

   For FD1, some APA will have FC termination cables and/or failsafe cables, and some APA will not have these cables. The exact allocations of these cables are unclear to us for now. In protoDUNE-II, the cable drawings have already prepared with FC termination cables and failsafe cable included. However, the bias cables are still missing in these drawings.

   https://edms.cern.ch/file/2772752/1/PDIICBL03_9M_1_REV-.pdf

   https://edms.cern.ch/file/2772752/1/PDIICBL03_22M_1_REV-.pdf

   We have the latest protoDUNE-II cable bundle drawing with all termination cables and bias cables included and have been added to the documentation.

2. The EDMS "Folder" called 'Parts and Assembly Drawings' contains entries older versions of 2D drawings. Which should be obsoleted? The same is true for the EDMS folder called '3D Models'. Recommend using the versioning feature of EDMS to store and upload new drawings and models to avoid confusion.

   Latest drawings and models are listed in these two documents. We will comb through the EDMS folders to remove old/obsolete drawings.

   https://edms.cern.ch/file/2771733/3/2771733_2774712_Drawings_index.pdf

   https://edms.cern.ch/file/2783038/2/HIERARCHY_OF_DUNE_CE_ASSEMBLY_DRAWINGS.pdf

3. Reviewers provided some annotated comments on the following documents and drawings:
    a. TPCElectronics_Cabling_kdz.docx
    b. 2088720_DID_SP-PDS_SP-TPC_V1c_kdz.docx
    c. 2088736_DID_APA_TPC_kdz.docx
    d. Drawing Notes_kdz.pdf

    We have reviewed the comments and agree with the recommendations. We are in the process of updating the documents and drawings to address the comments.