Single-photon imaging detector with encapsulated CMOS pixelated anode

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erc European Research Council

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Project goal and detector concept

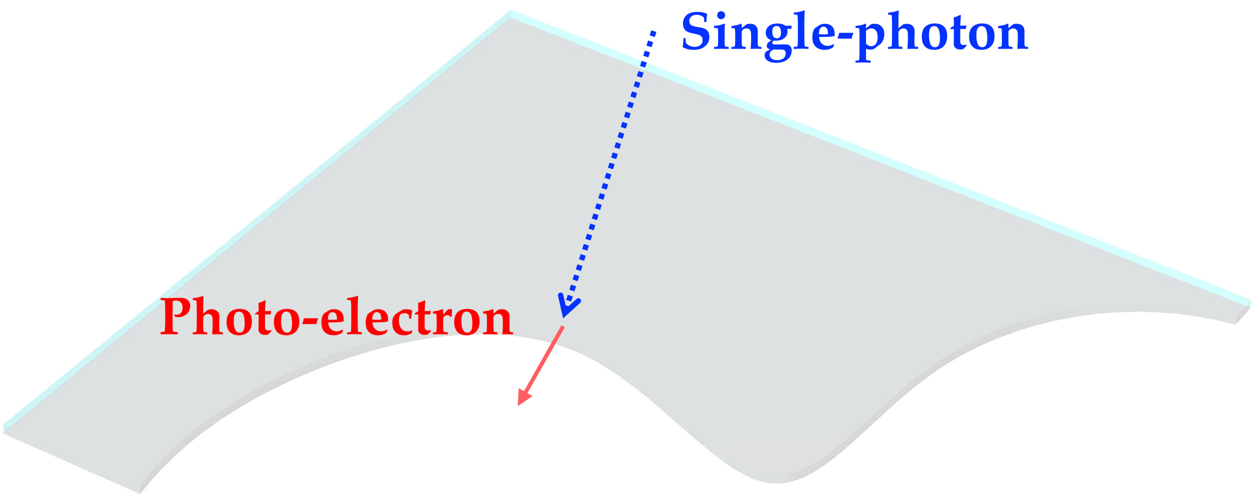
- Development of a new photodetector with large active area able to measure single photons with simultaneous excellent timing and spatial resolution, with a low noise level at room temperature
- Detector based on a "hybrid" concept:
  - Vacuum detector; photocathode with high QE in the region of interest
  - Proximity-focusing geometry
  - Micro-channel plate (MCP) amplification
  - Silicon ASIC embedded inside vacuum tube
  - Reference: JINST 13 C12005 2018

Target time resolution	<100 ps r.m.s.
Position resolution	5-10 μm
High-rate capability	10^9 hits/s
Low dark count rate at room T	~10^2-10^3 counts/s
Large active area	7 cm^2
High channel density	0.23 millions

Detector concept

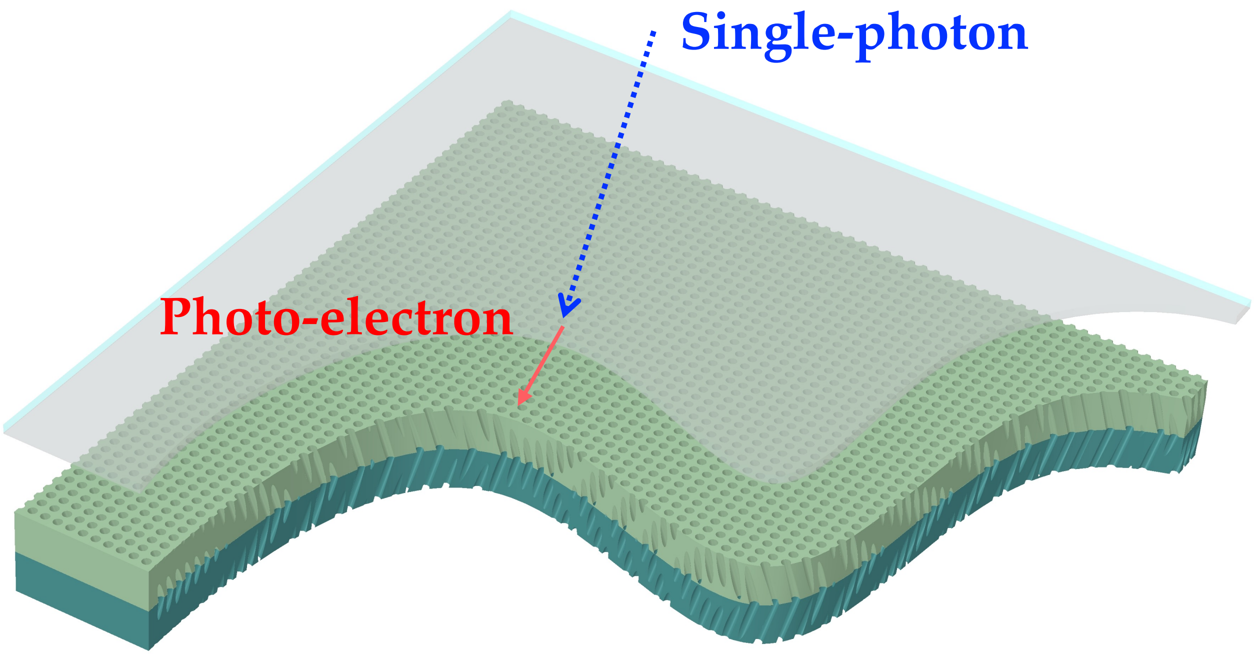
- Entrance window + photocathode

Detector concept



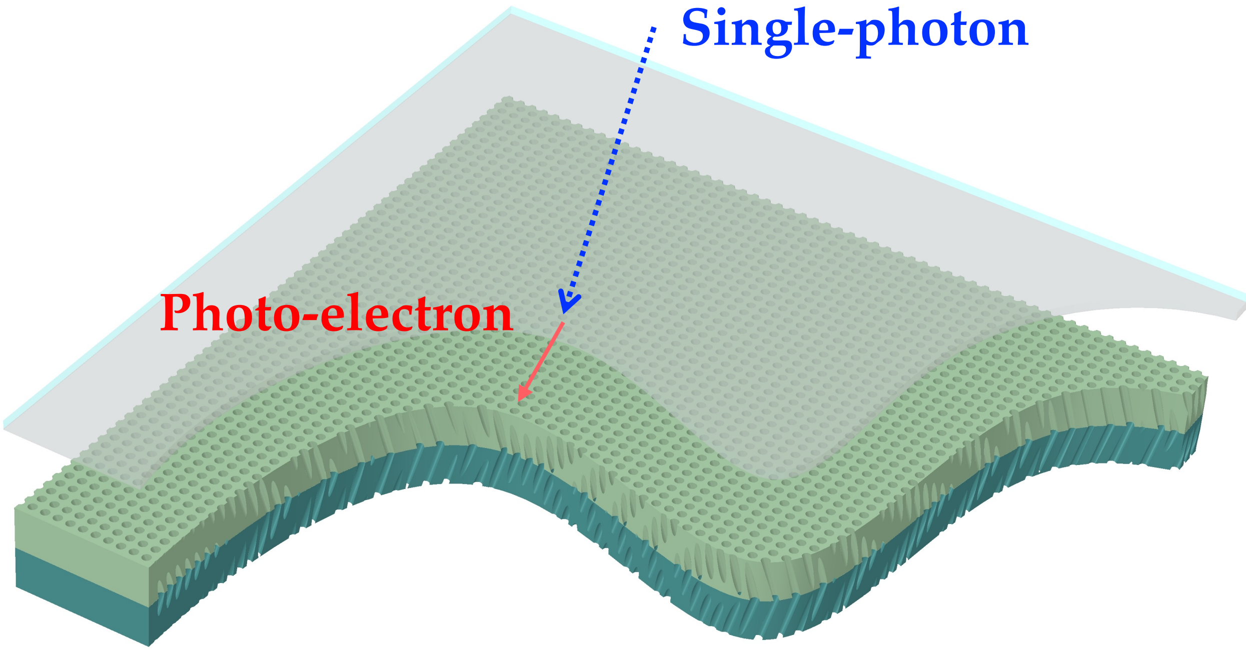
- Entrance window + photocathode
  - Photon conversion
  - High QE photocathode in the blue-green region
    - E.g. bialkali, multialkali
    - **~10^2 Hz/cm^2 dark count rate** at room temperature
    - Best for timing
  - Flexible design allows to use different photocathodes

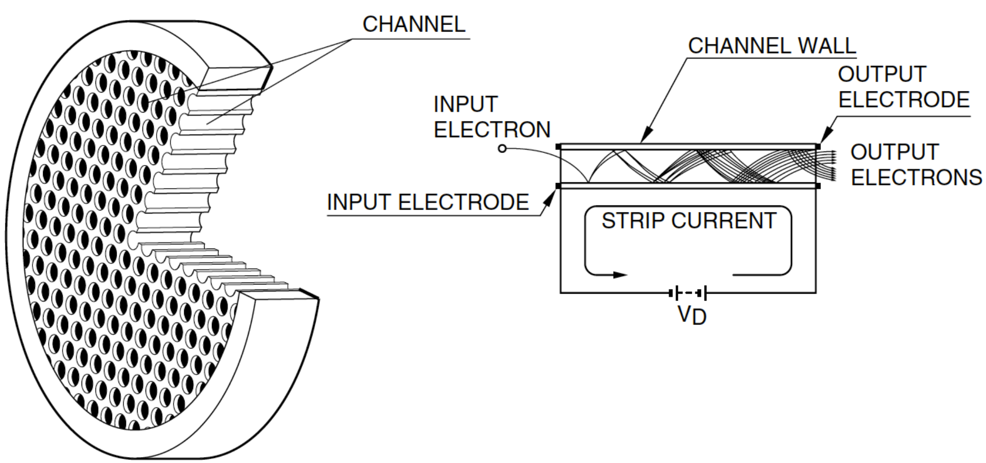
Detector concept



- Entrance window + photocathode
- Microchannel plate stack (chevron)
  - A few **10^4 gain**
  - **5-10 µm** pore size
  - Short distance from MCP to cathode and anode for best time and position resolution
  - Atomic layer deposition for **increased lifetime** >20 C/cm²

Detector concept





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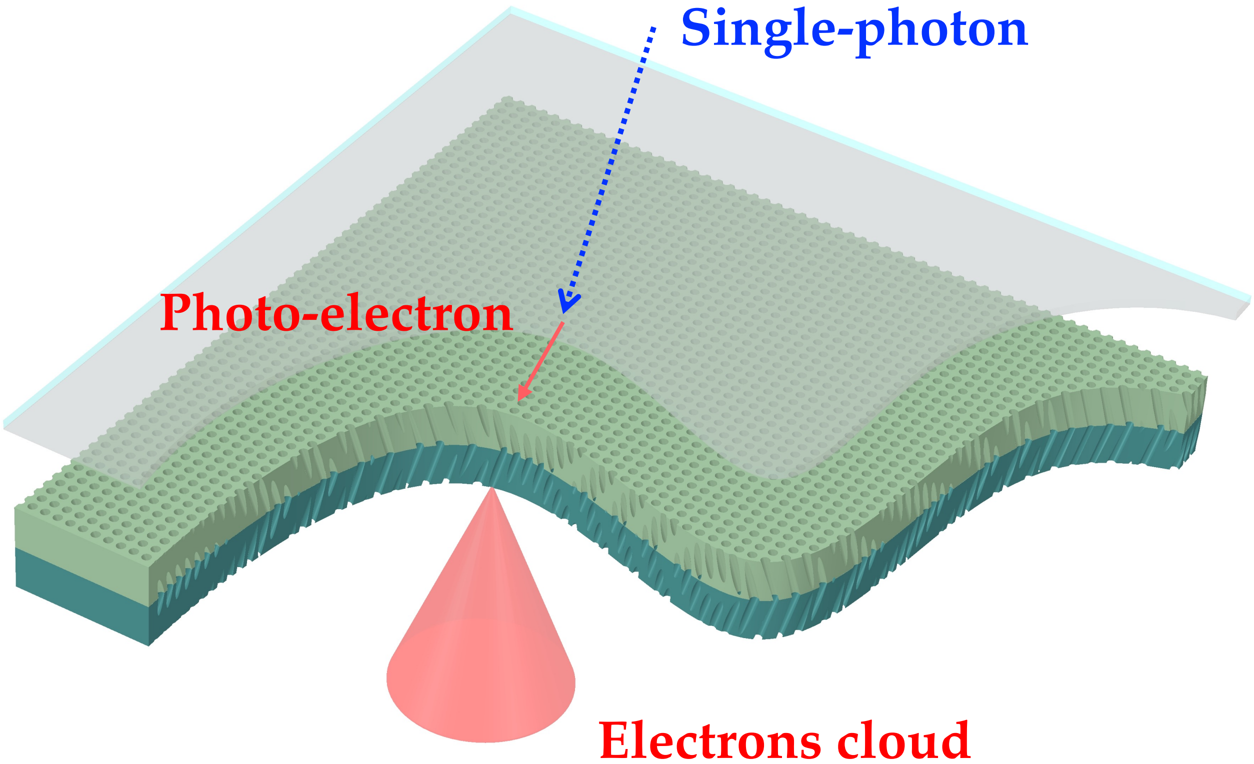

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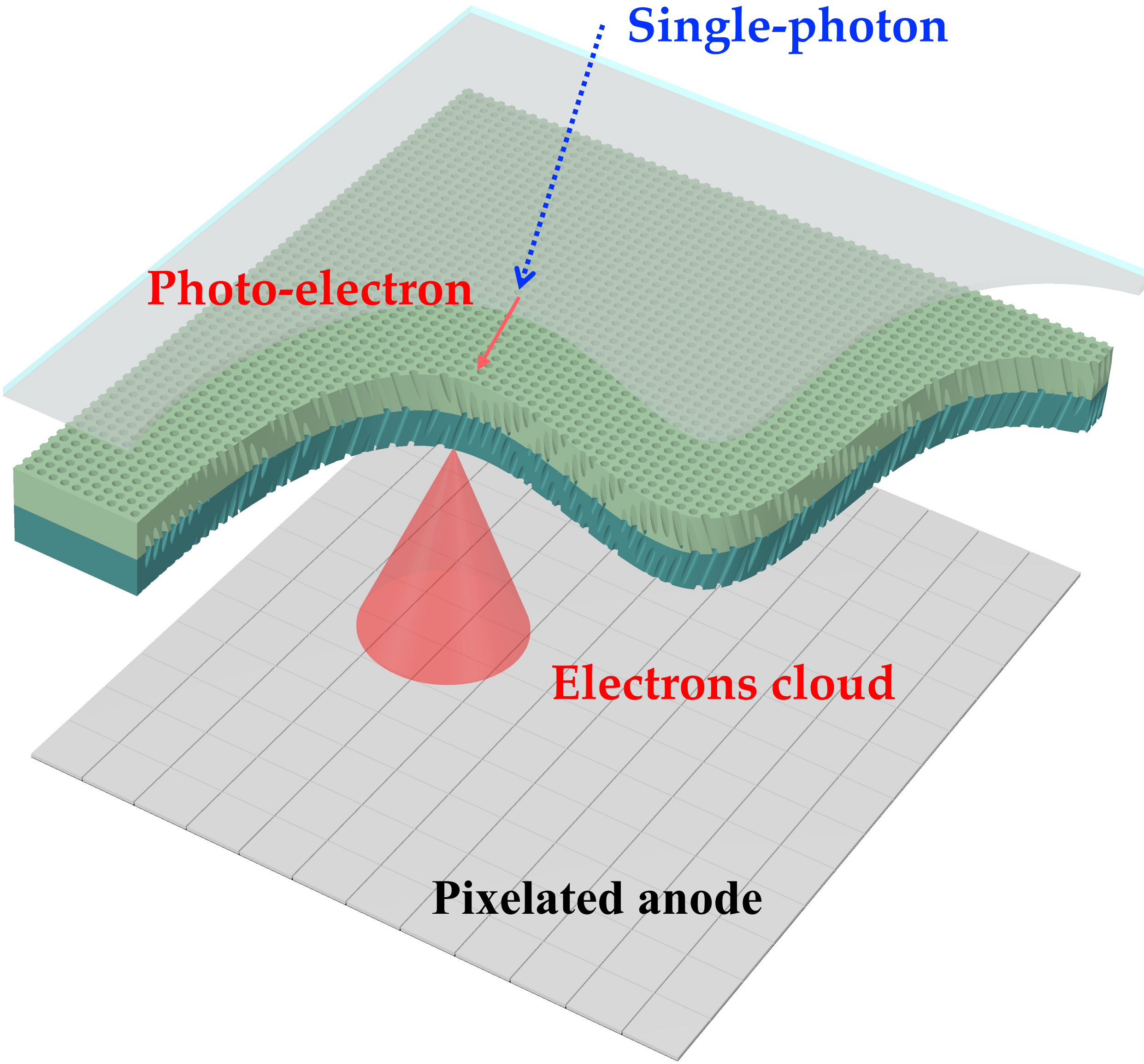
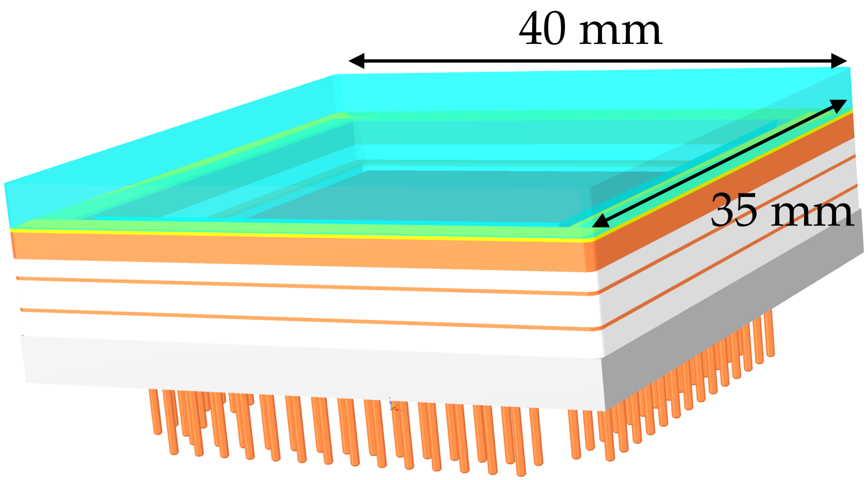


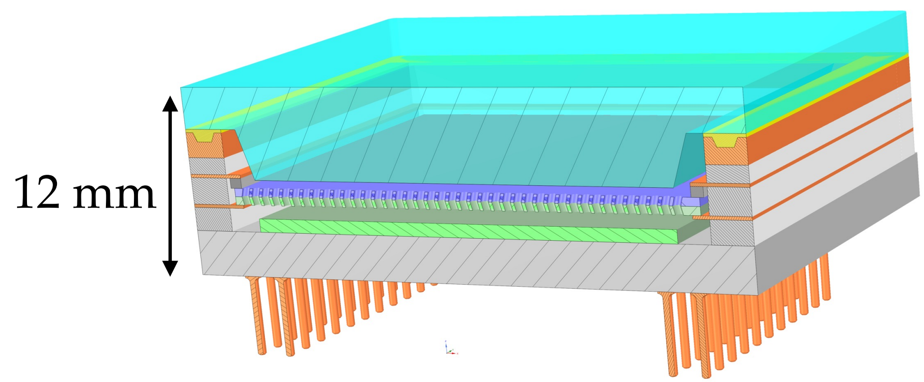
- Entrance window + photocathode
- Microchannel plate stack (chevron)
- Pixelated anode
  - Electron cloud spread over a number of pixels
  - **55μm × 55μm** pixel size
  - **0.23 M pixels** measuring arrival time and duration of input signals
  - **7 cm^2** active area
  - Up to **2.5 Ghits/s**
  - Local signal processing

Hybrid detector assembly

3D structure: detector rendering



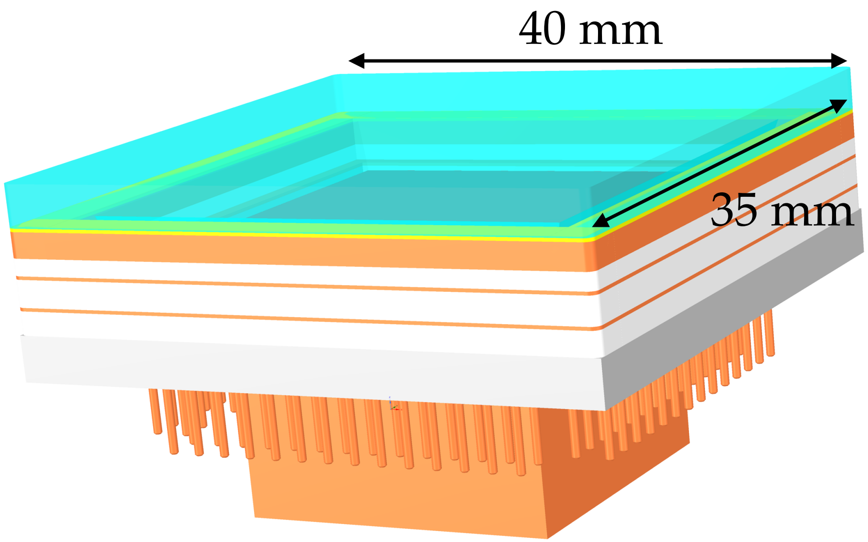
Section view

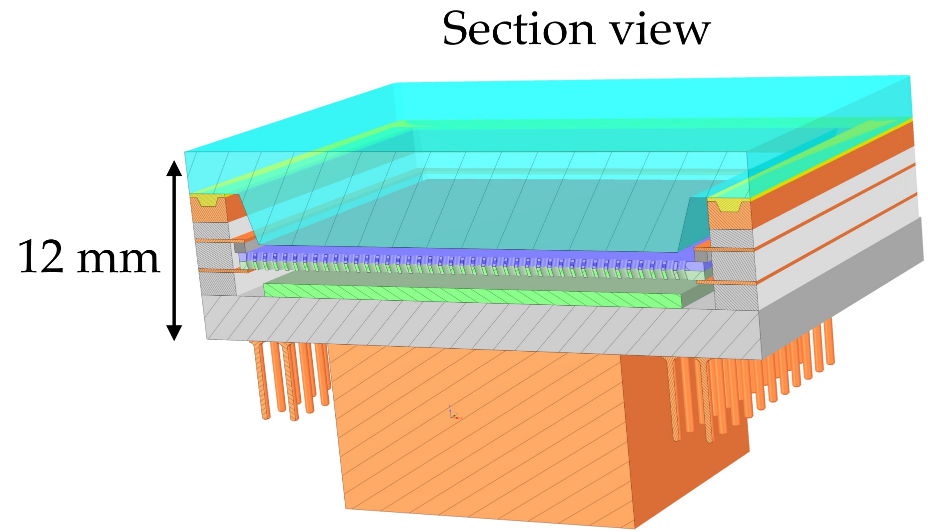


- Vacuum-based detector
  - Assembly of many components under high vacuum (~10^{-10} mbar)
  - High-speed connections through pins in ceramic carrier board

Hybrid detector assembly

3D structure: detector rendering





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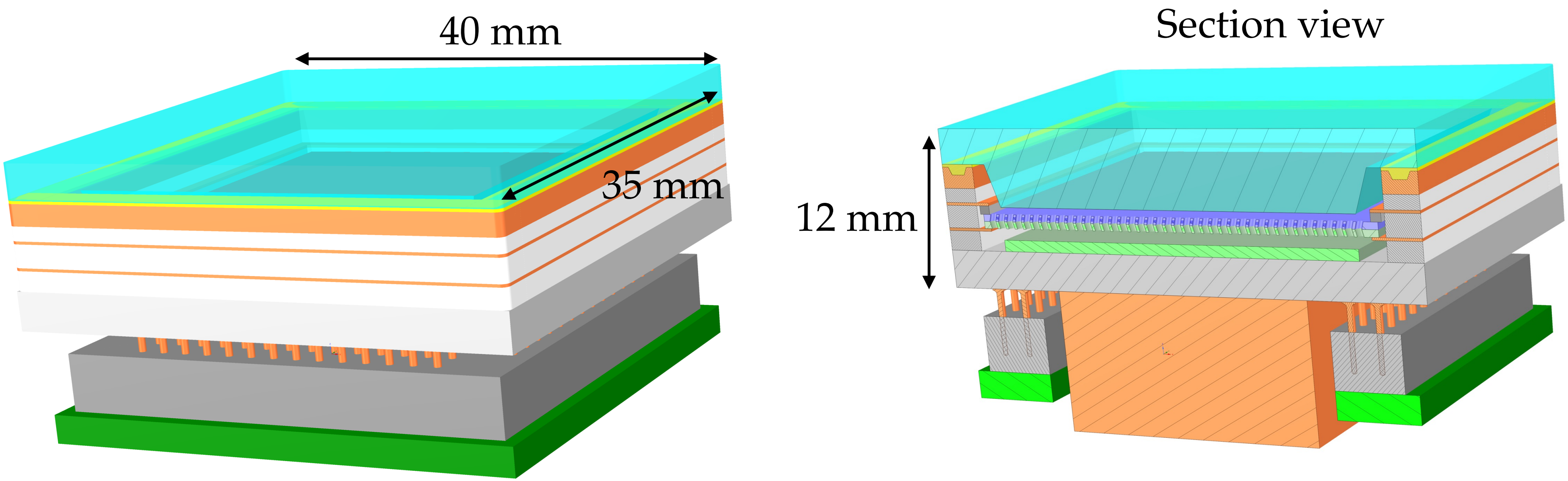
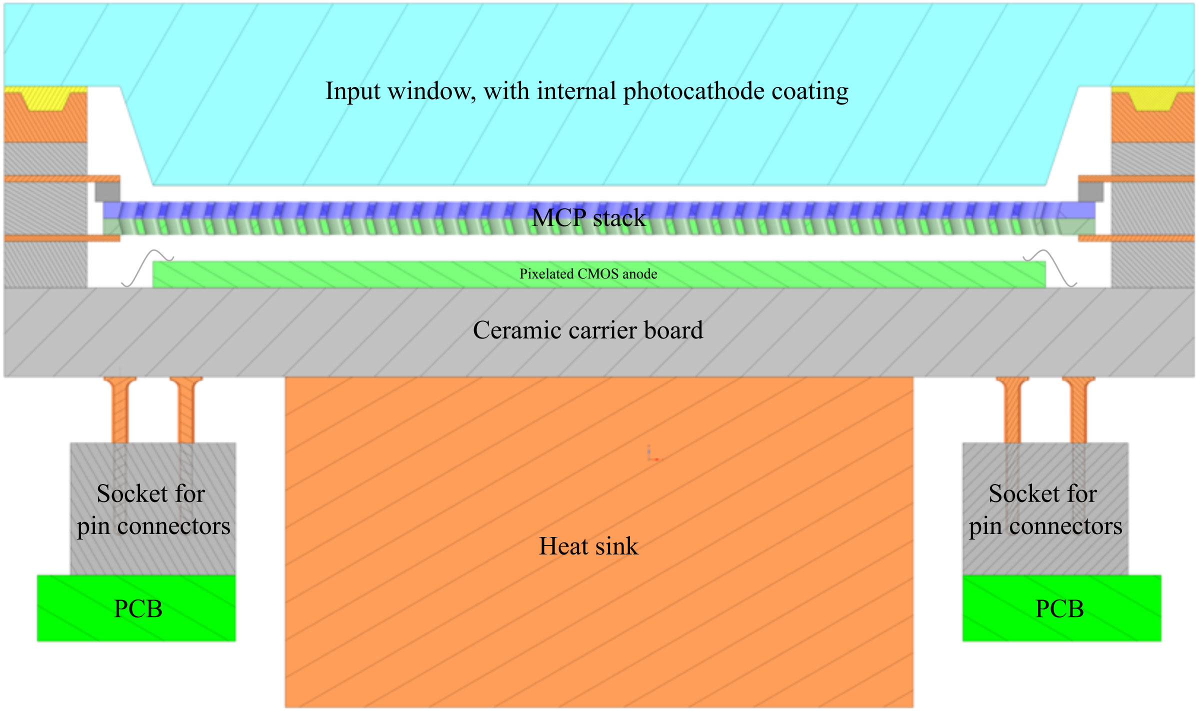


- Vacuum-based detector
  - Assembly of many components under high vacuum (~10^{-10} mbar)
  - High-speed connections through pins in ceramic carrier board
- Heat sink for stable detector operation (~5 W heat removal)
- Carrier printed circuit board (PCB)
  - Socket for detector pins, regulators and high voltage
  - Connected to FPGA-based read-out and DAQ via 16 × 10 Gbps links

Detector geometry

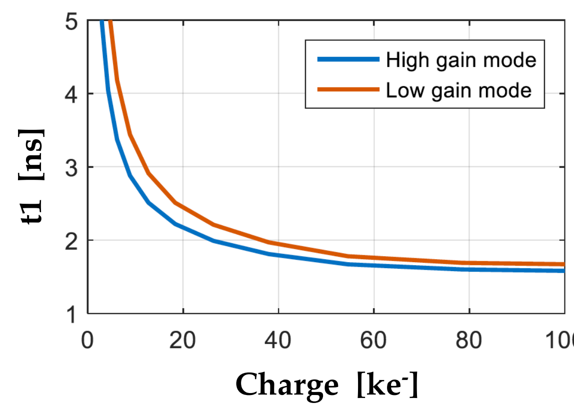


- Shortest photocathode-to-MCP distance preserves impact position information
- Optimized MCP-to-anode distance spreads the electron cloud over a number of pixels

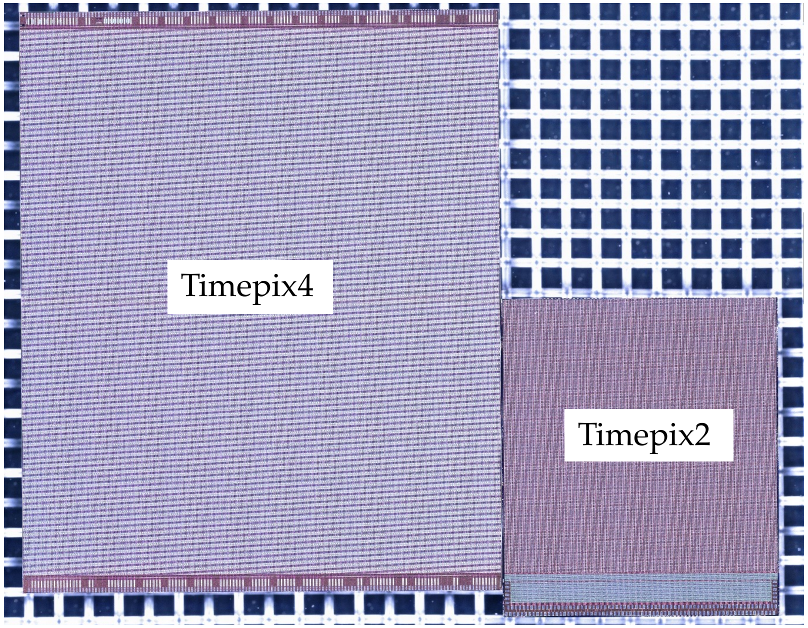
Pixelated anode

- Timepix4 ASIC in 65nm CMOS **silicon pixel technology**
  - Developed and produced by the Medipix4 Collaboration for hybrid pixel detectors
- Charge sensitive amplifier, single threshold discriminator and TDC based on Voltage Controlled Oscillator
  - 4-side buttable (TSV)
  - Data-driven and frame-based read-out

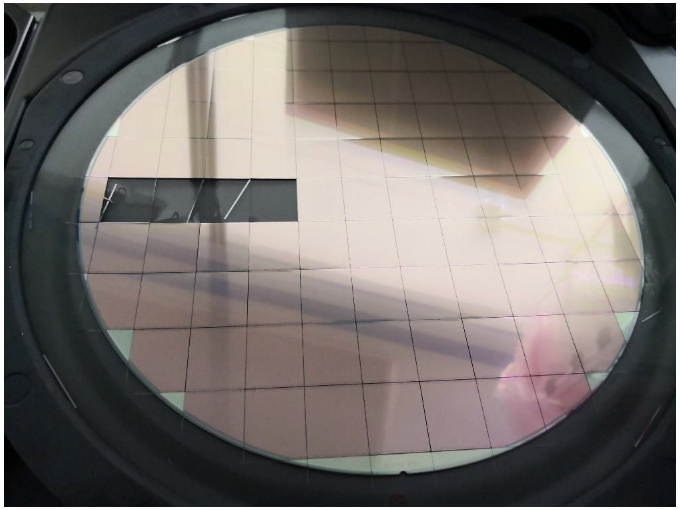
Technology			**CMOS 65 nm**
Pixel Size			55 μm × 55 μm
Pixel arrangement			4-side buttable 512×448 (0.23 Mpixels)
Sensitive area			6.94 cm² (2.82 cm × 2.46 cm)
Read-out Modes	Data driven	Mode	TOT and TOA
		Event Packet	64-bit
		Max rate	358 Mhits/cm²/s
TDC bin size			**195 ps**
Readout bandwidth			≤163.84 Gbps (16× @10.24 Gbps)
Equivalent noise charge			50-70 e⁻
Target global minimum threshold			<500 e⁻



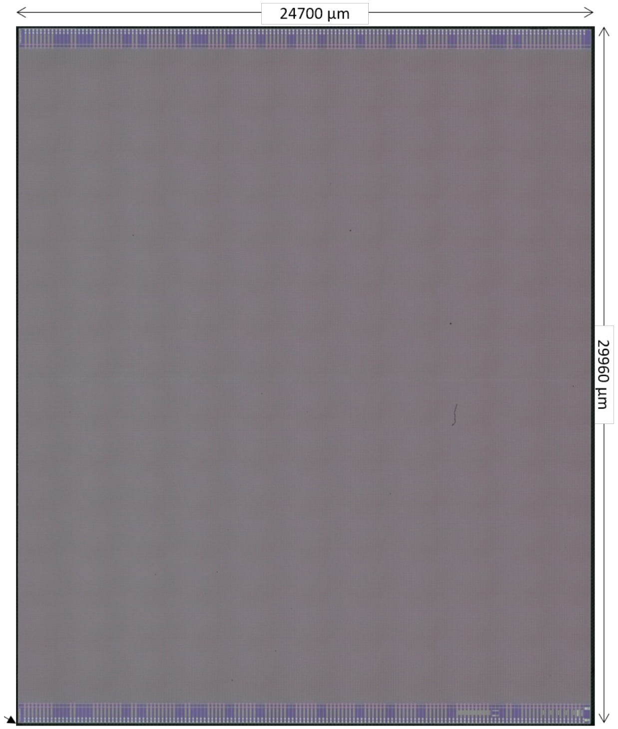
The Timepix4 ASIC



- 65 nm CMOS (TSMC)
- ASIC productions:
  - Timepix4_v0 (Q1 2020)
  - Timepix4_v1 (Q4 2020)
  - Timepix4_v2 (Q4 2021)

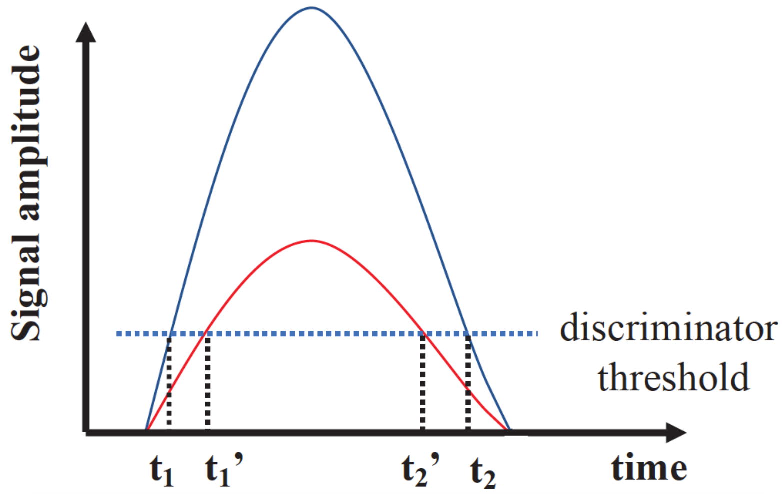


X. Llopart (CERN)



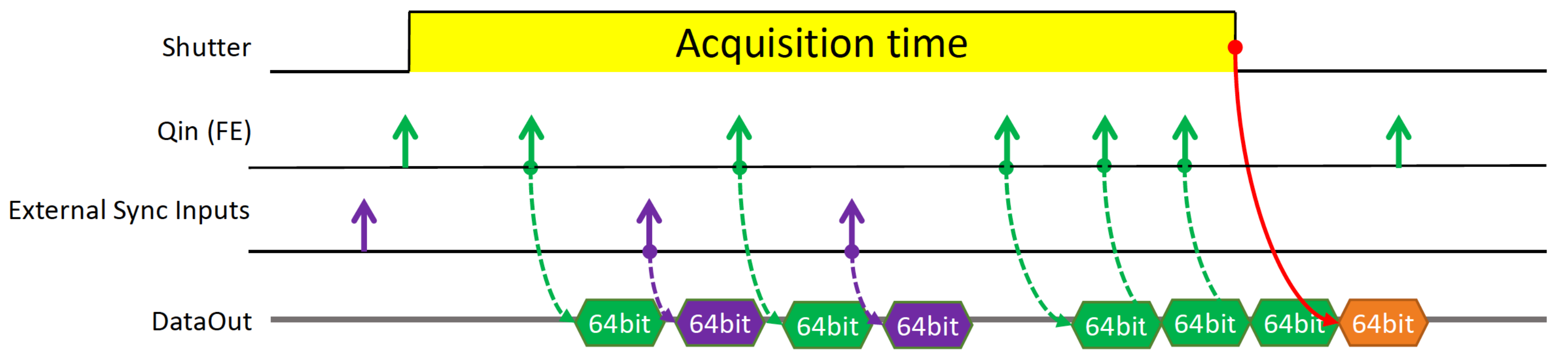
Timepix4 hit data

- Measures arrival time (t_1) and Time-over-Threshold ($ToT=t_2-t_1$)
  - TDC bin size: 195 ps (56 ps r.m.s. resolution per pixel)
- Electron cloud spread over a number of pixels → cluster
- Use ToT information (proportional to the charge in a pixel) to:
  - Correct for time-walk effect in every pixel
  - Improve **position resolution** by centroid algorithm
    - Go from $55\mu m/\sqrt{12}$~$16\mu m$ down to **5μm**
  - Improve **timing resolution** by multiple sampling
    - Many time measurements for the same photon → **few 10s ps**



Timepix4 data-driven read-out

- Zero-suppressed continuous data-driven
  - Output bandwidth from 40 Mbps (2.6 Hz/pixel) to 160 Gbps (10.8 KHz/pixel)
- 4 external inputs to synchronize/align external signals with data



SPEC: Packet specifications ToA/ToT				
Name	Width	MSB	LSB	Bits
Top	1	63	63	[63:63]
EoC	8	62	55	[62:55]
SP	6	54	49	[54:49]
Pixel	3	48	46	[48:46]
ToA	16	45	30	[45:30]
ufToA_start	4	29	26	[29:26]
ufToA_stop	4	25	22	[25:22]
fToA_rise	5	21	17	[21:17]
fToA_fall	5	16	12	[16:12]
ToT	11	11	1	[11:1]
Pileup	1	0	0	[0:0]

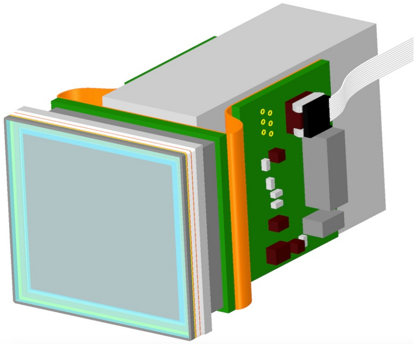
Address: 18 bits

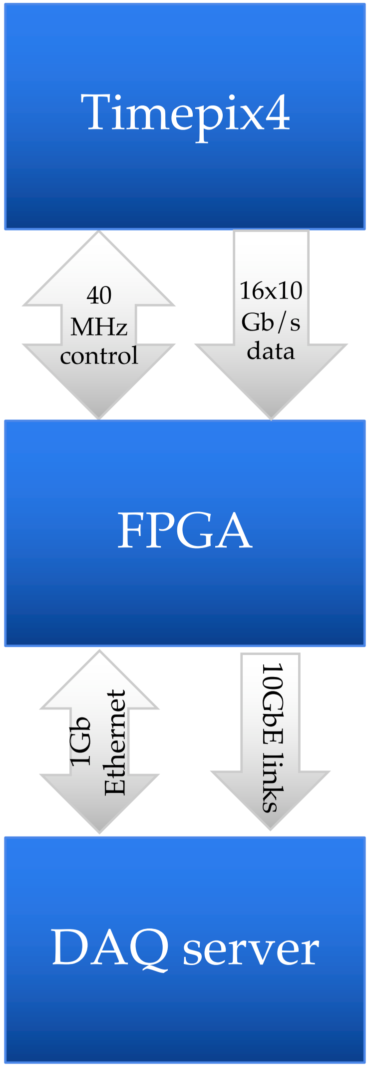
Time: 29 bits

Energy: 21 bits

Electronics and DAQ

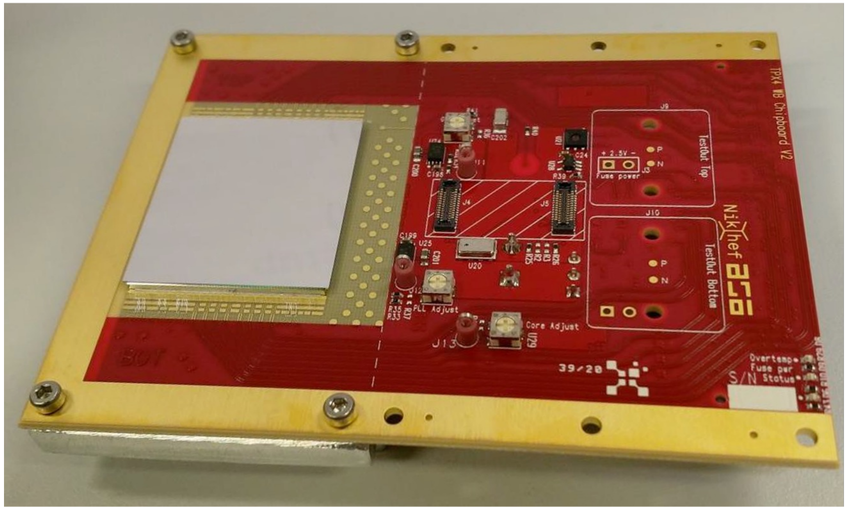
- On-detector electronics
  - Timepix4 ASIC
  - Electro-optical transceivers will link the ASIC to an FPGA-based board for the exchange of configuration (slow control) and the collection of event data
  - Regulators, etc.
- Off-detector electronics
  - FPGA far from detector
- The FPGA performs serial decoding and sends the data to a PC for data analysis and storage using fast serial data links

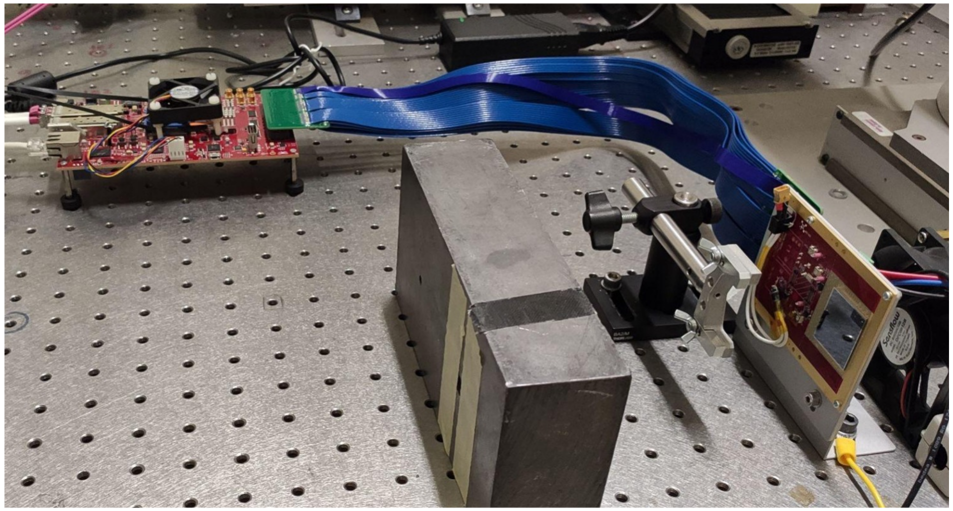




Current test system

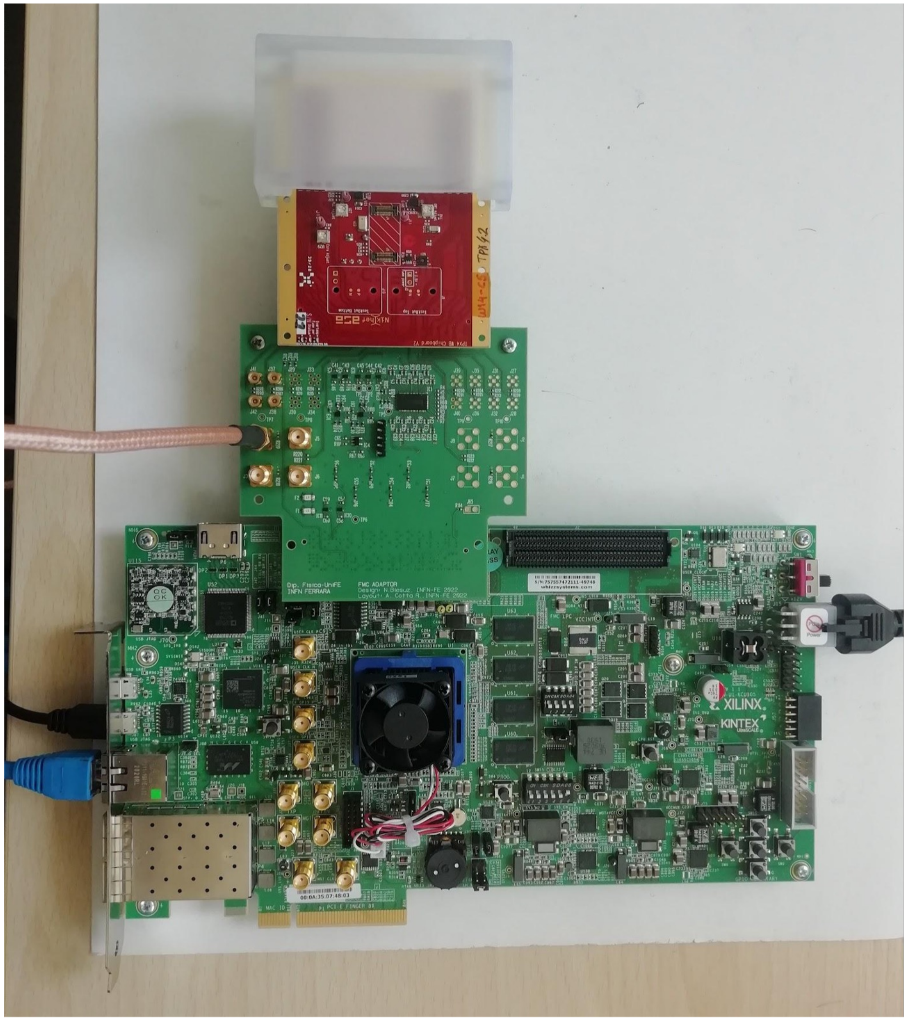
- Timepix4 bump-bonded to 300 μm thick silicon sensor
- SPIDR4 FPGA read-out system and sensor carrier board
  - Developed by Nikhef Medipix4 group





- Dedicated DAQ system under development

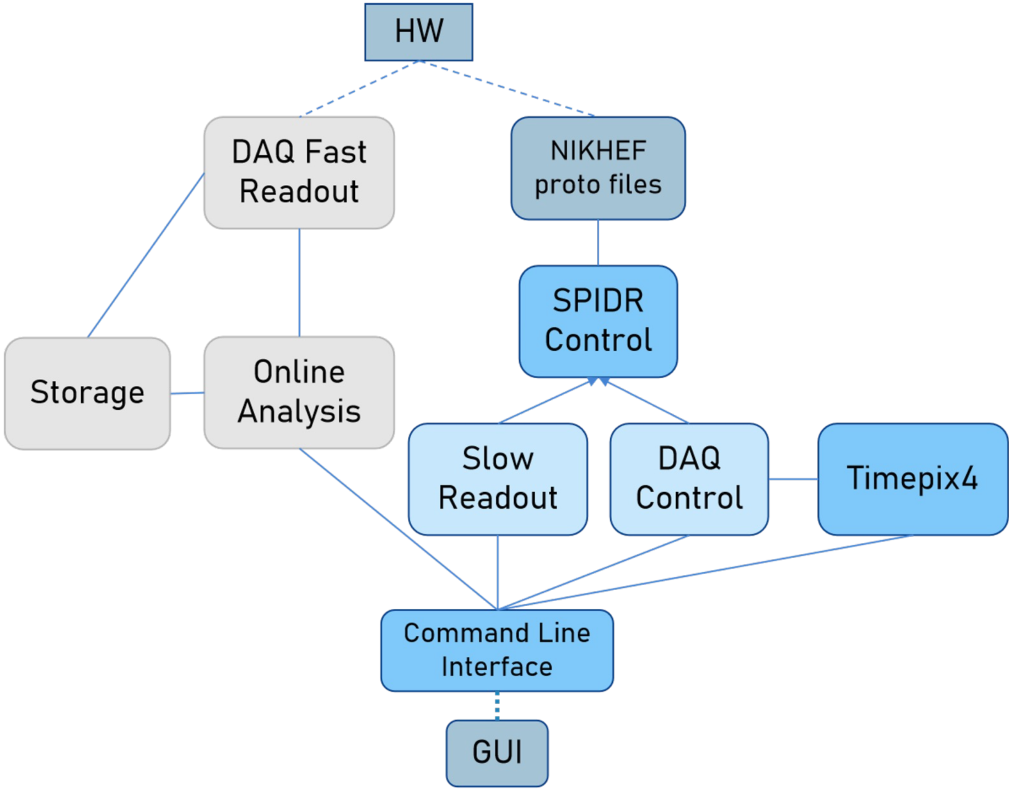
DAQ system under development



- System prototype
  - Based on Xilinx KCU105
  - Slow control (1 GbE)
  - Data stream (10 GbE)
- Status:
  - Dev Kit firmware in debug
  - Started work on high-speed communication
- Chipboard to Dev Kit adapter produced

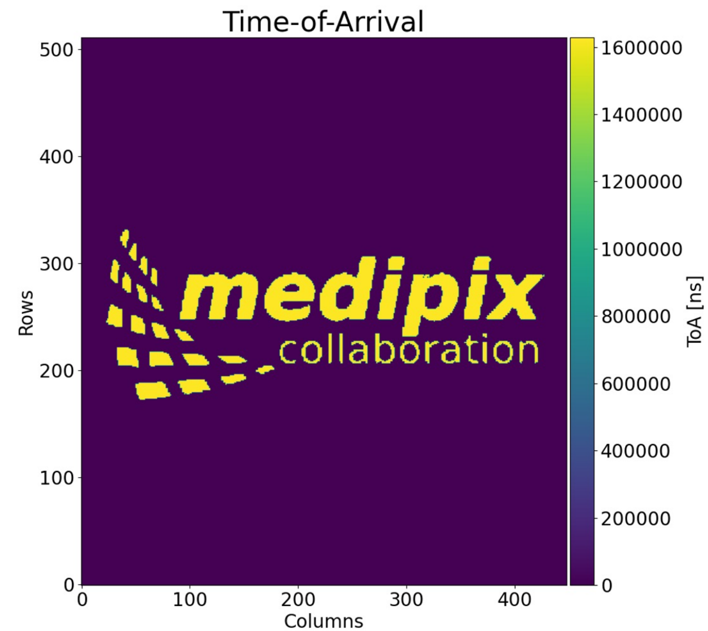
Software

- Dedicated software under development
- C++ based
  - Low-level
  - Object-oriented
- Readout and Control in unique CLI
- Read and Write register functions
- Application Programming Interfaces for Timepix4
- Packets decoder

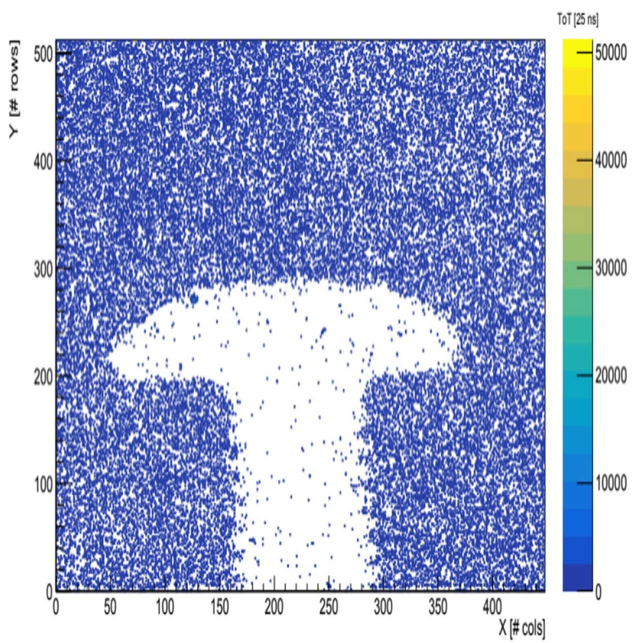


Measurements with Timepix4

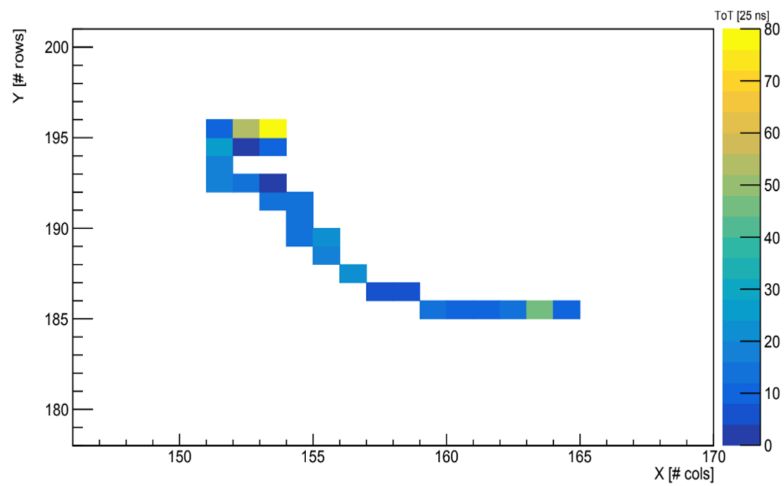
- Digital test pulse:
  - Correct patterns, number of pulses and ToA-ToT
- Radioactive sources measurement:
  - Density based clustering (DBSCAN)
  - Preliminary ToT-charge calibration



^{241}Am

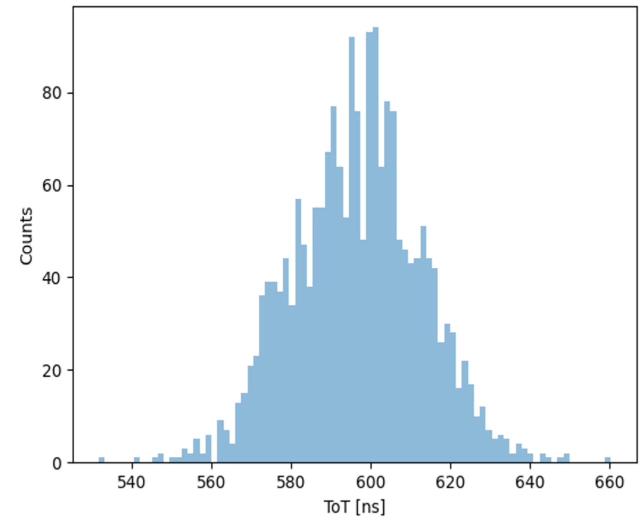


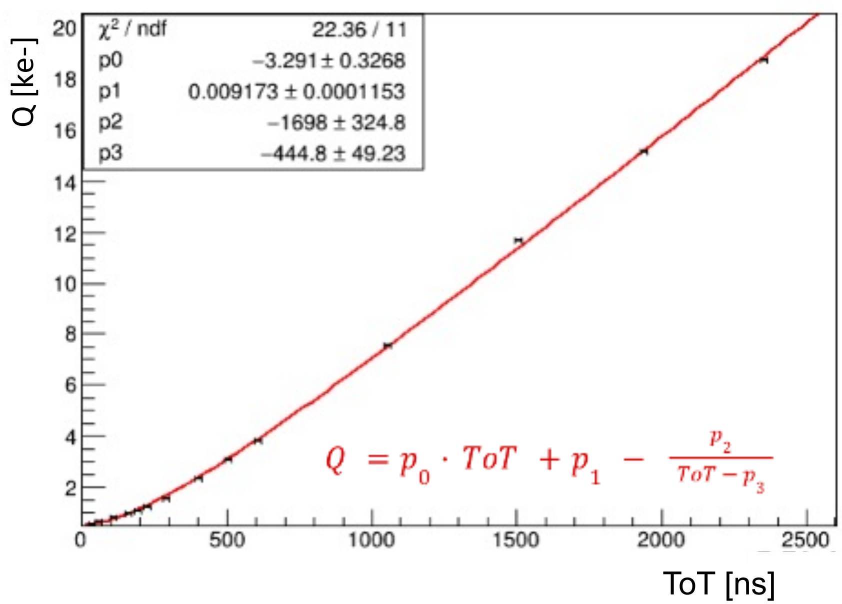
^{90}Sr



Measurements with Timepix4

- Analog test pulse:
  - Expected ToT gaussian distribution at fixed values of the test pulse voltage
  - Average ToT changes accordingly to the set voltage
  - Per-pixel ToT calibration through test pulse over the whole pixel matrix
  - Calibration validated using radioactive sources
- Next steps
  - Timing and spatial resolution measurement using digital pixels and laser setup





Detector advantages

- Advantage of the proposed device:
  - 5-10 μm position resolution
  - High granularity (55 μm × 55 μm) and rate capabilities (2.5 Ghits/s) for applications with large detector occupancies
  - <100 ps resolution per single photon excellent handle for pattern recognition and time-association of the individual photons
  - Negligible detector-related background (DCR) at room T
    - Can be further reduced with cooling
  - Robust in magnetic fields
  - Longer lifetime compared to standard applications due to low gain
  - On-detector signal processing and digitization with large number of active channels (~230 k pixels), with limited number of external interconnections (~200)

Project status

- Electronics
  - Timepix4: v2 bare ASIC extensively tested; first tests with Si sensor in summer 2022
    - Detailed study of ASIC performance and calibrations
    - Calibrations with radioactive sources and test pulses
    - Power measurements and cooling system development
  - Development of FPGA-based control board
    - Firmware almost complete
- C++ software development for ASIC configuration, DAQ and analysis
- Ceramic carrier studies
  - Engineering mock-ups
  - Thermal simulation and measurements
  - Simulation of effects of ceramics on 10 Gbps lines (signal integrity)
  - Components connection

Summary

- A detector for visible single photons, based on a bare Timepix4 CMOS ASIC embedded in a vacuum tube with a MCP is under development for the detection of up to 10^9 photons/s with simultaneous measurement of time and position with excellent resolutions
  - Fully exploit both timing and position resolutions of a MCP
  - High-performance data acquisition (up to 160 Gbps)

- The presented single-photon imaging technology could enable discovery in different fields of science
  - High-energy physics, life sciences, quantum optics, etc.

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European Research Council


THANK YOU
FOR YOUR ATTENTION
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