

# **Module 2 CRS Performance Update**

December 2, 2022

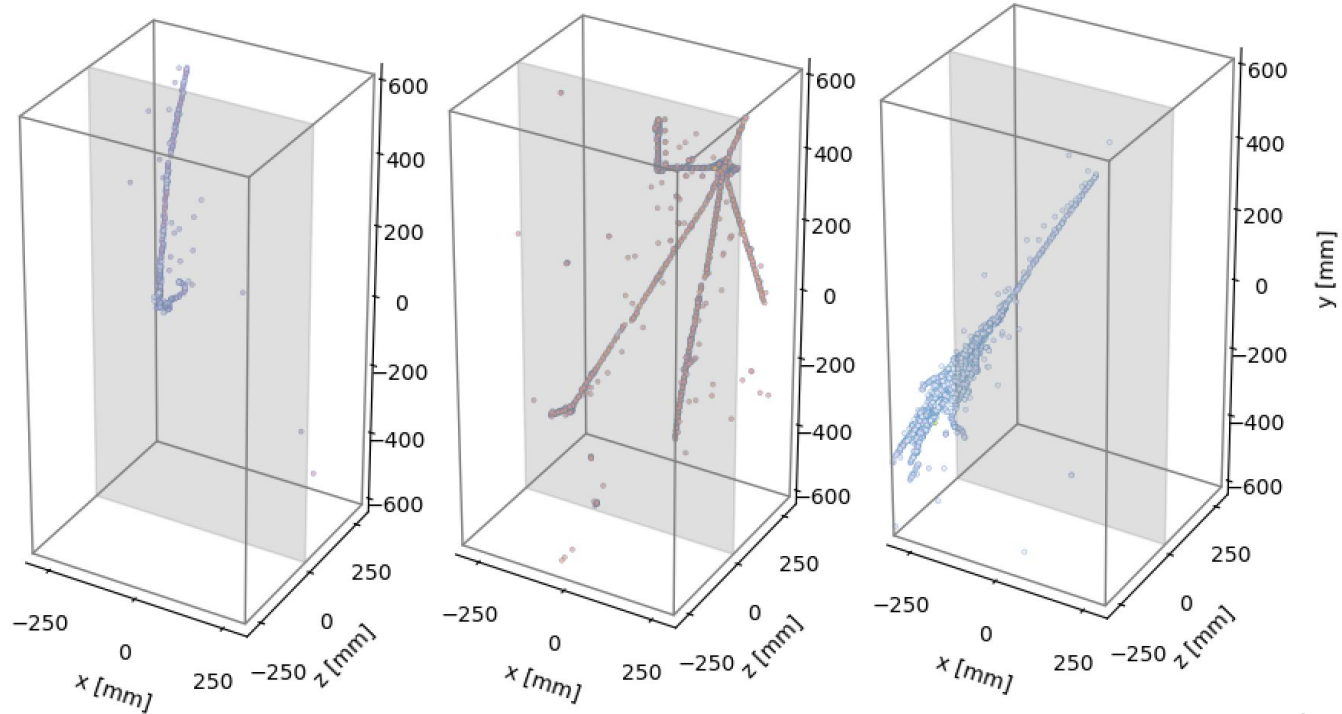
Stephen Greenberg

# Overview

- As of yesterday evening (Bern time), stable self triggering with 55-60 mV 'target' thresholds
- Quality appears to be good
  - Stable packet rate
  - Low rate of 'hot channel' emergence
- **Mainly operational considerations limiting thresholds for now**
  - Difficulty enforcing ASIC considerations with noisy channels

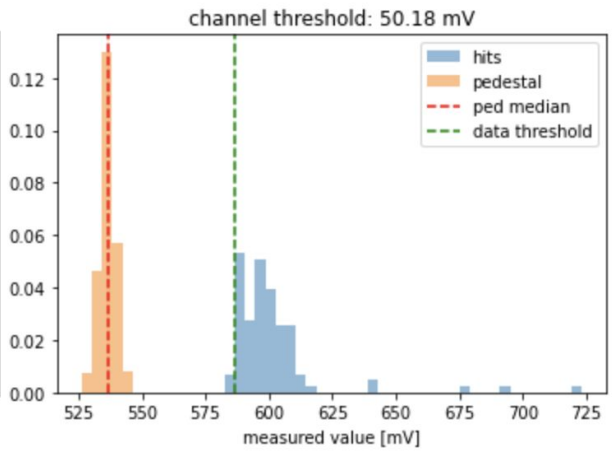
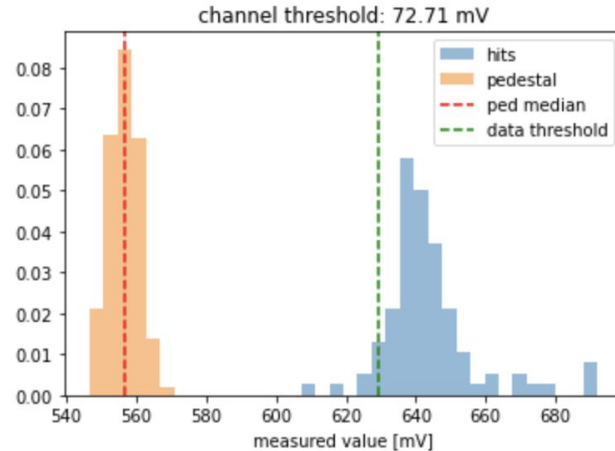
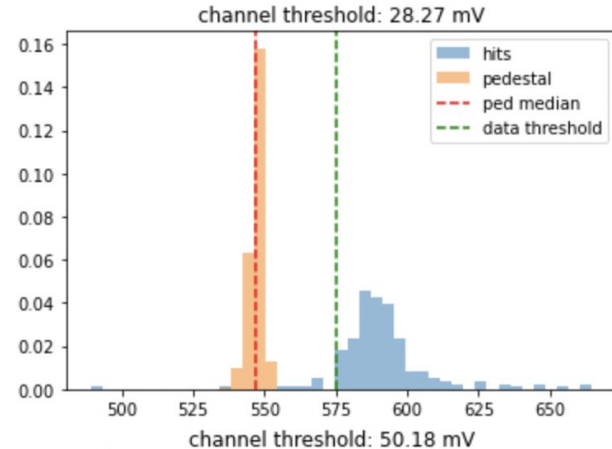
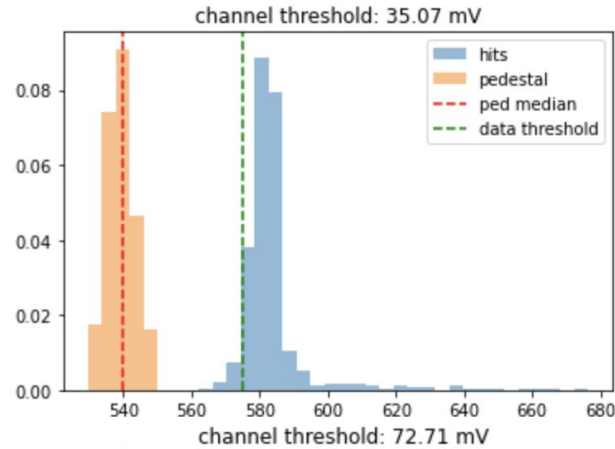
Operating at 64 (rolling)  
periodic reset cycles

## Events from 55 mV Threshold Run 12/02/2022



# Approximate Threshold Extraction

- Threshold extraction done on channel-by channel basis
- Take packet threshold to be 5th percentile of dataword from packets
- Define threshold as difference between packet threshold pedestal median on a given channel

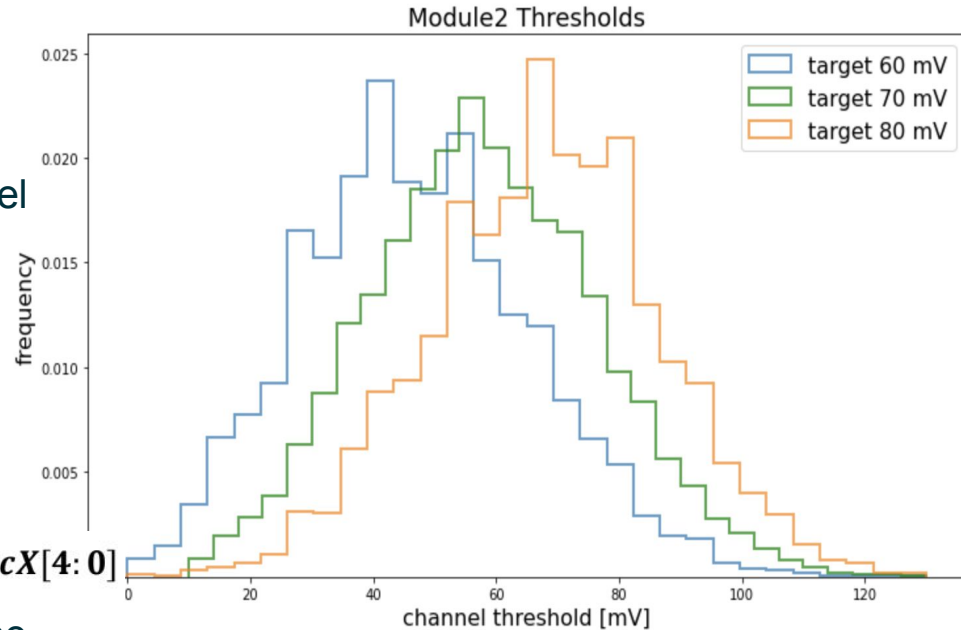


# Target Threshold Accuracy

- Target threshold is converted to `global_threshold` and `pixel_trim_dac` on channel by channel basis
- **Conversion difficulties:**
  - Conversion of `global_threshold` and `pixel_trim_dac` based on simulation of front end, known to be unreliable at cold due to mismatch

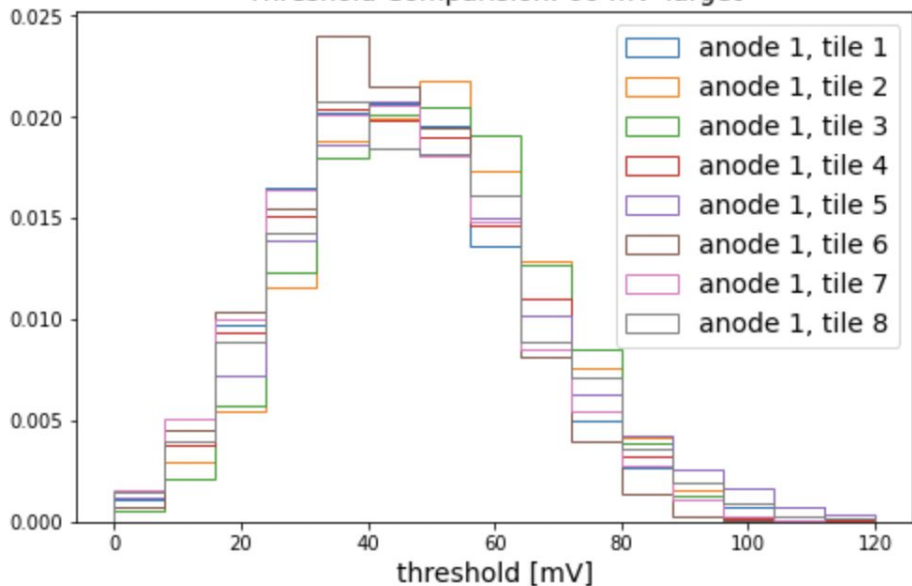
$$Th_{chan\_88K_X} = Th_{Gl} + 465\text{ mV} + 2.34\text{mV} * \mathbf{pixel\_trim\_dacX[4:0]}$$

- Threshold offset estimated from data to be closer to ~350 mV, some variation between ASICs possible.
  - *Using this offset when setting thresholds*
- 'Target' threshold appears to be an OK (but conservative) estimate of actual thresholds

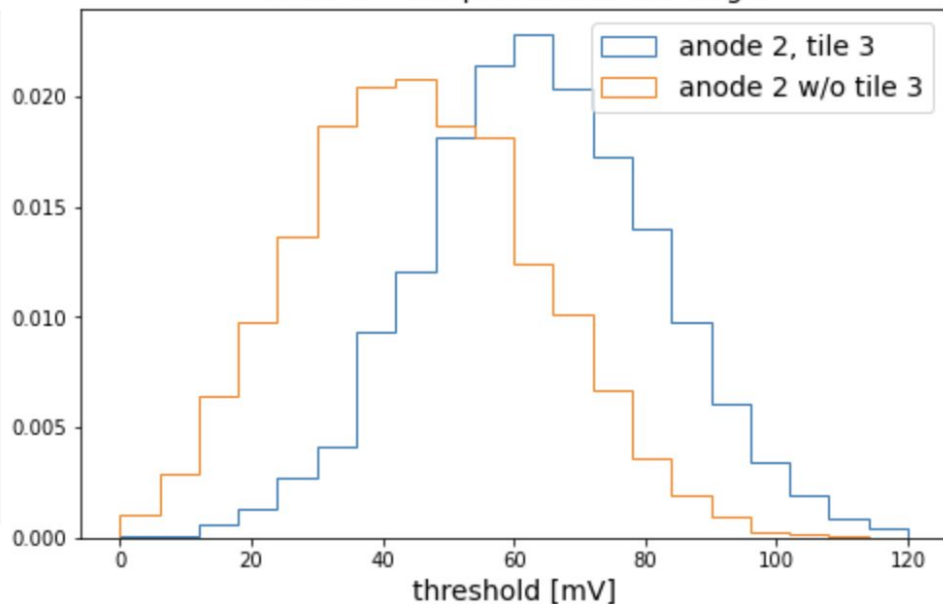


# Tile-by-tile Threshold Variation

Threshold Comparison: 60 mV Target



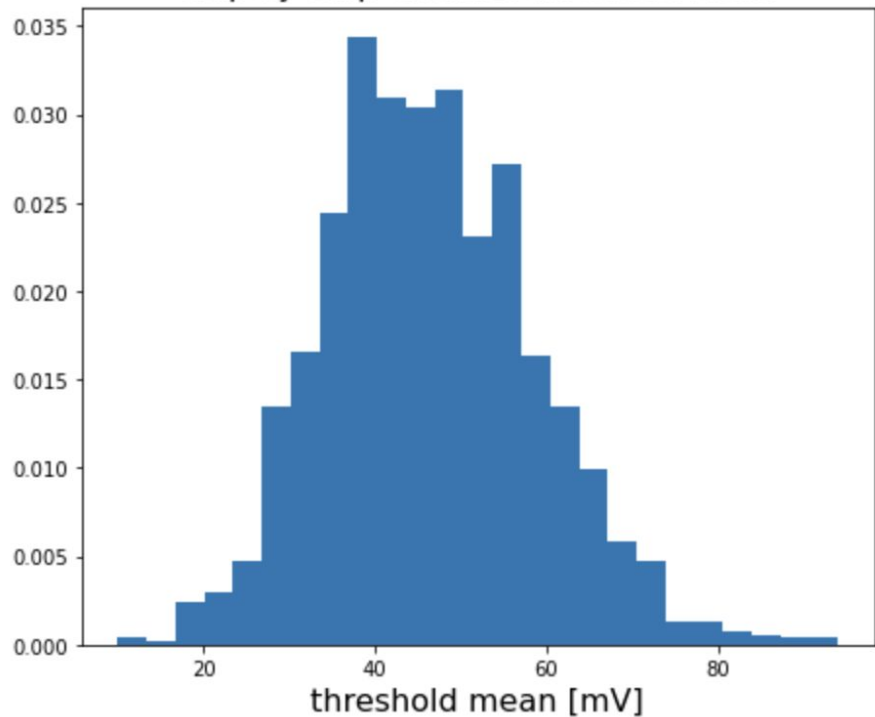
Threshold Comparison: 60 mV Target



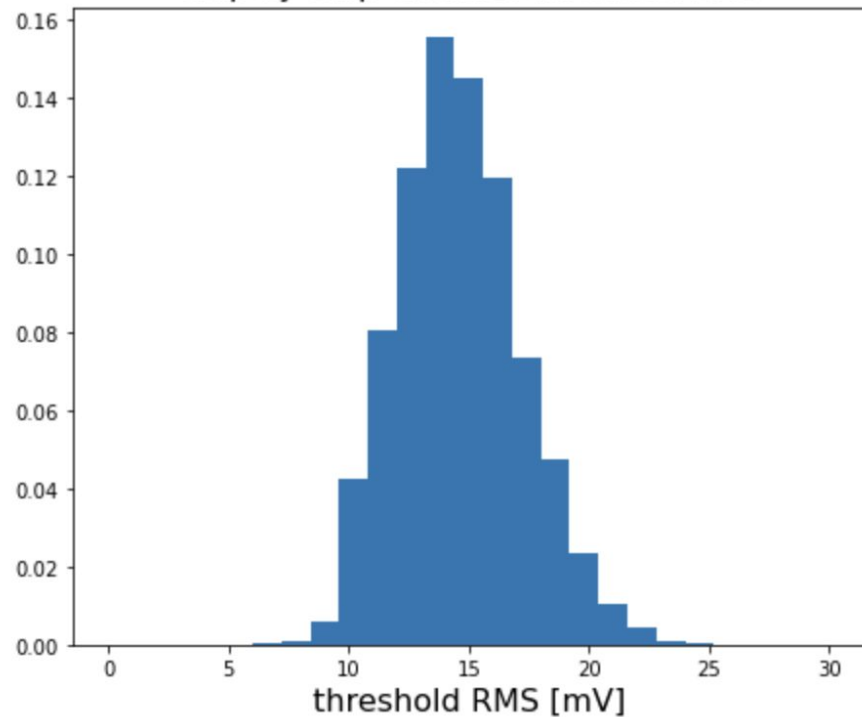
# Chip-by-chip Threshold Variation

*Coming soon: anode map of thresholds*

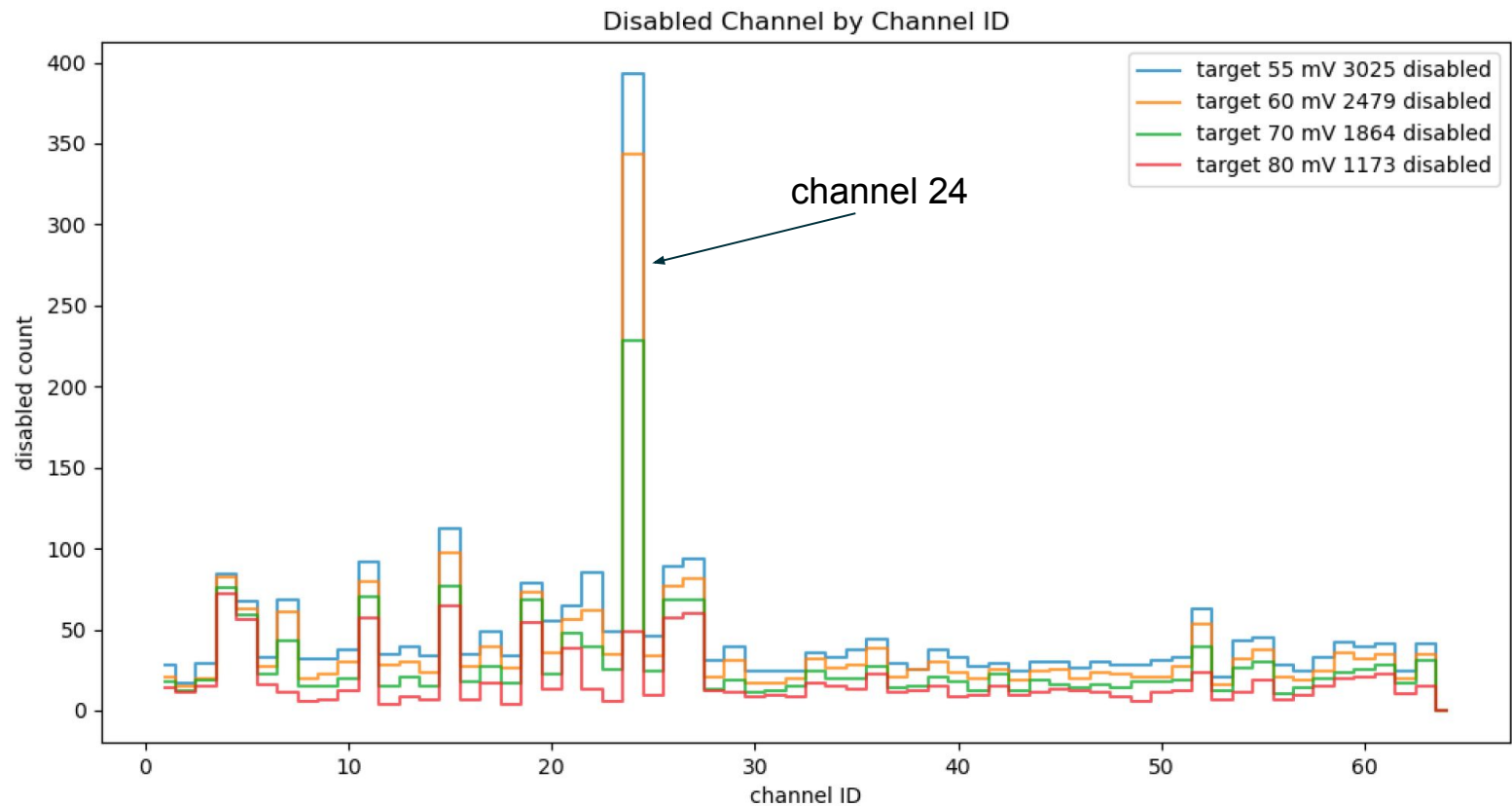
Chip by Chip Channel Threshold Mean



Chip by Chip Channel Threshold RMS

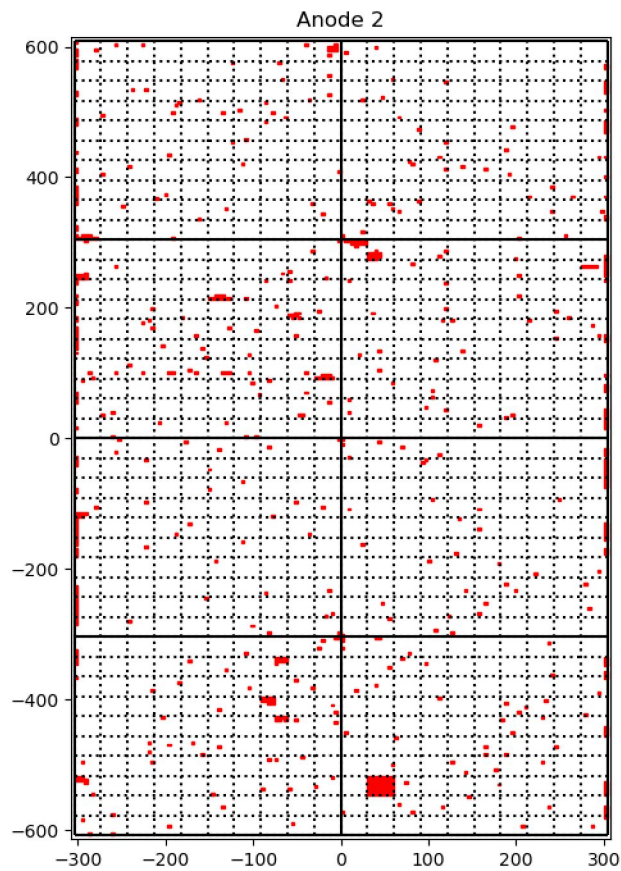
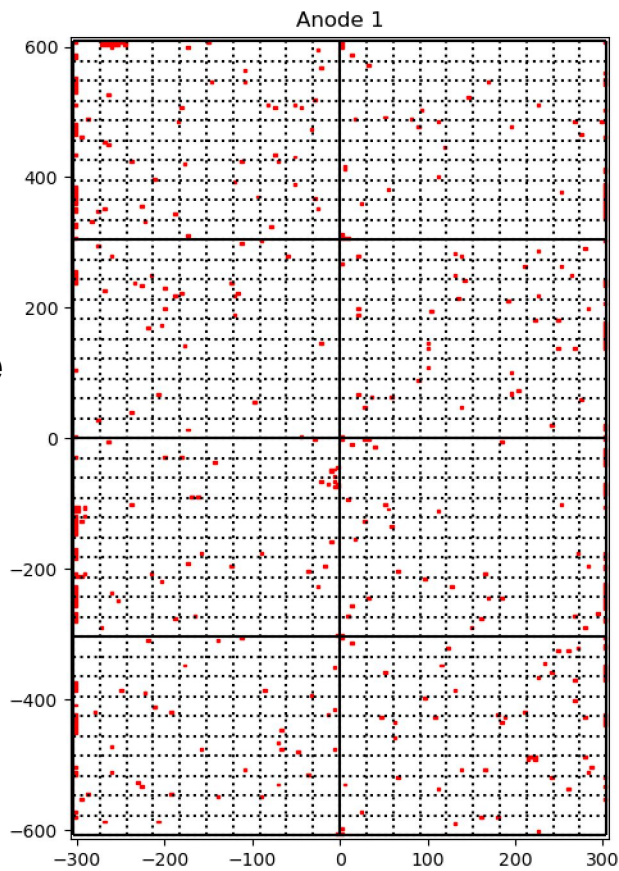


# Disabled Channel Breakdown



# Target 80 mV Disable Map

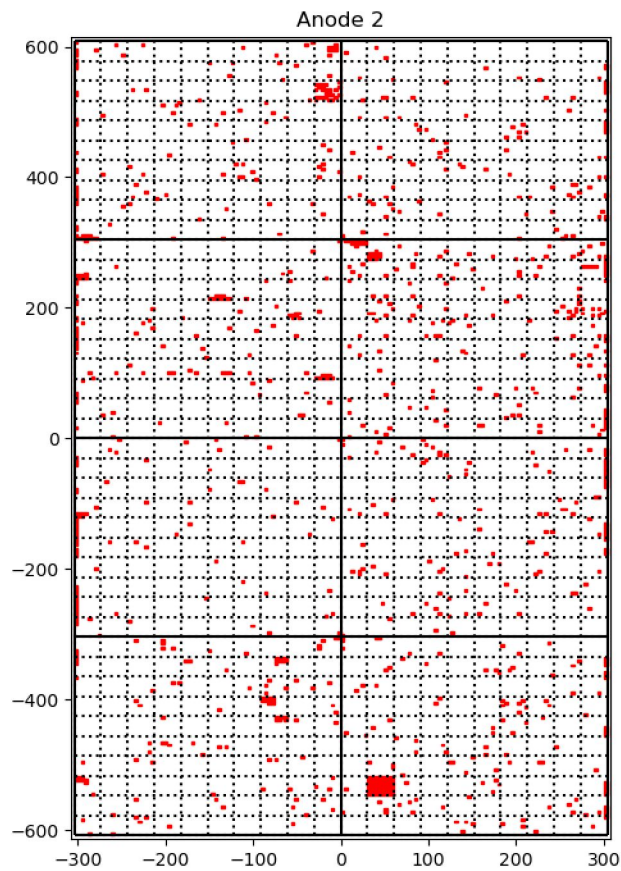
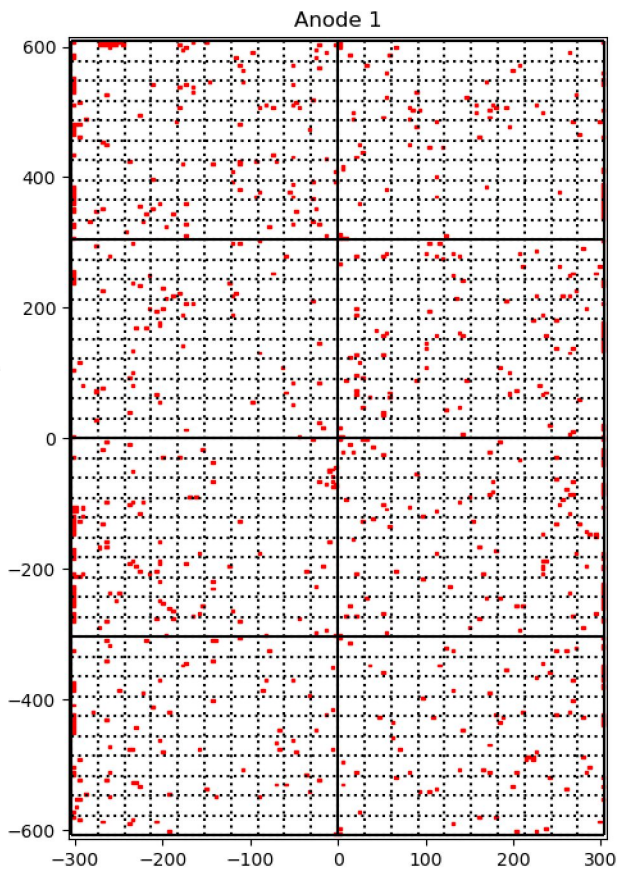
**98.9% Active**





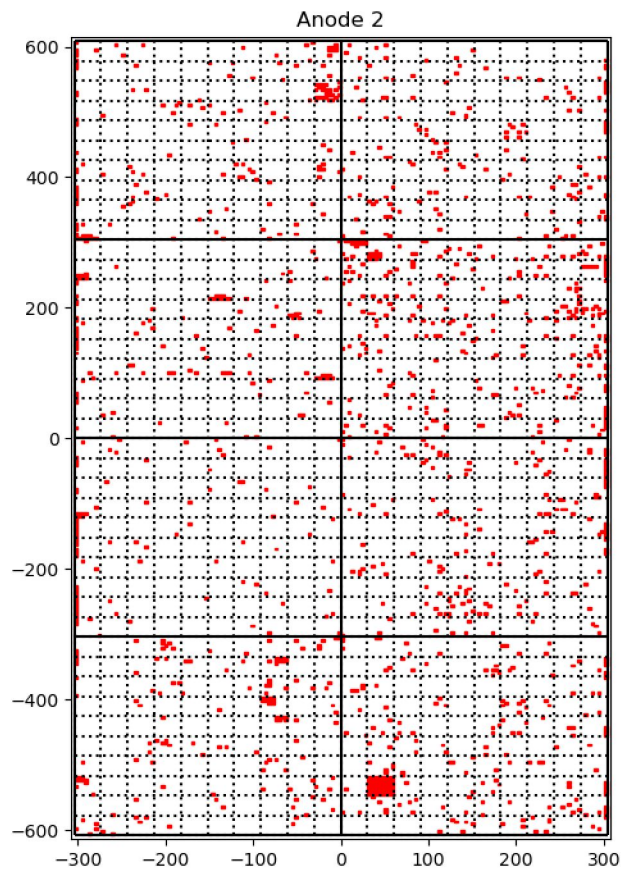
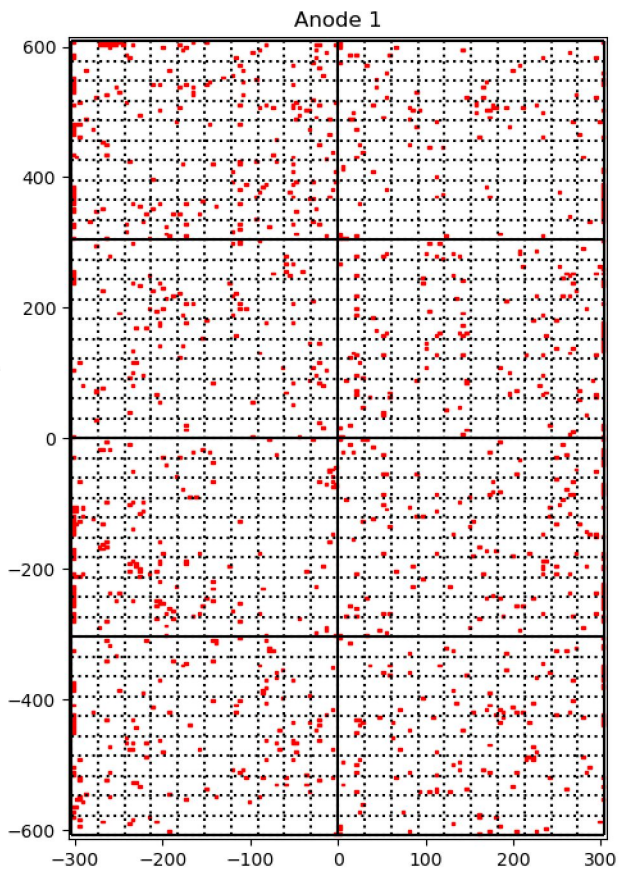
# Target 70 mV Disable Map

98.2% Active



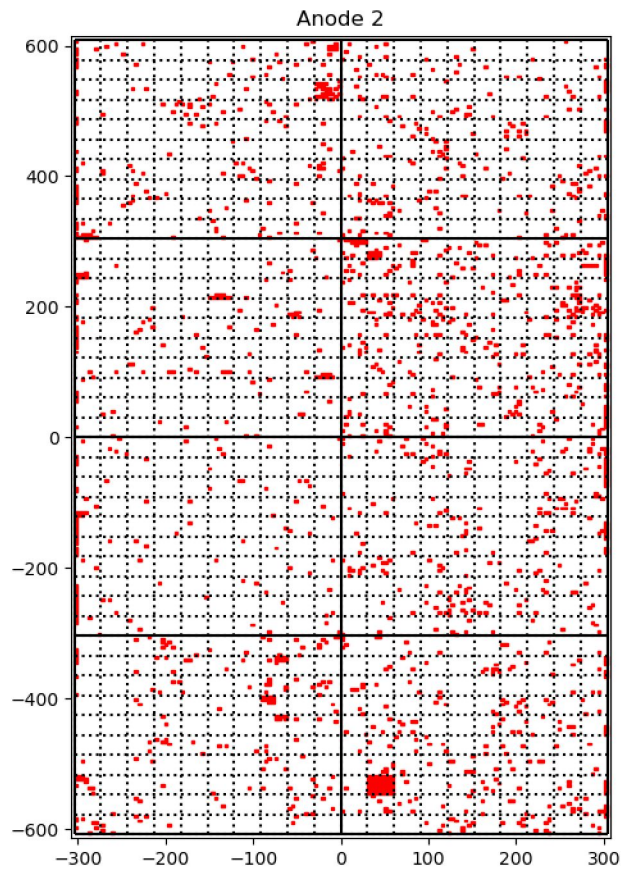
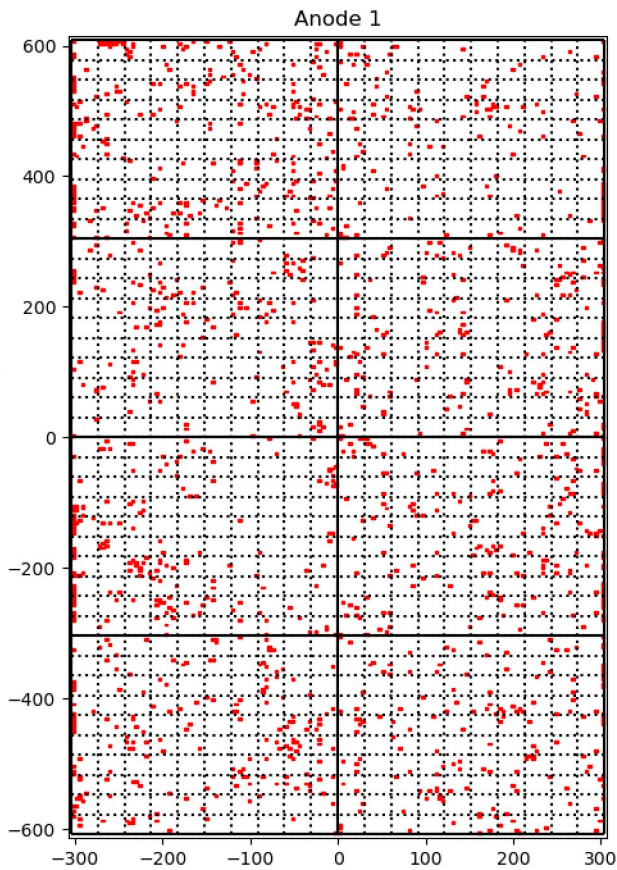
# Target 60 mV Disable Map

**97.6% Active**



# Target 55 mV Disable Map

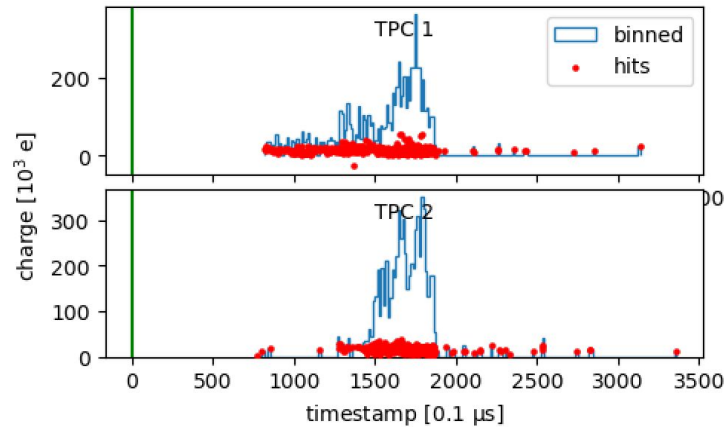
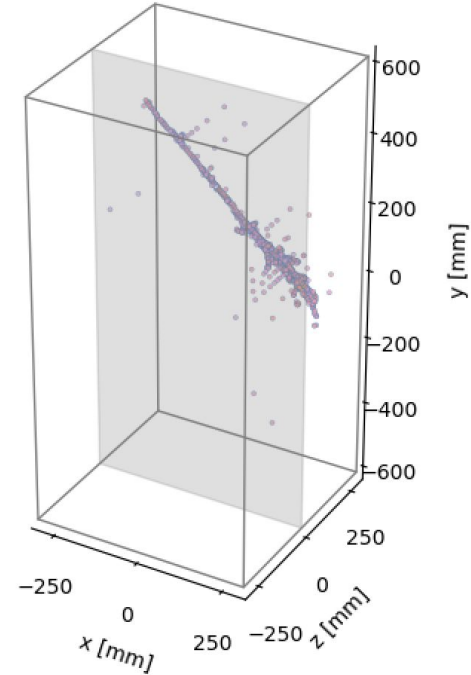
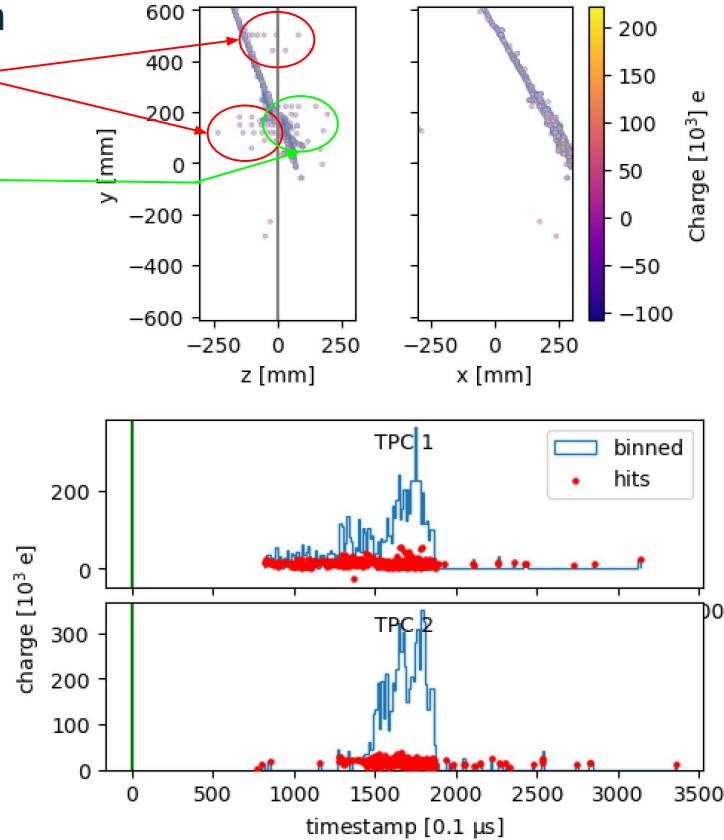
**97.1% Active**



# Hit-Correlated Noise

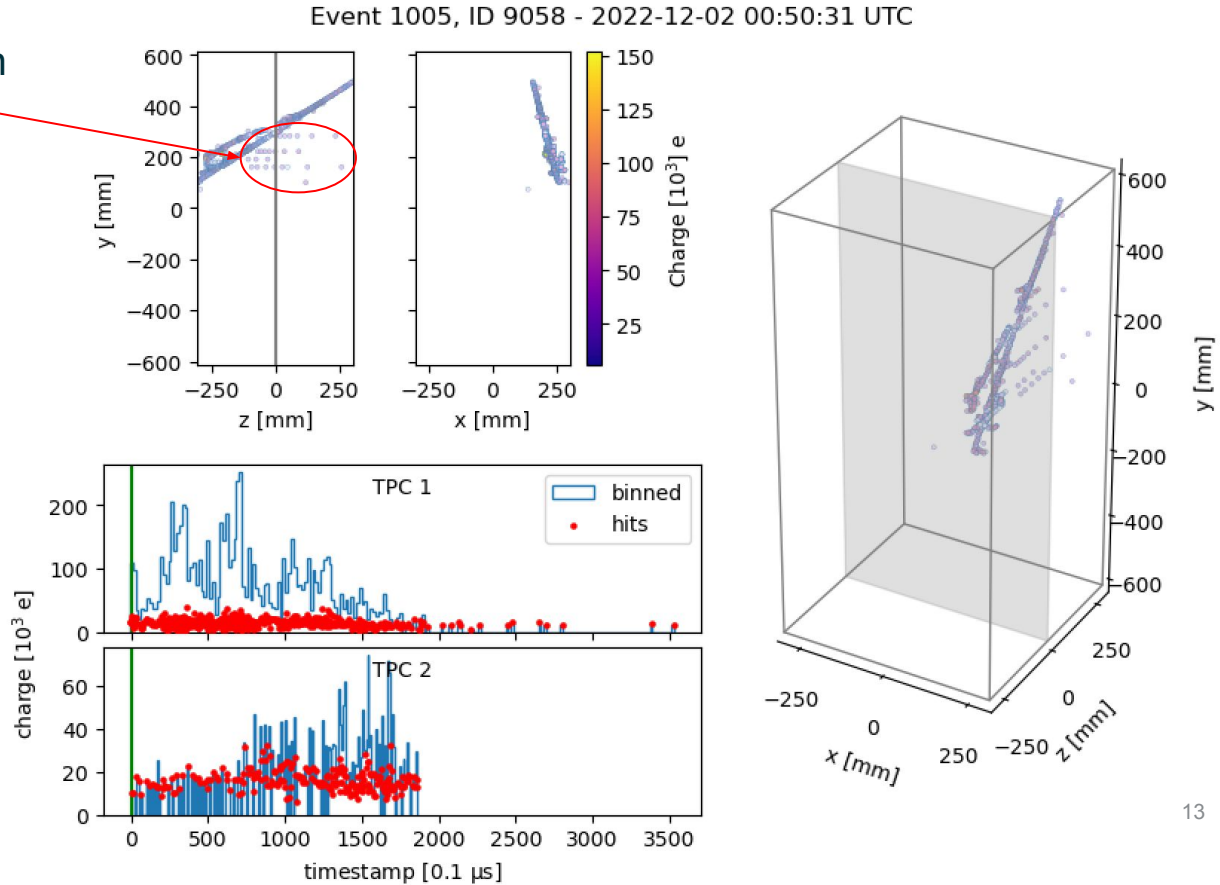
- ‘After-pulse’ like hits–noise on individual pixels after seeing charge
- Far-field induced hits

Event 1021, ID 9173 - 2022-12-02 00:50:32 UTC



# Hit-Correlated Noise

- ‘After-pulse’ like hits—noise on individual pixels after seeing charge
- Far-field induced hits



# Operational Challenges in Lowering Thresholds

- Difficulty dynamically disabling channels when attempting to lower thresholds
  - Noisy channels filling FIFOs on upstream chips prevent configuration packets from reaching entire hydra network
  - Work around—hard reset+reconfigure, takes ~20 minutes
- DAQ machine memory consumption
  - When data rate is too high, DQM and hot channel identification takes >10-20 mins
  - Makes automatic hot-channel identification very difficult

## Potential solution to be implemented:

- Disabling downstream receivers on chips in network of noisy channel when attempting to disable channels to stop FIFO from filling
  - If FIFO is full on other chips in network, this may fail

# Summary and Next Steps

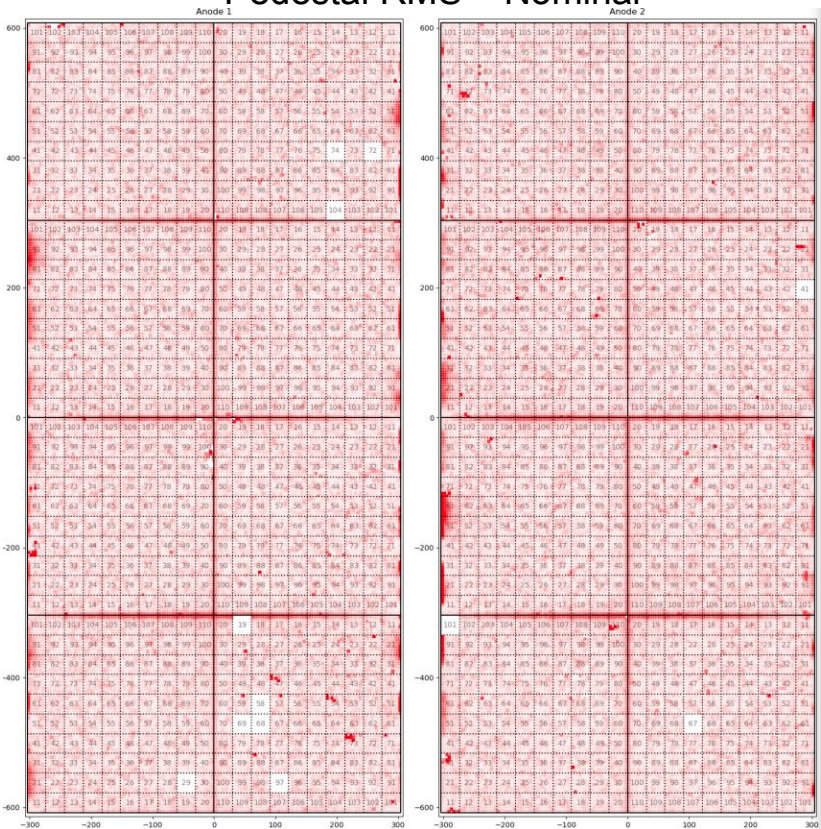
- **Summary**
  - Microphonics noise issues resolved in Run 2 (see backups), allows for lower, stable thresholds
  - Stable cosmic data at 55 and 60 mV target thresholds (cosmics and HV studies)
- **Next steps:**
  - Time permitting until the end of the run, iron out operational issues and lower thresholds
  - Extensive cosmic data taken at lowest stable thresholds, +2000e-, +4000e-
  - Alternative, data driven threshold extraction using leakage-induced trigger rate

# Backup

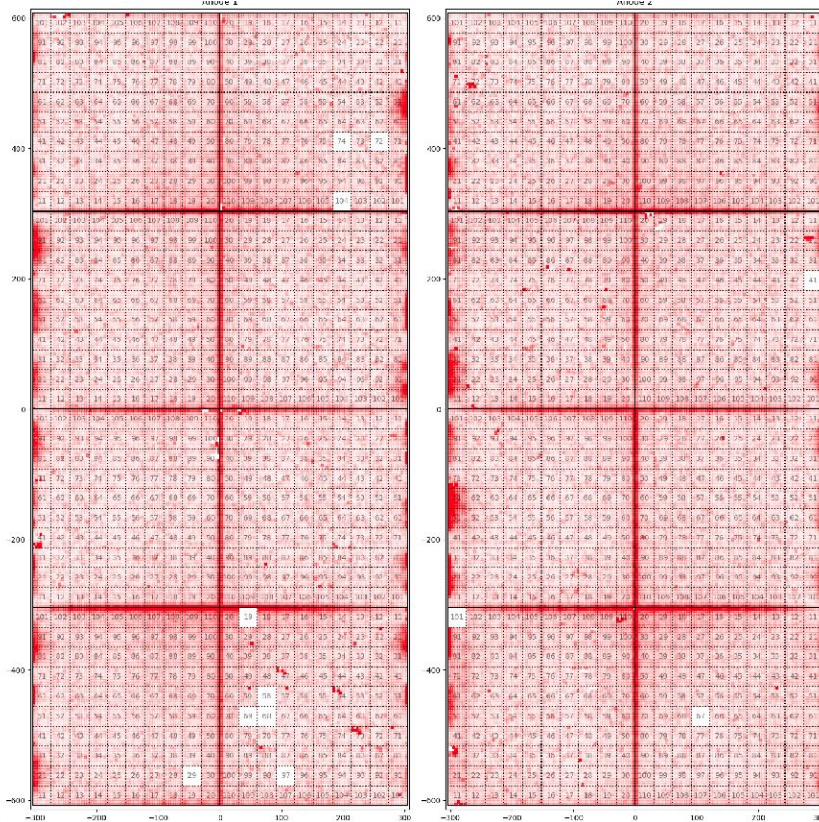


# Run1 Noise Around E-board, Tile Boundaries

## Pedestal RMS – Nominal



## Pedestal RMS – Induced Vibration



# Microphonics Resolved

