**PIP-II AccU-BSTR -Dampers-CHG0 DAQ Network Specifications**

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Document Approval

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Table of Contents

[1. Purpose 4](#_Toc102057330)

[2. Scope 4](#_Toc102057331)

[3. Acronyms 5](#_Toc102057332)

[4. Reference Documents 6](#_Toc102057333)

[5. System ArChitecture Summary 7](#_Toc102057334)

[6. Booster Electronics Chassis 7](#_Toc102057335)

[6.1. Overview 7](#_Toc102057336)

[6.2. Transition Module 10](#_Toc102057337)

[6.2.1. Digital I/O Logic 11](#_Toc102057338)

[6.2.2. Analog Signal Conditioning Circuity 11](#_Toc102057339)

[6.2.3. Signal Digitization and Buffering 12](#_Toc102057340)

[6.2.4. Digital Signal Processing 12](#_Toc102057341)

[6.2.5. Ethernet Communication 13](#_Toc102057342)

[7. DAQ COMMUNICATION PROTOCOL 14](#_Toc102057343)

[**7.1.** Configuration and Subscriber Information 14](#_Toc102057344)

[**7.2.** Redis Stream Specifications 14](#_Toc102057345)

[**7.3.** Redis Pub/Sub Specifications 14](#_Toc102057346)

[7.4. Redis Lists and Sorted Sets Specifications 14](#_Toc102057347)

[8. Front End Server 14](#_Toc102057348)

[8.1. Overview 14](#_Toc102057349)

[8.2. Control System Device Properties 15](#_Toc102057350)

[8.3. Diagnostic Data Device Properties 15](#_Toc102057351)

# Purpose

This document describes the details of the firmware and software specifications for the new Booster BCM system of the PIP-II AccU-BSTR -Dampers-CHG0 Task, 121.05.04.04.03 PIP-II Project.

Key cost, schedule, technical and programmatic assumptions are provided in PIP-II Project Assumptions [1]. Interface specifications are upwards traceable to the associated Global Requirements Documents (GRDs)[2], Physics Requirements Documents (PRDs)[3][5], Functional Requirement Specifications(FRSs)[6], and Technical Requirement Specifications(TRSs)[7] where applicable. All specifications shall abide by requirements outlined in Fermilab Engineering Manual (FEM), Fermilab ES&H Manual (FESHM), and Fermilab Radiological Control Manual (FRCM), as appropriate.

# Scope

This document will elaborate on specifications for the signal digitization, firmware modules, and software modules, internal to the Booster BCM system. External interfaces along the new Booster BCM signal path are addressed in the Interface Specification Document (ISD)[8]. Since the external interfaces for this activity are external to the PIP-II project Level 3 Tasks, they aren’t included in the PIP-II MICD[4].

# Acronyms

|  |  |
| --- | --- |
| ACNET | Accelerator Control NETwork |
| AD | Accelerator Division |
| ADC | Analog to Digital Converter |
| BCM | Beam Current Monitor |
| BI | Beam Instrumentation |
| DAQ | Data Acquisition |
| DCCT | DC Current Transformer |
| DDCP | Distributed Data Communication Protocol |
| DSP | Digital Signal Processing |
| EMI | Electromagnetic Interference |
| EPICS | Experimental Physics and Industrial Control System |
| FEM | Fermilab Engineering Manual |
| FESHM | Fermilab ES&H Manual |
| FRCM | Fermilab Radiological Control Manual |
| FRS | Functional Requirements Specification |
| GRD | Global Requirements Document |
| ISD | Interface Specification Document |
| IOC | Input/Output Controller |
| LLRF | Low Level Radio Frequency |
| MFTU | Multi-Function Timing Unit |
| MICD | Master Interface Control Document |
| PRD | Physics Requirement Document |
| QA | Quality Assurance |
| QC | Quality Control |
| REDIS | REmote DIctionary Server |
| RF | Radio Frequency |
| RFI | Radio Frequency Interference |
| TRS | Technical Requirements Specification |

# Reference Documents

|  |  |  |
| --- | --- | --- |
| # | Reference | Document # |
| 1.
 | PIP-II Project Assumptions | PIP-II docDB 144 |
| 1.
 | PIP-II Global Requirements Document (GRD) | ED0001222 |
| 1.
 | PIP-II Parameters Physics Requirements Document (PRD) | ED0010216 |
| 1.
 | PIP-II Master Interface Control Document | ED0010433 |
| 1.
 | PIP-II Booster BCM Physics Requirements Document (PRD) | ED000xxxx |
| 1.
 | PIP-II Booster BCM Functional Requirements Specification (FRS) | ED00xxxxx |
| 1.
 | PIP-II Booster BCM Technical Specification Document (TRS) | ED00xxxxx |
| 1.
 | PIP-II Booster BCM Interface Specification Document (ISD) | ED00xxxxx |
| 1.
 | PIP-II 121.03 Accelerator Systems Quality Assurance (QA) Plan  | PIP-II docDB 4805 |
| 1.
 | PIP-II Beam Instrumentation Quality Control Plan | PIP-II docDB 5520 |
| 1.
 | Multi-Function Timing Unit | docDB 6741 |

# System ArChitecture Summary

To accompany the commerical pickup, the vendor shall provide an 3U tall, 19” wide electronic chassis, 2 power supply modules, and 2 cassette modules. Both cassettes are matched to their associated sensor and cable's length. When a cassette is used with another unmatched sensor, its output shall most likely be unstable and noisy. However, connecting to another sensor does not damage the electronics.

The active cassette modules provide two output signals. An output signal from the active cassette module shall be given to the Booster Signal Distribution box. Another signal from the active cassette module shall be connected to the Booster DCCT Electronics. As shown in Figure 5‑1, the Booster DCCT Electronics shall receive signals from the Booster LLRF as well as Control MFTU.



Figure 5‑1 – External Interfaces to components within the Booster BCM system (blue) architecture

In addition, the Booster DCCT electronics shall host analog signal conditioning circuitry, firmware for digitization and buffering, DSP for normalized current measurements, and software for data acquisition for the Booster DCCT Front End Server.

Booster BCM electronics shall be capable of up-linking to dedicated, centrally managed switch with at least 10/100 Ethernet connectivity. This switch shall connect with a rackmount front end Linux-based server. Together, these form a private DAQ network. The server shall maintain all the external interfaces to the Control System Network.

# Booster Electronics Chassis

## Overview

The Booster Electronics Chassis is a combination of commercial and in-house modules. Table 6‑1 enumerates the components, shown in Figure 6‑1. Table 6‑2 enumerates the connections, shown in Figure 6‑1.

Figure 6‑1 – Electronics Signal Interface Block Diagram



Table 6‑1. Summary of Components within Booster DCCT Electronics Chassis

|  |  |
| --- | --- |
| Figure 6‑1 | Component Description |
| 1 | Front Panel Booster DCCT Electronics Chassis |
| 2 | Back Panel Booster DCCT Electronics Chassis |
| 3 | Active commerical cassette module in powered slot, which uniquely identified by a vendor-supplied serial number and paired with commercial sensor and interconnect cable |
| 4 | Spare commerical cassette module in non powered slot, which uniquely identified by a vendor-supplied serial number and paired with commercial sensor and interconnect cable |
| 5 | Vendor-provided spare power module, used to power Transition Module, which conditions, digitizes, and measurements the NPCT signal |
| 6 | Vendor-provided power module, connected to active commerical cassette module |
| 7 | AC power connection; the electronics chassis is grounded to the AC mains ground |
| 9 | Transition Module, containing circuitry for signal conditioning, signal digitization, DSP, and DAQ |

Table 6‑2. Summary of Connections to Booster DCCT Electronics Chassis

|  |  |  |  |
| --- | --- | --- | --- |
| Figure 6‑1 | Connection Type | Interfacing Components | Description |
| 8 | DB15 for analog signals | Commercial Pickup and Active Commerical Cassette | 8-pair connection for analog excitation, sense, monitoring, and calibration signal  |
| 10 | Non-isolated BNC for TTL signals | Transition Module and MFTU | TTL inputs, which are controlled by event and delay settable ACNET devices |
| 11 | Isolated BNC for analog signals | Transition Module and Active Commerical Cassette (Front Panel) | 100Ω high-impedance bipolar signal of +/-10Vpk, 20mA max, with zero offset pot adjustment |
| 12 | Non-isolated BNC for analog signals | Transition Module and Booster LLRF Fanout Port | 1Vpp bipolar sinewave sweeping between 37.86MHz and 52.81MHz, at 20Hz |
| 13 | DB6 for TTL signals | Transition Module and Active Commerical Cassette (Rear Panel) | Vendor-defined TTL digital lines to set dynamic range as well as enable built-in +100mA calibration source |
| 14 | 10/100 Ethernet Port | Transition Module and Front End Server | Ethernet connection, abiding by network infrastructure requirements and distributed data network protocols, shall be send/receive data to/from the dedicated front-end server. NOTE: A separate Ethernet shall connect the server to the Control System as well any other client applications |
| 15 | Isolated BNC for analog signals | Booster Distribution Box and Active Commerical Cassette (Rear Panel) | 100Ω high-impedance bipolar signal of +/-10Vpk |

## Transition Module

The transition module shall consist of PCB mounted onto a Xilinx TUL PYNQ-Z2 Board, as shown in Figure 9‑2.



 Figure 9‑2 – Sketch of Transition Module Assembly

The architecture of the transition module shall consists of analog, firmware, and software components, as shown in



Figure 9‑2 – System Block Diagram of Transition Module

### Digital I/O Logic

|  |  |
| --- | --- |
| Booster NPCT DB9 Control Lines | * The NPCT shall be remotely controlled by TTL signals through Rear panel Controls DB9 connector.
* Dynamic Range Selection shall be set to ±2A.
* Remote enabling and disable of internal +100mA calibration signal to sensor head.
* Default configuration shall be recoverable after boot up.
 |

### Analog Signal Conditioning Circuity

|  |  |
| --- | --- |
| MFTU Timing Signal | * Circuitry shall provide an 50Ω TTL receiver channel.
* MFTU’s timing signal shall be configured to be locked to event with a parametrized delay value, through a ACNET device
* All MFTU components shall be supported by AD Controls Department.
* At a minimum, 5 MFTU outputs shall mimic B:TCMR2, B:TCMR3, B:TCMR4, B:TCMR5, and B:TCMR6.
 |
| Booster LLRF Signal | * Circuitry shall provide an AC-coupled 50Ω 1Vpk input channel.
* Circuitry shall down convert LLRF signal to X and Y frequency range, with a resolution of Z Hz.
* Circuity shall maintain Ndeg phase stability.
 |
| Booster NPCT signal | * Circuitry shall provide a DC-coupled high impedance 10Vpk coaxial input channel.
* Circuitry shall provide for DC offset adjustment.
* Circuitry should provide for optional high pass filtering stage.
* Circuitry shall maintain the useable bandwidth of up to half of the sampling frequency of the ADC.
* Circuitry shall maintain a 1A,avg/1Vpk dynamic range into the ADC.
* Circuitry shall maintain X SNR and X THD.
* Circuitry shall maintain RMS noise levels to <0.5μArms/√Hz.
* Circuitry shall maintain a rise time of 50µsec.
 |

### Signal Digitization and Buffering

|  |  |
| --- | --- |
| Booster NPCT signal | * The ADC shall have a sampling frequency of at least 1MSPS and at least 14 effective number of bits.
* ADC configuration shall be restorable at boot-time.
* ADC configuration shall be parameterized for remote edit/save capabilities.
* The total number of raw ADC samples shall be large enough to resolve a rise time of 50µsec.
* The raw waveform, capturing the beam response throughout the Booster ramp, shall be decimated and buffered for diagnostic viewing.
 |

### Digital Signal Processing

|  |  |
| --- | --- |
| Noise Mitigation | * Filtering techniques shall be used to reduce signal bandwidth to no less than 10kHz.
* Filtering techniques shall be used to mitigate spurious noise sources.
* The intensity measurement shall maintain a resolution of <0.5μArms/√Hz.
* The filtered waveform, capturing the beam response throughout the Booster ramp, shall be buffered for diagnostic viewing.
 |
| Baseline Correction | * The baseline correction should contribute <1% cycle to cycle variation of the intensity measurement.
* The first 3 harmonics of 60Hz shall be attenuated by X dB.
* A waveform, capturing the no-beam response throughout the Booster ramp, shall be buffered for diagnostic viewing.
* The Booster Electronics shall have the capability to reload a new waveform, capturing the no-beam response throughout the Booster ramp.
 |
| LLRF Normalization | * Frequency measurements shall be calculated with a time resolution no slower than 25 Booster turns (50 microseconds).
* An array of the LLRF frequency measurements throughout the ramp shall be buffered for diagnostic viewing.
* Normalization of LLRF signal throughout the ramp shall not contribute >0.5% error to the intensity measurement.
 |
| Intensity measurement | * Calibration of the intensity measurement shall maintain <0.5% linearity error.
* The intensity measurement shall maintain <2% accuracy at injection.
* The intensity measurement shall maintain <0.1% accuracy from the time of 20% of the injection (53turns PIP2 // 45turns BSTR) as well as through ramp until extraction.
* Intensity measurements shall be timestamped to at least 10msec resolution.
 |

### Ethernet Communication

Booster BCM electronics shall be capable of up-linking to dedicated, centrally managed switch with at least 10/100 Ethernet connectivity. This switch shall connect with a rackmount front end Linux-based server. Together, these form a private DAQ network.

|  |  |
| --- | --- |
| Ethernet Network | * All network connections must abide by global PIP-II network and security requirements and protocols.
* All network hardware shall be supported by AD- Controls Department networking staff.
* Future expansion in a climate-controlled environment suitable for commodity network and computer equipment should be considered.
* A connection to the NTP server shall be required for timestamping.
* A connection to the FTP server shall be required for remote programming.
* REDIS shall be used as a low-latency message queue & broker software, to manage communications between the Transition Module and Front End Server.
 |
| Connection between Transition Module and Switch | * 10/100 MBps connectivity to a dedicated switch shall be sufficient.
* Transition Module shall exist on a private VLAN, outside both the Fermilab General and Control Networks.
 |
| Connection between Front End Server and Switch | * 10GBps connectivity to a front end server shall be sufficient.
* Transition Module shall exist on the Fermilab Control Network.
* ACL exceptions shall be provided, as needed, to allow expert user access from the general network.
 |

# DAQ Communication Protocol

The REDIS platform provides the following :

* Redis Streams doubles as a communication channel for building streaming architectures and as a log-like data structure for persisting data.
* Redis Pub/Sub is an extremely lightweight messaging protocol designed for propagating short-lived messages with low latency and high throughput within a system.
* Redis Lists and Redis Sorted Sets are the basis for implementing message queues.

## Configuration and Subscriber Information

## Redis Stream Specifications

## Redis Pub/Sub Specifications

## Redis Lists and Sorted Sets Specifications

# Front End Server

## Overview



Figure 8‑1 – Block Diagram of Front End Server

The front server shall be responsible for concentrating data from the data acquisition modules in the Booster BCM Electronics, using the REDIS communication protocol.

In addition, the server shall manage servicing all data request from client applications, including delivering data to the Controls System through the EPICS Input/Output Controller (IOC) applications.

## Control System Device Properties

The requirements for the IOCs are:

* Must be capable of data logging all process variables (PVs) per Booster cycle at 20Hz.
* Must be capable of delivering and displaying waveforms up to 2048 points per Booster cycle at 20Hz.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Type | Name Format | Size (B) | Rate | Description | Unit |
|  |  |  |  |  |  |

## Diagnostic Data Device Properties

The requirements are:

* Must be capable of writing data to comma separated value files for archival
* Must be capable of delivering and displaying waveforms up to 2048 points per Booster cycle at 20Hz.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Type | Name Format | Size (B) | Rate | Description | Unit |
|  |  |  |  |  |  |