Proposed DAPHNE V3 Architecture

Jamieson Olsen (with minor mods & additions by dcc 11/15/22)

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Legacy DAPHNE Architecture

DAPHNE V1 and V2 is based around an FPGA and microcontroller

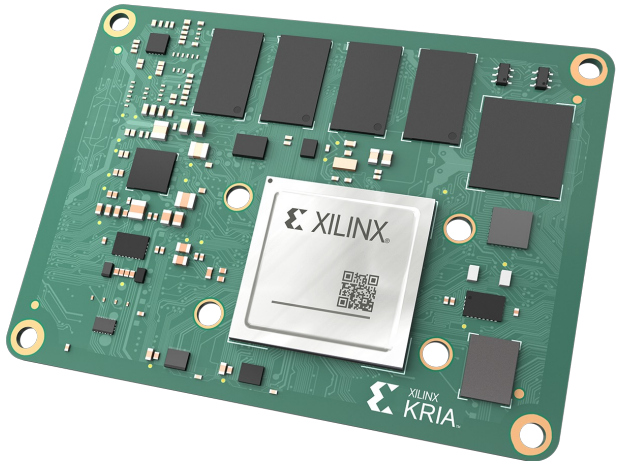
- Artix-7 FPGA
  - Collects data from AFE front ends and sends output to DAQ
  - High speed serial links limited to 6.6Gbps
  - 200k logic cells
- ARM Cortex M4 Microcontroller
  - Controls most “slow” board functions (DACs, ADCs, configures FPGA, etc.)
  - Software based on FreeRTOS and programmed in C
  - Only supports 10/100 Ethernet
  - Stores a single FPGA bitstream in Flash (no filesystem)
  - Software updates via USB programmer cable

DAPHNE V3 Upgrade Plan

- Replace the current FPGA + microcontroller with system on module (SOM)
  - More and better FPGA resources
  - Supports multiple 10G Ethernet links to DAQ
  - Supports 1G Ethernet link for controls
  - Real operating system and real file system
- Minimize changes to analog front end circuitry
- Minimize changes to HV Bias circuitry
- Minimize changes to readback and other telemetry
- Simplify and improve power regulation
  - Improve regulation on analog power rails
  - Eliminate some digital power rails (+1.0VD, +1.2VD)

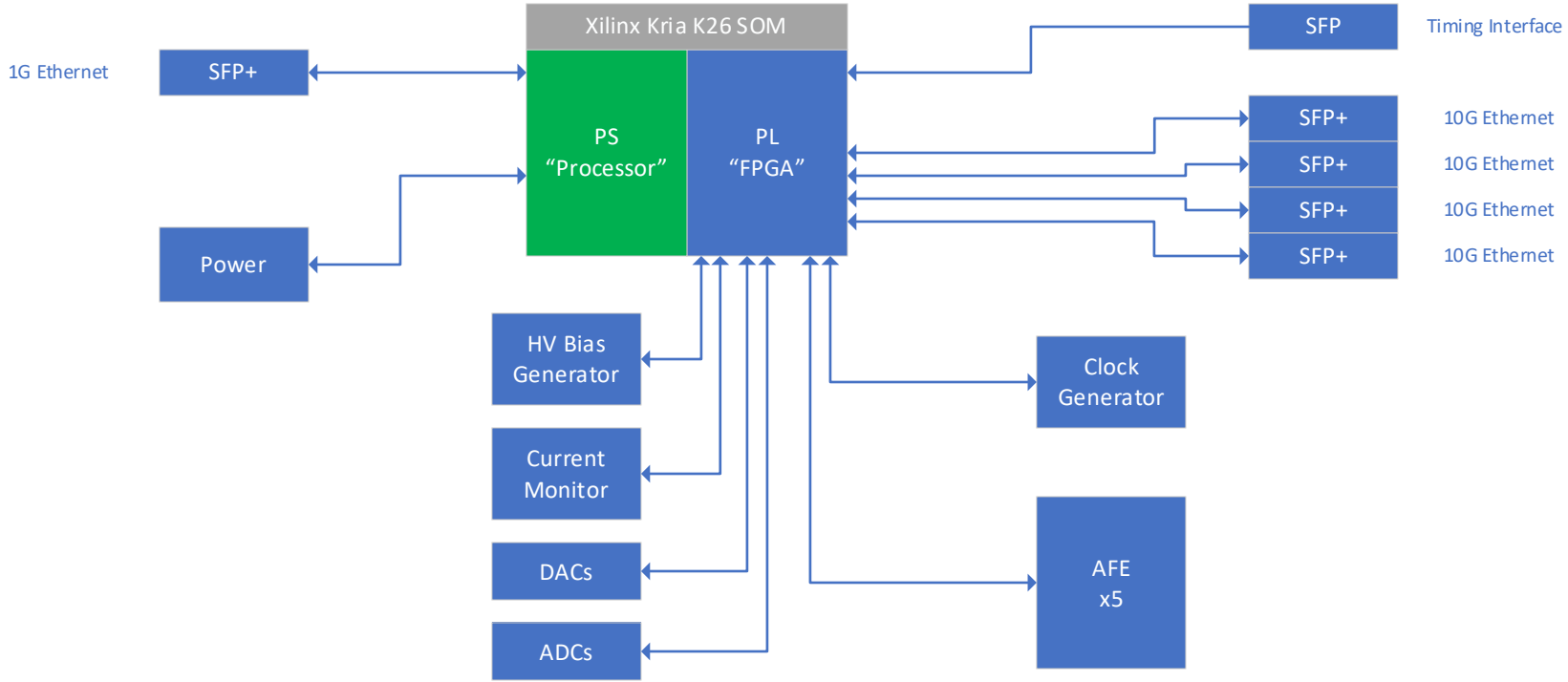
Xilinx KRIA SOM

- Based on Zynq UltraScale+ MPSoC FPGA and manufactured by Xilinx
- Processor (PS)
  - Multicore ARM CPU capable of running full Linux OS
  - Module includes 4GB RAM and 16GB flash storage
  - Optical Gigabit Ethernet connection
- Logic (PL)
  - 250k logic cells (equivalent to current Artix-7)
  - 4 x 12.5Gbps serial links
  - Lots of I/O pins brought out to two 240 pin connectors
- Single +5V power supply
- Small sized module
- In stock $390 each (quantity 1)



77mm x 60mm x 11mm
(with heat spreader)

DAPHNE V3 Block Diagram



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Firmware Changes

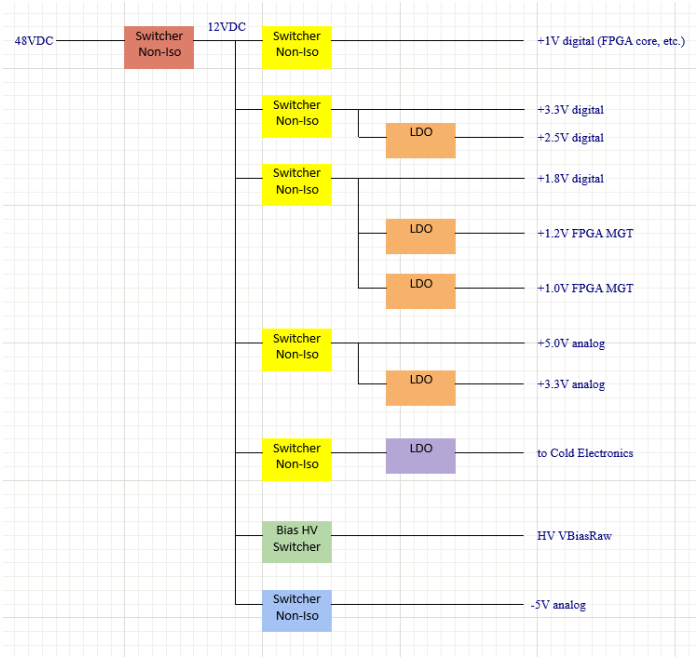
- Remove Gigabit Ethernet interface logic
- Keep AFE front end
- Keep spy buffers
- Keep core sender logic
  - Change from FELIX format to Ethernet format
- Keep timing interface
- Add peripheral IP blocks (or do this on the PS side)
  - SPI master
  - I2C master
- Add bridge/interface to “PS” side
  - AXI bus or something simpler

Software Changes

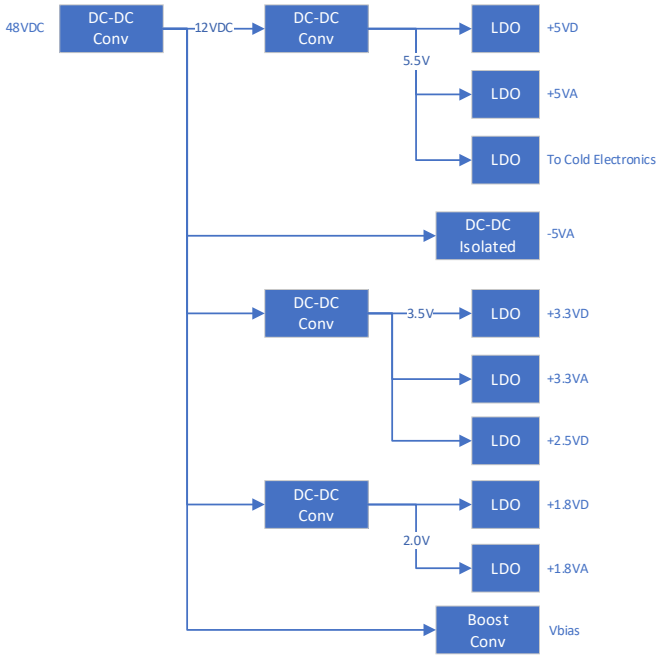
Rather than developing “bare metal” software on a small microcontroller we now have a full OS to work with. Software development times should decrease, and more collaborators can be involved at a higher level.

- Users connect via SSH, telnet, FTP, browser, etc.
- Real file system is available for storing multiple FPGA bit files
- Create device drivers for DAPHNE board components
  - These map into filesystem “UNIX style” under /dev
- Users write shell scripts, Python, C++, etc. to control the board functions
- Can copy the Firmware/Software architecture used by the TPC electronics Warm Interface Board (WIB)

Power Distribution Changes



DAPHNE V1 and V2A



DAPHNE V3

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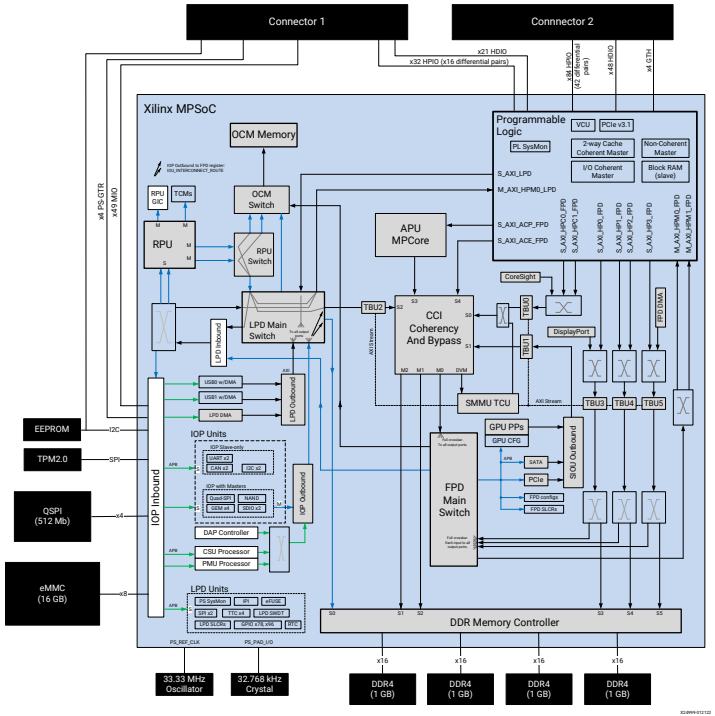
Kria K26 I/O & DAPHNE requirements

- Two 240-pin connectors provide:
  - Power and ground
  - Control and status signals
  - Connections to the Programmable Logic (PL):
    - 58 HPIO (high performance I/O) pairs
      - 5x9=45 required for AFE readout + 1 pair for the 62.5 MHz clock
    - 69 HDIO (high density I/O) for CMOS signals
    - 4 GTH (high speed serial transceivers) [10 GbE]
  - Connections to the Processing System (PS):
    - 49 MIO (multiplexed I/O)
    - 4 GTR (serial transceivers) [GbE]
- PS includes I2C and SPI units
  - I2C and SPI could be connected directly to the PL side of the Zynq or could be connected [through multiplexer chips] to the PS side.

Kria K26 block diagram

Figure 1: **K26 SOM Block Diagram**



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