Status of Microelectronics Program at Fermilab

Farah Fahim and Jim Hirschauer on behalf of Microelectronics Division

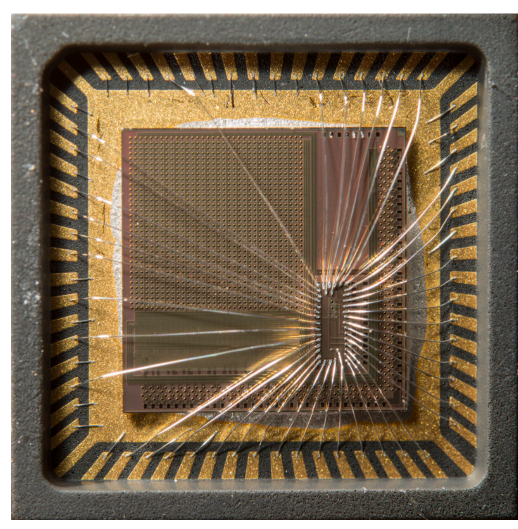
Outline

- Vision and Strategic Drivers
  - Leveraging Unique and Core capabilities
- Microelectronics Division organization
  - Structure
  - Workforce development
- Microelectronics Program Update
  - CMS
  - Quantum
  - Pixel detectors
  - AI
  - Microelectronics co-design

Vision and Strategic drivers

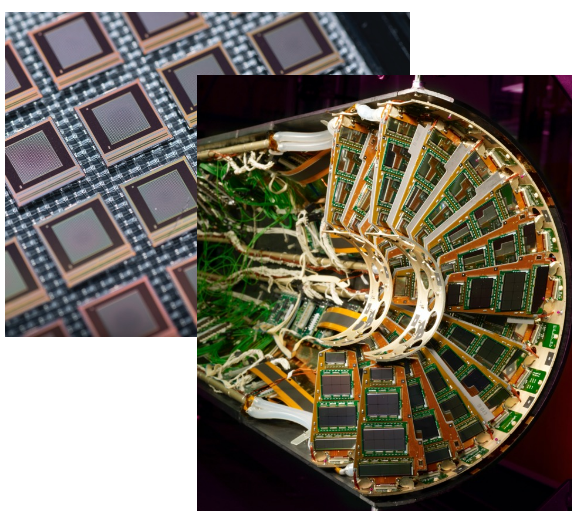
Fermilab ASIC Design Capabilities and Mission

ACADEMIC RESEARCH



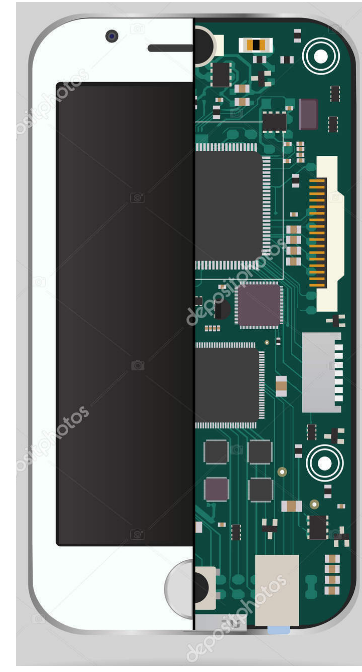
- **Support interdisciplinary research**
- **Enables new scientific discovery and foundational engineering**
- **Novel solutions**
- **Mission: new knowledge and education of students**

NATIONAL LABS: ADVANCED SCIENTIFIC INSTRUMENTATION



- **Support scientific experiments operating in extreme environments**
- **Mid-size scaling for large experiments**
- **Mission: robust performance over several decades**

INDUSTRY – PRODUCT DRIVEN



- **Support consumer electronics**
- **Mature designs**
- **Mission: incremental product driven design**

Technology readiness level

Growth of IC design over 3 decades

DOE HEP builds and operates among the most difficult and biggest projects with the most complex detectors in science.

These experiments operate in **extreme environments** which require robust custom microelectronics with long-term reliability over decades

Since 1980's

Ionizing radiation
>1 Grad (1000x higher than outer space)
Extreme flux for single event upsets
- Collider Experiments (FCC, HL LHC)

Since 2010's

Cryogenic electronics (77K – 100K)
- Neutrino experiments (DUNE), Dark matter experiments (Skipper CCDs)

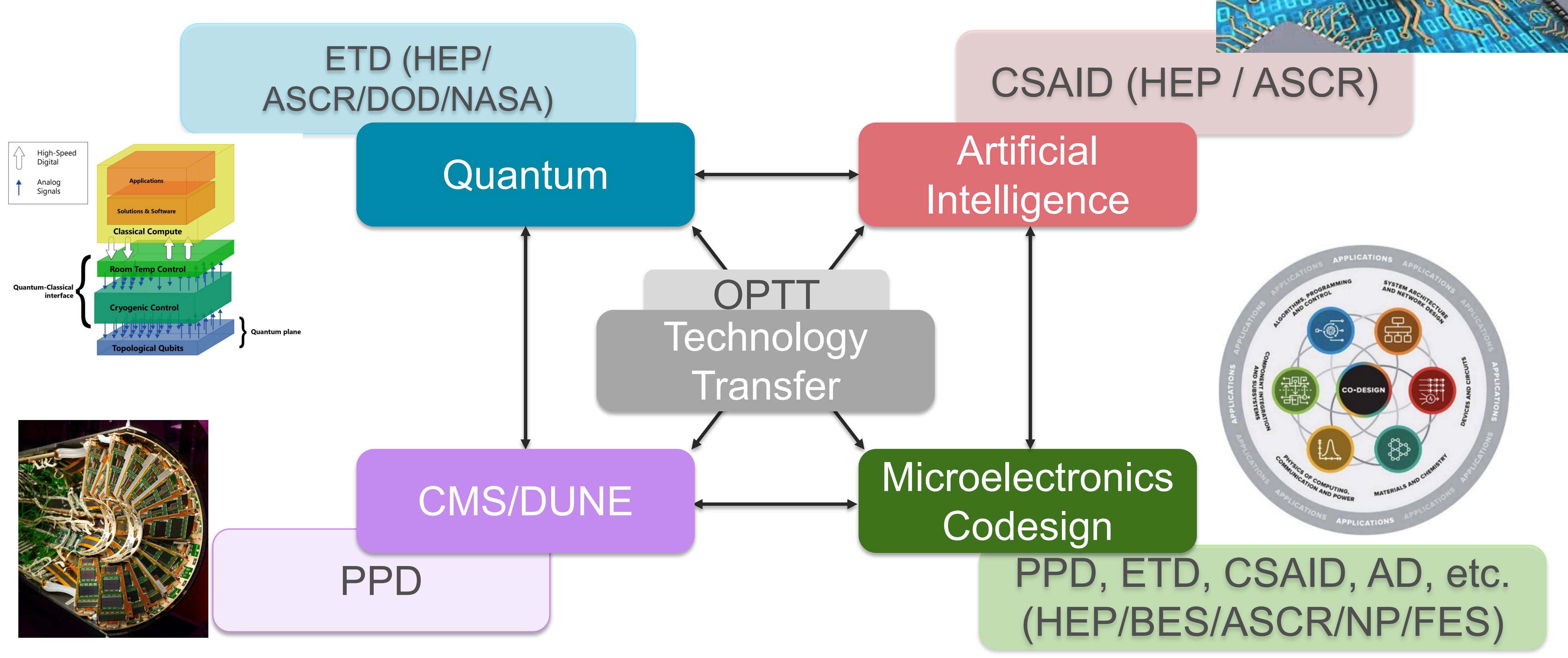
Since 2019

Deep Cryogenic electronics (~ 4K)
- Dark matter experiments (Cryogenic detectors e.g. SNSPDs, TES etc.), Quantum Information Science

New 2022

Superconducting electronics (~100 mK)
- Quantum Information Science (TWPAs, JPAs for ADMX)

ASIC Design at Fermilab



Fermilab

Microelectronics

Vision: Fermilab together with other national labs, academic and industry partners establishes and co-leads a major US Microelectronics Co-design center

Major decadal goals

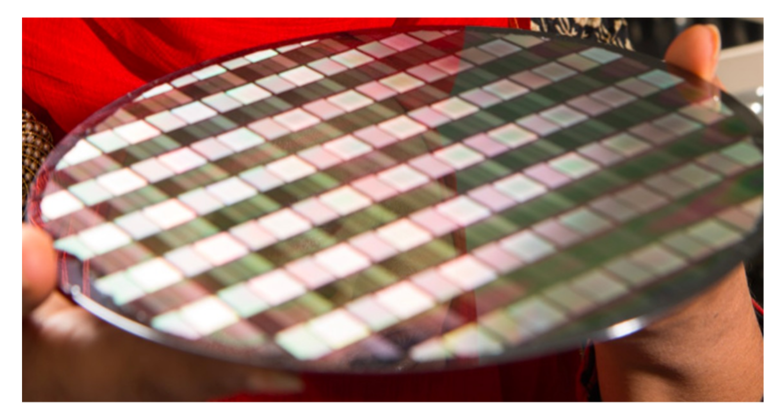
- **Support the community for extreme environment microelectronic development**
  - Develop ecosystem, promote/foster collaboration

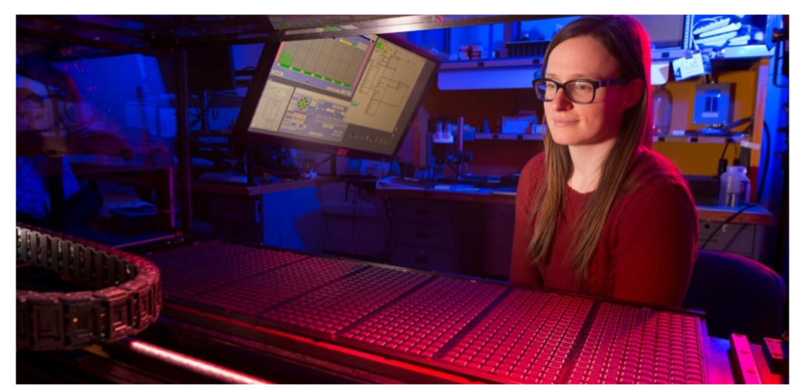
Further advance expertise in state-of-the art integrated circuit design and testing to enable precision science measurements

- Develop smart detectors with integrated sensing - edge computing - communication

Engage with Industry on Heterogeneous Integration and Advanced packaging solutions

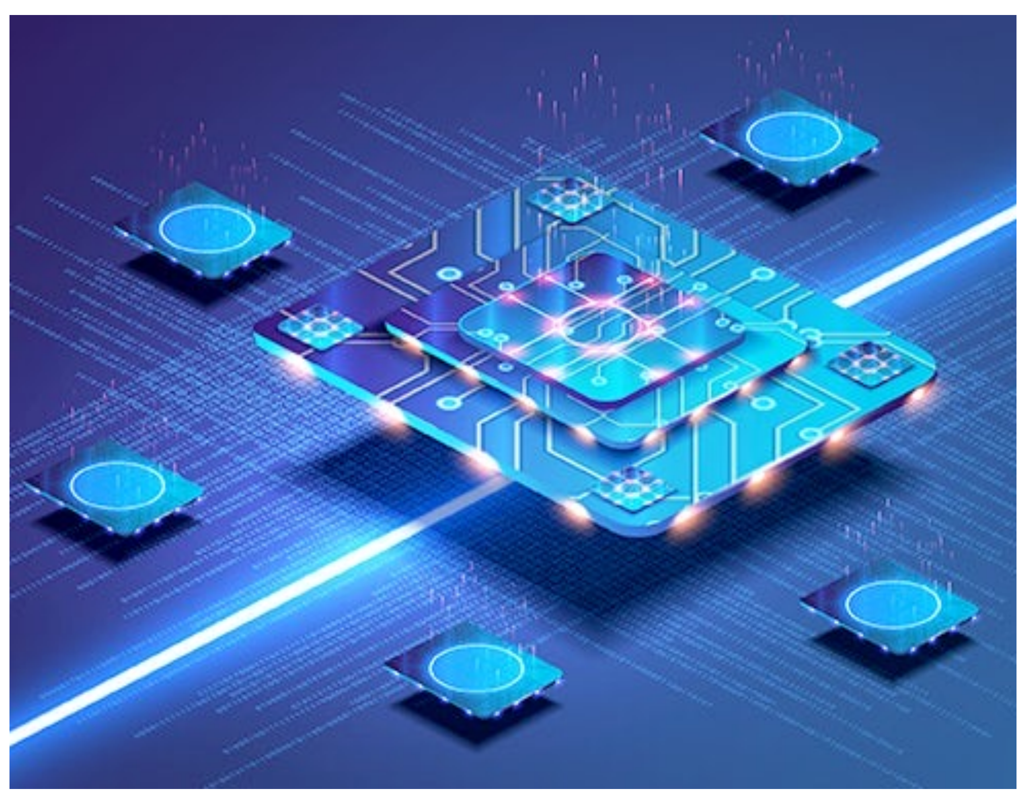
- Both leverage and advance transformative technologies





Design Goals for the next 20 years: Enable Smart Sensors

- Low power, low noise, ultra-sensitive analog for sensor signals (both amplitude and time)
- CMOS sensors
- SOC approach for integrated digital (reconfigurable, reprogrammable architectures)
- AI-on-chip for compact ML inference models for edge compute (data processing at source)
- Wireless / Integrated photonics (long distance data transfer)
- Integrated THz electronics (short distance communication)



Work with Material scientists (BES) to integrate new devices with CMOS chips
Work with Algorithm Developers (ASCR) to exploit neuromorphic and distributed compact algorithms
Work with industry to leverage production-scale processing

Microelectronics Ecosystem

- *CAD-EDA tool initiative for growth of microelectronics teams across the DOE complex (led by Helmut Marsiske)*
- Co-designing with other applications more cross agency collaborations (DARPA: new extreme environment initiative)
- Collaborative cross disciplinary teams with academia, national labs, international partners and industry
- Microelectronics workforce: Career pipeline for research engineers
- Focus on technology transfer and enable spin-offs

HEP for Microelectronics for HEP: Emphasis on Co-design

Fermilab is a key contributor and a driver in the Microelectronics ecosystem

- Fermilab's expertise in Microelectronics for extreme environments and collaboration with industry and academia enables the development of robust techniques which allows the **maturation of novel technologies**
- Fermilab collaborates extensively to enable breakthroughs in instrumentation: Academia, National Labs and Industry form a spectrum from foundational research, advanced instrumentation to mature production. **Driver for mid-volume prototyping**
- **Multidisciplinary teams** to enhance microelectronics co-design
- Innovation translation: Small volume prototyping of systems based on novel devices, innovative circuit solutions and integrated architectures would enable accelerated demonstration leading to industry spin-offs or rapid adoption for **economic growth**
- Tools and techniques developed for HEP research in addition to accelerating scientific discovery will also benefit industry applications. **Democratizing innovation**

HEP for Microelectronics: Application driven innovation

- Cutting edge particle detectors and accelerators create massive amounts of data which require powerful and energy efficient processing. The **engineering design requirements** for these detectors exceed those associated with industry including the Internet of Things for Industry 4.0, Smart cities, and Smart sensors for autonomous driving:
  - The data generated per second in just one large collider physics experiment is equivalent to the average internet traffic across North America.
  - Experiments require more than one billion individual sensors with edge computing and ultra-low power and low-latency communication. The time scale to make decisions are a few orders of magnitude faster than typically required for industry applications.

- **New tools and fabrication techniques** are required to build microelectronics that provide robust performance in the extreme operating conditions of a HEP experiment:
  - The high radiation environment of a collider detector (1000x outer-space) demands development of techniques to radiation-harden commercial microelectronics.
  - The technical challenge, cost, and environmental impact of powering and cooling one-billion sensors of a HEP experiment necessitates optimized devices with ultra low power consumption.
  - Cryogenic operation (100 mK to 77K / -459F to -321F) of devices for readout of quantum sensors and cryogenic detectors necessitates collaboration with industry to develop cryogenic models and improve device performance.
  - The inaccessible location of microelectronics operating in extreme environments requires long-term reliability (2-3 decades) for robust operation.

HEP for Microelectronics: Application driven innovation

- **Rapid prototyping** at scale requires us to evaluate competing technologies:
  - We are early adopters of technology allowing us to assess and increase technology readiness level resulting in accelerated lab to fab innovation
  - Some of our sensor arrays are almost twice the area of a basketball court requiring small volume prototyping. This gives us invaluable statistical insight into device properties, and influences improvements in material growth and fabrication.
  - Deployment of compact detectors with lower size weight and power (SWaP) is a driver for evaluating hybrid integration and advanced packaging solutions

Microelectronics for HEP:
Beyond state-of-the-art Sensor development for production scale

- ***Fabrication and Prototyping:***

Fermilab and SLAC researchers are working with Tower Semiconductor (recently acquired by Intel) to develop Skipper-in-CMOS for precision cosmology experiments which require mid volume production. Invaluable statistical insight into new device properties, and influences improvements in fabrication processes.

- ***Devices, Circuits and System integration:***

Fermilab has developed low power, low latency, radiation tolerant and/or cryogenic circuits to process sensor data at-source for almost 40 years. We have developed world leading integrated circuits for ultra-sensitive (< 1e- noise) or ultra-fast timing (< 10ps) detection, high frame rate pixel detectors, cryogenic data convertors and processors, radiation tolerant AI-on-chip and AI-in-pixel. Fermilab is working with Microsoft to develop low-power, high-speed, deep cryogenic data convertors for scaling Quantum systems. Fermilab with MIT Lincoln lab is developing 3D electronic-photonic integration prototypes to demonstrate low size, weight and power (SWaP) hybrid heterostructures. Over two decades Fermilab has worked with industry including Ziptronix, RTI International - now Micross, NHanced, Global Foundries, Skorpios Technologies, Cactus materials to advance and demonstrate key 3D integration technologies.

Microelectronics for HEP

- *<u>Computing and Algorithms:</u>*

hls4ml - a powerful open-source hardware-to-software codesign tool to optimally implement machine learning algorithms on extremely efficient hardware platforms to address data reduction challenges for ultrafast detectors operating at Pb/s. Beyond driving AI-on-chip applications in the scientific community, Fermilab works with industry leaders to provide custom optimized solutions: Siemens is working to integrate the hls4ml flow with their synthesis tools for industry end users; and we collaborated on Internet-of-Things "TinyML" solutions with AMD/Xilinx for industry-standard MLPerf benchmarks.

- *<u>Characterization and Testing:</u>*

Fermilab researchers are working with Synopsys and Global foundries to test, characterize and model properties of devices at deep cryogenic temperatures facilitating the development of cryogenic process design kits (PDK). Reducing the need for component vendors to develop cryogenic test systems and deep in-house expertise and spurring the growth of beyond CMOS hybrid architectures such as cryoCMOS with superconducting devices.

DOD Microelectronics commons

DISTRIBUTION STATEMENT A. Approved for Public Release

Microelectronics Commons Addresses the Valley of Death

THE OFFICE OF THE DEPUTY TECHNOLOGY OFFICER FOR CRITICAL TECHNOLOGIES

Microelectronics Commons

Electronic Warfare

Secure Edge/IoT Computing

AI HW at the Edge

Quantum Technology

5G/6G Technology

Commercial Leap Ahead Technologies

Core Facilities
- CMOS + New Technology Integration
- Non-CMOS

Commercial Industry

Defense Industrial Base

Defense Programs

Required Investment

Research Universities, Start ups face barriers to Technology Demonstration

Innovation Hubs boost research connections to facilitate prototypes targeted to regional market strengths

Core Facilities provide access to scale early stage prototyping, and engage with Industry and NSTC to burn down risk for integration of new technologies with commercial SOTA

Commercial adoption and optimization for Defense program demonstrators

University & USG

VC Investment

Commercial and DoD Program Investment

"Valley of Death"

Proof of Concept → Prototype in Laboratory → Prototype in a Foundry/Fab → Capacity in Production Environment → Demonstration of Production Rates → Defense Program and Commercial Adoption

11

DOD Microelectronics commons

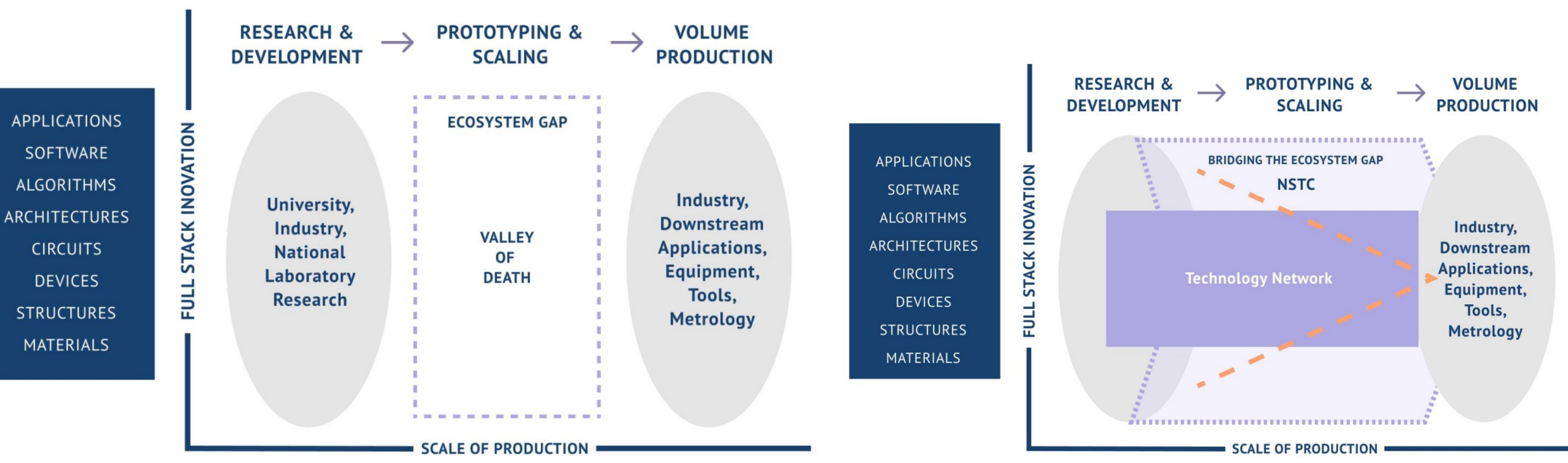
- Investigating joining and participating in Indiana led regional hub with UIUC/NU/ANL/UC

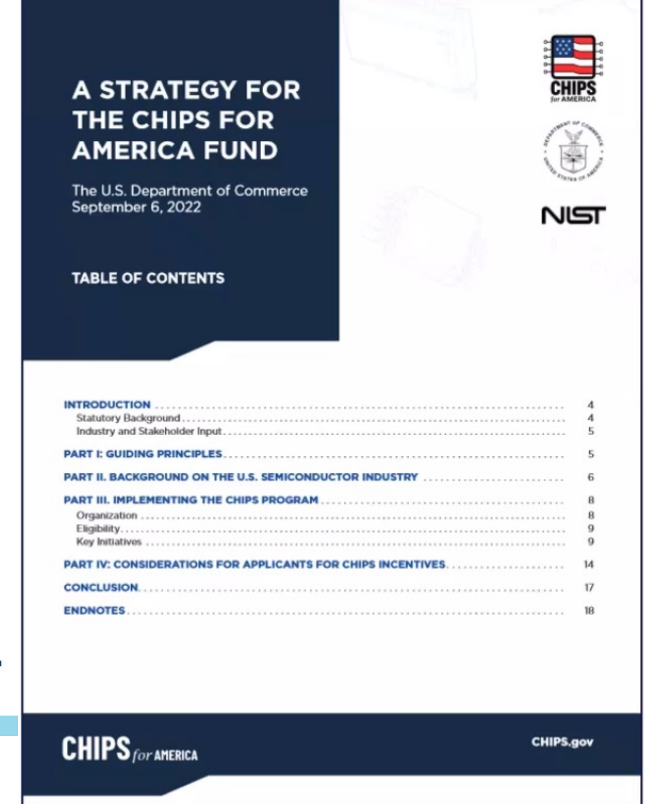
Microelectronics Commons development notional timeline

	Oct – Dec 22	Jan – Mar 23	Apr – Jun 23	Jul – Sep 23	Oct – Dec 23
Program Elements	**FY23 Q1**	**FY23 Q2**	**FY23 Q3**	**FY23 Q4**	**FY24 Q1**
Announcements	Coming Soon Announced via NSTXL/S2MARTS; Industry Awareness Day		NSTXL Call for Projects		
Acquisition	RFS for 9 Regional Hubs via NSTXL/S2MARTS	9 Hubs selected	Awards to 9 Regional Hubs	Project Selection Finalized	Project Awards

CHIPS Act. and Microelectronics

- National Laboratories possess unique technical expertise and user facilities that are essential to overcoming foundational research challenges relevant to the topics described in materials science, electronic and photonic device technologies, processing and packaging technologies, manufacturing technologies, circuit, chip, and system architecture, and software system and algorithm development in a co-design fashion, and translating and transferring research outcomes to industry
- IBM led: **ASIC: American Semiconductor Innovation Coalition** – JOINED (6/10 work streams)
- Mitre led: **Semiconductor Alliance** – In discussions for membership

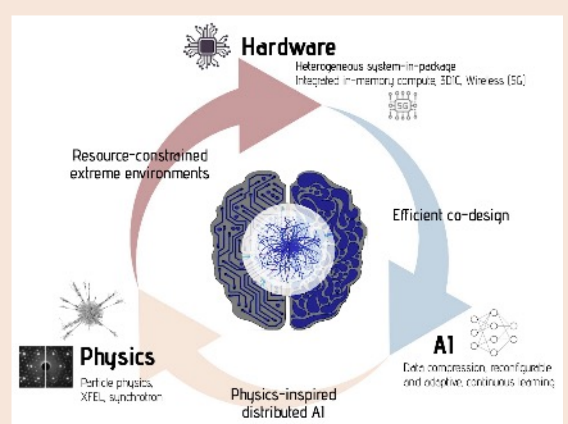




Systematic co-design for extreme edge computing in smart sensors

a DOE co-design microelectronics center for real time sensing, communication and storage

New devices for sensing and computing – Materials & Devices
Circuits, micro-architectures, algorithms – Edge Sensing, Edge Computation & Low Power Communication
Systems, Architectures and applications – Integration and Packaging Technologies



- Planning for a potential DOE Microelectronics Center
- Organized series of workshops to define center focus
- In discussions with ORNL and ANL as potential other partners
- Strong participation with Industry Collaborators (Global foundries, Intel, Synopsys, Siemens, Cadence, Microsoft, AMD, Xilinx)

Microelectronics Division Organization

Proposed Microelectronics Division

- Synergies with Detector Development

Emerging Technologies Directorate

Microelectronics Division

ASIC Design Department
1. Advanced Digital and Verification
2. Ultrafast timing and Cross cutting Initiatives
3. Quantum and Analog cryoelectronics

Advanced Packaging and Metrology
1. Testing and Characterization
2. Advanced Packaging

Codesign
1. Sensors Codesign
2. AI Codesign

ASIC Design Department

Head : Farah Fahim
Deputy : Jim Hirschauer

ASIC R&D Department

University Interns
Dyumaan Arvind (Stonybrook)
Manuel Blanco Valentin (Northwestern)
Priyanka Dilip (Stanford)
Olivia Seidel (UTA)
Suyash Tripathi (U. Toronto)
Austin Williams (Purdue U.)

Advanced Digital and Verification
Group Leader: Jim Hoff
Deputy Group Leader: Chinar Syal

Giuseppe Di Guglielmo
Christian Gingu
Neha Kharwadkar
Alpana Shenai

Ultrafast timing and Cross cutting Initiatives
Group Leader: Davide Braga
Troy England
Quan Sun
Xiaoran Wang
Kyle Woodsworth
Fabricio Alcalde Bessia (JA)
(Datao Gong)
Tom Zimmerman (R)

Quantum and Analog cryoelectronics
Group Leader: *Shaorui Li (LOA)*
Farah Fahim

Benjamin Parpillon
Adam Quinn
Hongzhi Sun

Structure and Partnerships

ASIC PMG (oversight)

University Partnerships

(ECE departments)

- Northwestern U.
- Columbia U.
- Purdue U.
- Washington U.
- UIC, UIUC
- University of Washington
- Stonybrook University
- EPFL
- and several other physics departments

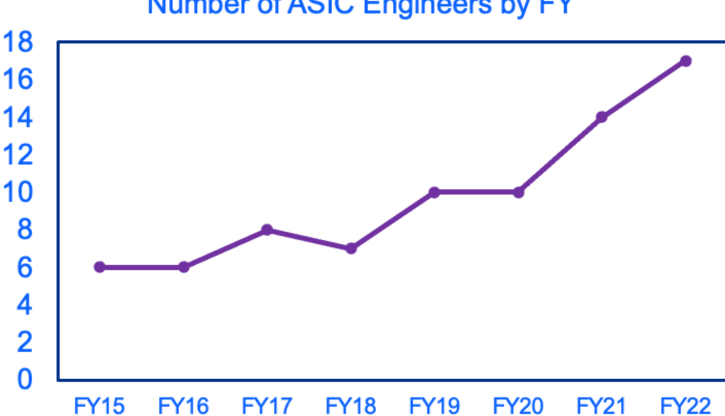
Industry Partnerships

- Microsoft
- Global Foundries
- Synopsys
- Siemens
- Skywater
- Flex logix
- Caporus Technologies
- Nhanced
- Qolab
- other SBIR companies ….

ASIC Groups

- Quantum and Analog Cryoelectronics
- Advanced Digital and Verification
- Ultrafast timing and Cross-cutting initiatives
- Testing and Tool support

- 19 ASIC designers (2 JA) + *1 open position*
- 1 scientist, 2 Application Physicist
- 1 test engineer, 1 engineering associate
- Other matrixed personnel



Workforce development

ASIC Design Associate Internship Program (5 per year from 3 to 6 months)

2021: Adam Quinn, Zexi Liu, Aly Shoukry, Nate Corrier, Apurv Bharadwaj

2022: Austin Williams, Olivia Siedel, Suyash Tripathi

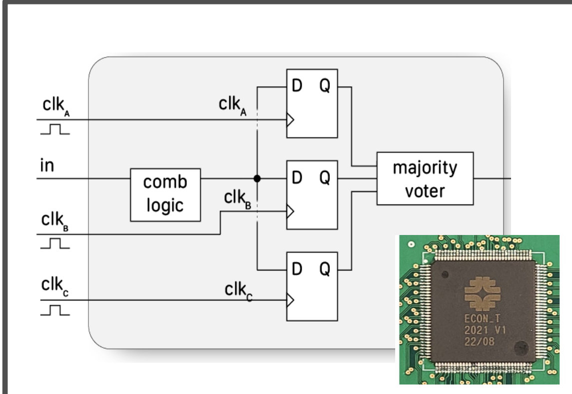
HEPIC Internship: 2022: Priyanka Dilip

PhD/MS students: Manuel Blanco Valentin, Dyumaan Arvind, Suresh Senthilkumar

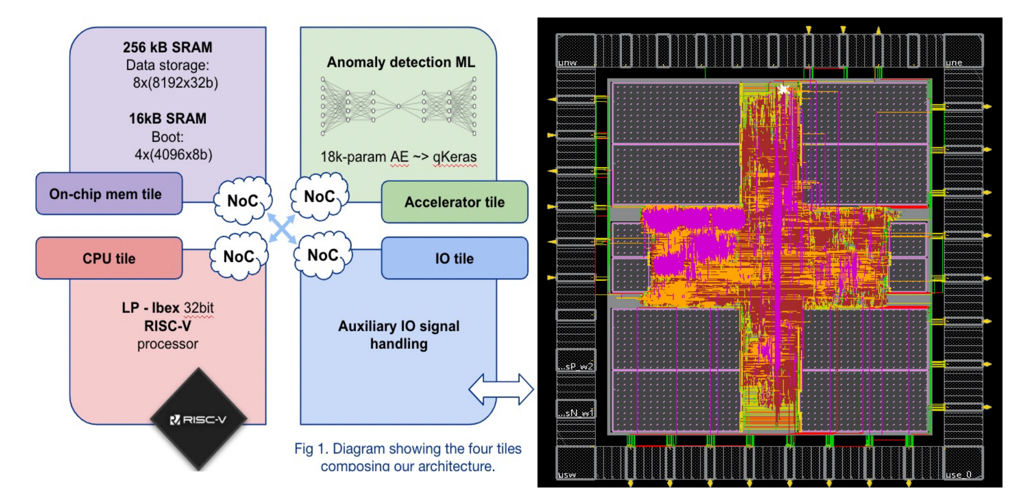
Hosted 4 target students last year, support students through the various Fermilab internship programs

Hiring IC Designers has been extremely difficult, 1 position open for more than 1 year

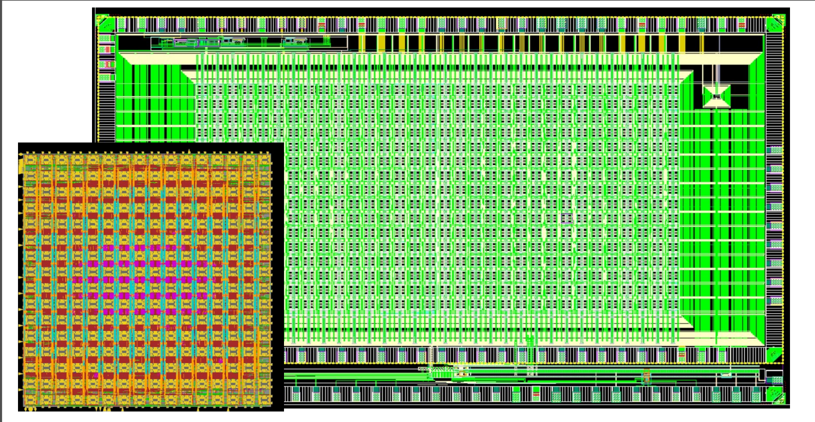
Highlight – Manuel Valentin (NU)



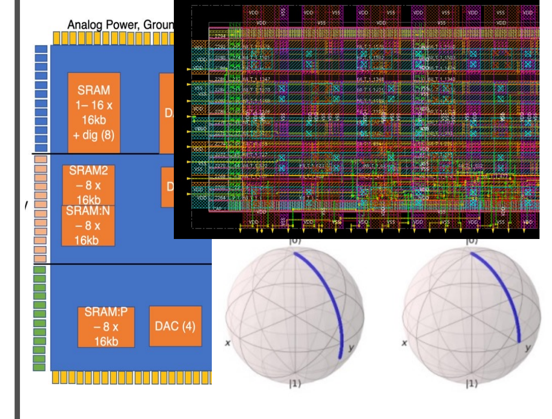
(2020/21) - TMR – ECON-T
On detector ASIC for data compression in hard-rad env (CMS)
Auto code-agnostic tool for triplication: HackDL



(2021/2023) - CryoAI
Prototyping cryogenic chips for machine learning at 22nm
Digital flow – GF22nm
ESP – Cryogenics - SLVT – Biasing

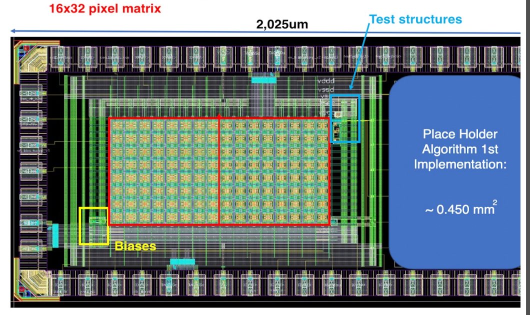


(2022) - AI in Pixel (a.k.a SPROCKET)
Xray imaging – 4 quads
Digital flow – TSMC65 (2 tapeouts)
Congestion solving approaches



(2022) - CITC2 - GF22
(2022) - SQUID - GF22
Bin2therm cryo DACs
(2022) - quantumML
Quantum readout/ctl

(2022/23) - CMS28
Data compression with AI – CMS Pixels
Digital flow - TSMC28



Digital process flow automation

https://github.com/manuelblancovalentin/wolf

(2021/22/23) - Wolf

Tool for automatic digital flow environment control

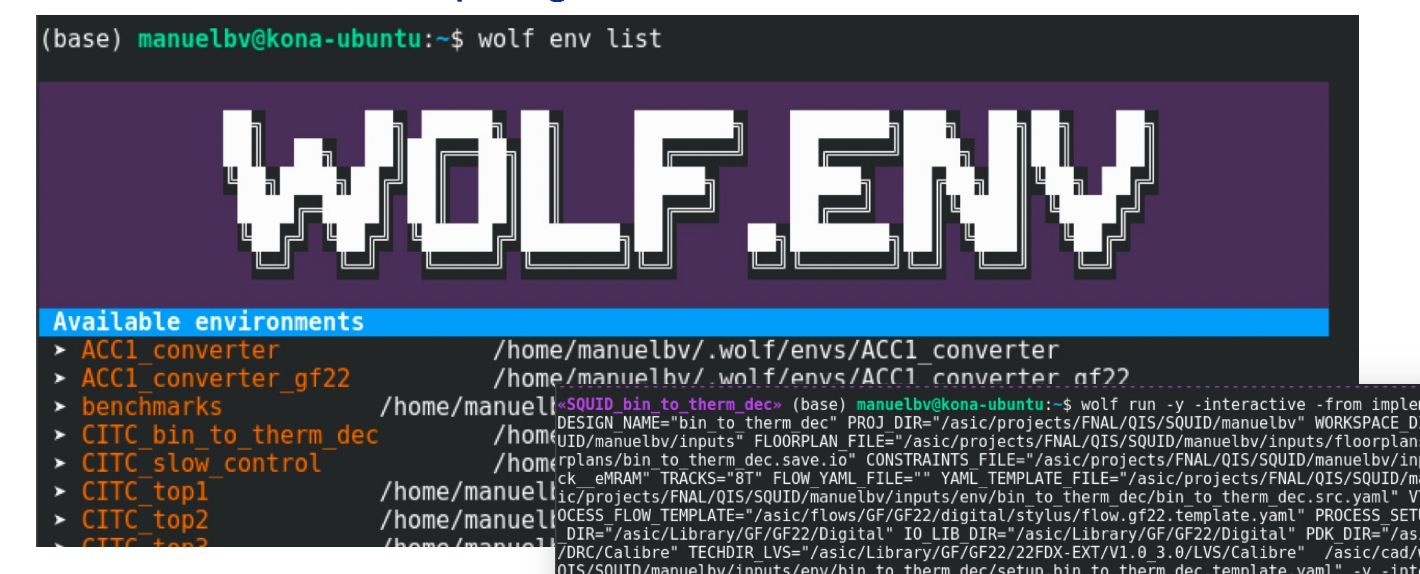
- Creates containers (env) where variables associated with
  - PROCESS
  - DESIGN
  - PROJECT SPECIFICATIONS
  - …

  are defined

- Automation of:
  - flowtool
  - stylus flows

- Easy exportation of environments for sharing

- ***HIRED by CADENCE for an internship in 2023***



Wolf environment

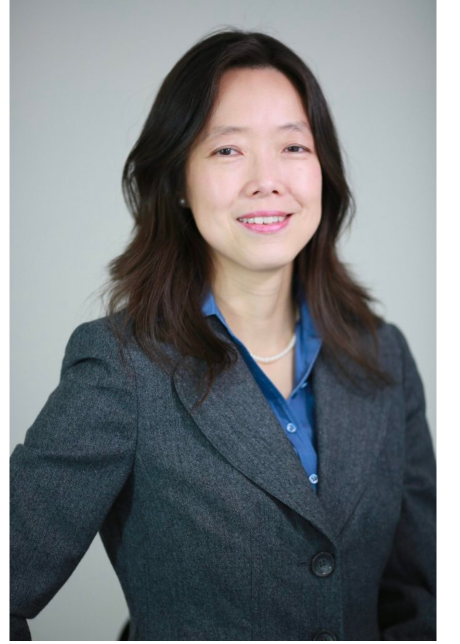
DESIGN_NAME=…
PROCESS=…
VTHS={…}
CONSTRAINTS=...

Process flow (flowtool)

Technology Transfer

- Based on technology developed out of the Fermi National Accelerator Laboratory, Lismikro's microchip controllers enable quantum computers to solve the biggest computational challenges

Fermilab Engineer Scales Quantum Startup with Support from UChicago



Shaorui Li,
Group leader: Quantum and Analog Cryoelctronics
Fermilab Lab Innovation Fellow

Requirements for success

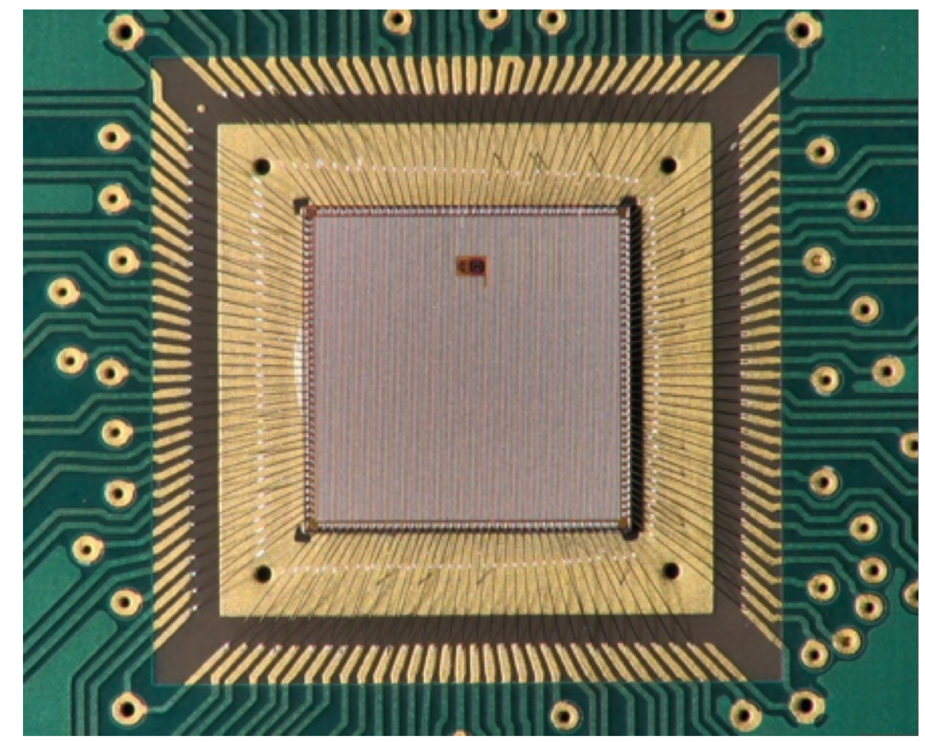
- **Seed funding for deep technology R&D**
  - Business Development funds
  - LDRD funding
  - Base funding
- **Strong scientist support and participation**
- **Workforce training and development**
  - Employee training
  - Career pipeline development
- **Partnership with Academia and Industry**
  - Beyond Physics group engaging Engineering departments
- **Partnerships beyond HEP: Develop technology roadmaps in parallel with science goals**
  - Across Office of Science
  - Across federal agencies (NASA, DOD etc.)

Microelectronics Program: CMS Upgrade

CMS HL-LHC Upgrades: Production ASICs

- **ECON-T and ECON-D Data Concentrator ASICs** for High Granularity Calorimeter
  - Manage extreme data challenge of 6M-channel "imaging calorimeter" on Trigger and DAQ paths
  - First radiation-hard neural network for on-detector data compression with ML
  - **ECON-T-P1** : full functionality prototype, extensively tested for functionality and radiation tolerance
  - **ECON-D-P1** : to be submitted March 1, 2023

- **ETROC Frontend ASIC** for Endcap Timing Layer
  - High precision TDC (resolution better than ~40ps) for use with LGAD sensor; radiation tolerant, low power
  - **ETROC1** (4x4 pixels, simplified readout) : fully tested and meeting all specs
  - **ETROC2** (16x16 pixels, full functionality) : submitted Oct 2022.



Quantum: QSC, Quantised, LDRD

QSC: Cryogenic Electronics for Ion Traps

Goal

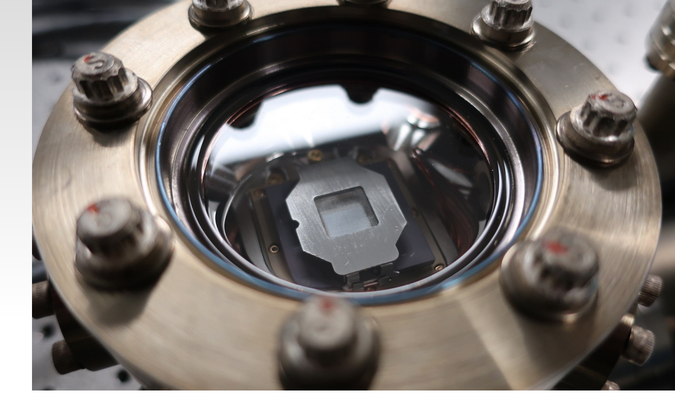
Develop cryogenic electronics for low noise control of ion trap simulation platform.

Team

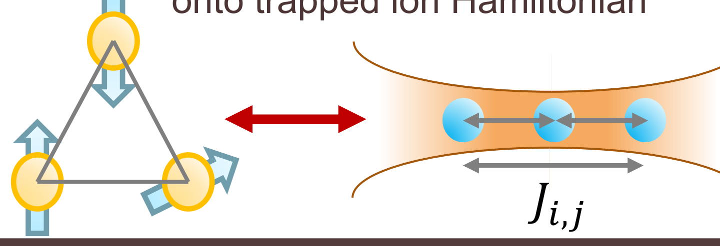
PI: Farah Fahim, *FNAL,*
Hongzhi Sun, Shaorui Li, Zexi Liu, Xiaoran Wang, Chinar Syal, Austin Williams **FNAL**. Dyumaan Arvind, Milutin Stanacevic **Stonybrook University**, Manuel Valentin, Seda Memik, **Northwestern University** Chris Seck, John Comish, Gilles Buchs, ***ORNL***

Approach

- Utilize Fermilab expertise in cryogenic applications-specific integrated electronics to develop low noise control system for ion traps
- Co-design with simulations thrust by implementing in existing ORNL ion trap system to scale up number of trapped ions.
- Use natural mapping of quantum spin liquid Hamiltonian onto ion trap system to simulate properties of QSL
- Test predictions with materials samples and sensors developed by QSC



QSL Hamiltonian can be directly mapped onto trapped ion Hamiltonian

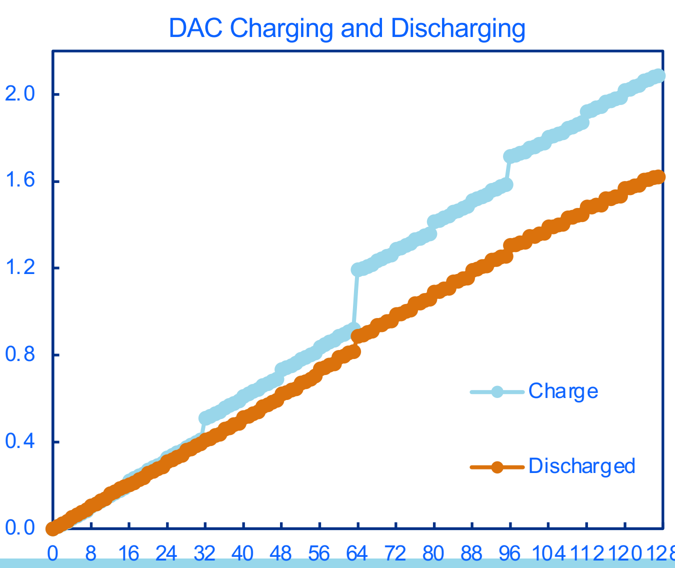


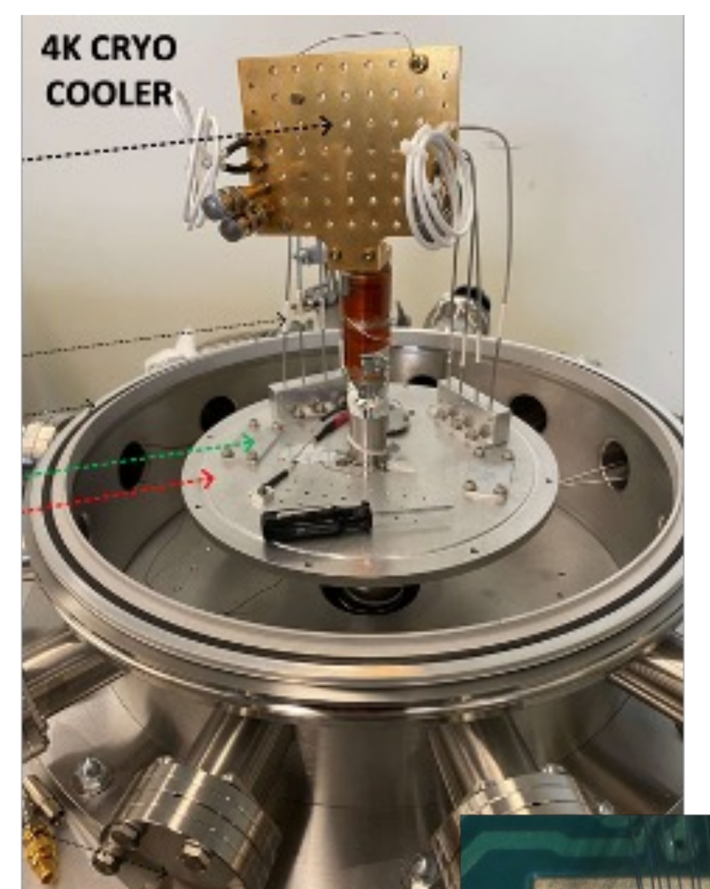
Milestones

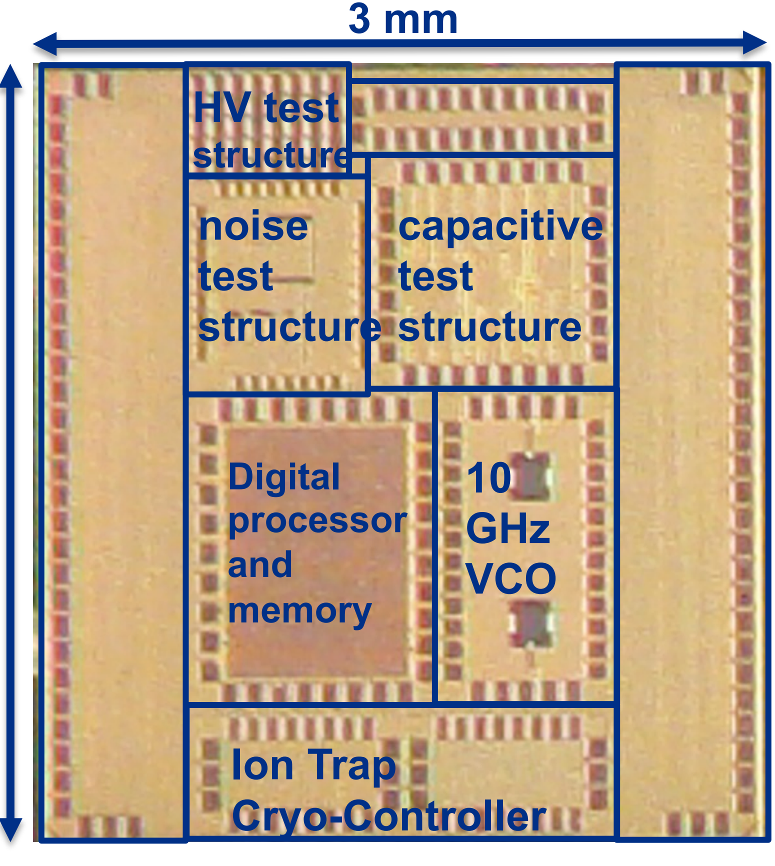
Year 1	Year 2	Year 3	Year 4	Year 5
Design of array of 10 MSPS 14-bit digital-to-analog converters (DAC)	Delivery of arrays of 10 MSPS 14-bit DACs operating at 4K	Delivery of arrays of 100 MSPS 16-bit DACs operating at 4K (higher speed, better resolution). Integrate with Ion trap	Design of arrays of 100 MSPS 16-bit DACs, focusing on lower noise, lower power.	Delivery of ultralow noise (nV/rtHz), ultralow power arrays of 100 MSPS, 16-bit DACs for integration with the ion trap system.

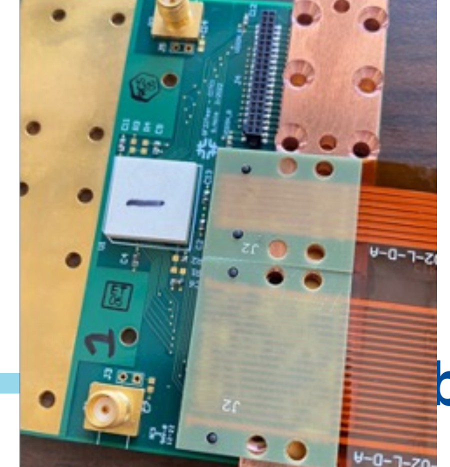
Key Accomplishments in Years 1 and 2

- Quantified performance of High voltage transistors at cryogenic temperatures
- Designed, fabricated and tested 2 DAC channels operating at 7K (up to 100 MSPS, with 1mV resolution for 10V swing)
- Established digital IC flow and built components for on-chip PLL









Year 3 – CITC_v2 (Jan 2023 submission)

- Low power, High Voltage design in advanced geometry node
- 16 DAC channels (10b, 10V, 10 MHz)
- 2 design variations for optimized cryo performance
- 1 MB on-chip memory
- Channels match footprint of ion-trap electrode

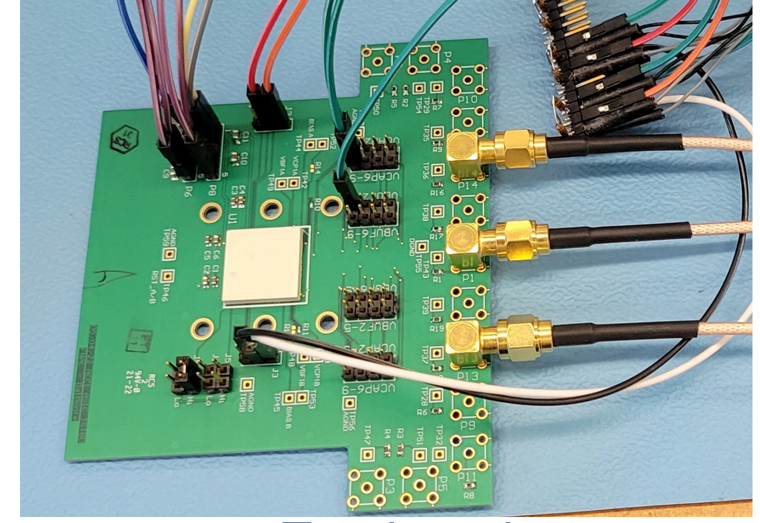
Next steps – Chip testing, integration with ion-traps

Final design to be optimized for 20V operation

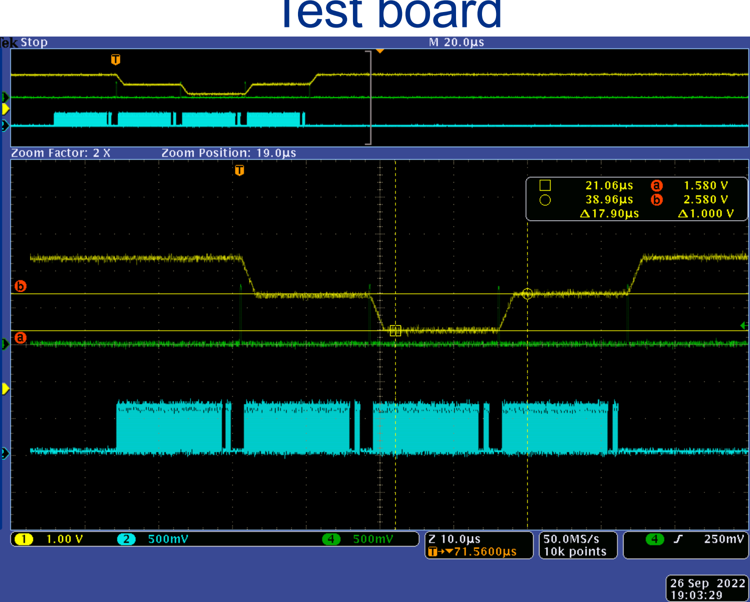
Integrated photonics for low power data transmission

QuantiSed: Portable Optical Atomic Clocks: Joint DOE-DOD

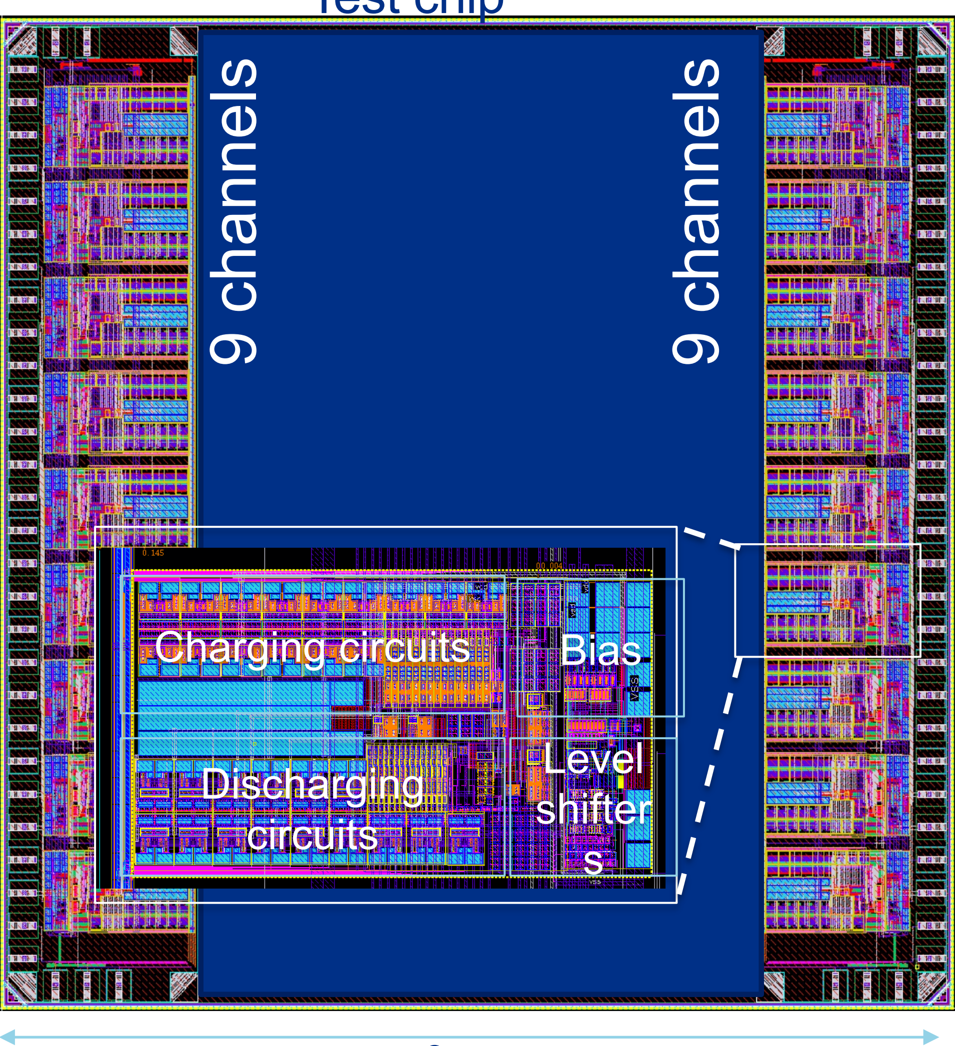
- Demonstrated 1st working prototype
- Next steps: Develop SPAD readout electronics



Test board



Waveforms



Test chip

3 mm

3D-integrated trapped-ion control and readout system

● ○ Ions

1/17/23

Trap/photonics chip

Electronics chip

LDRD: Cryogenic Quantum readout: collaboration with Microsoft

- Parallelization of RF reflectometry for scaling
- High performance ADC development

  12 bits; >50 dB of SFDR; ENOB of 9 at 5 GHz input: ≈ 56 dB SNDR

  10 GS/s at 4K (under 100mW)
- Chip 0, **Mismatch Test Chip Nov 2021**

  Custom capacitor mismatch test, minesweeper
- Chip 1, **Michigan: July 2022**

  Four separate sub-ADCs at 1 GSPS

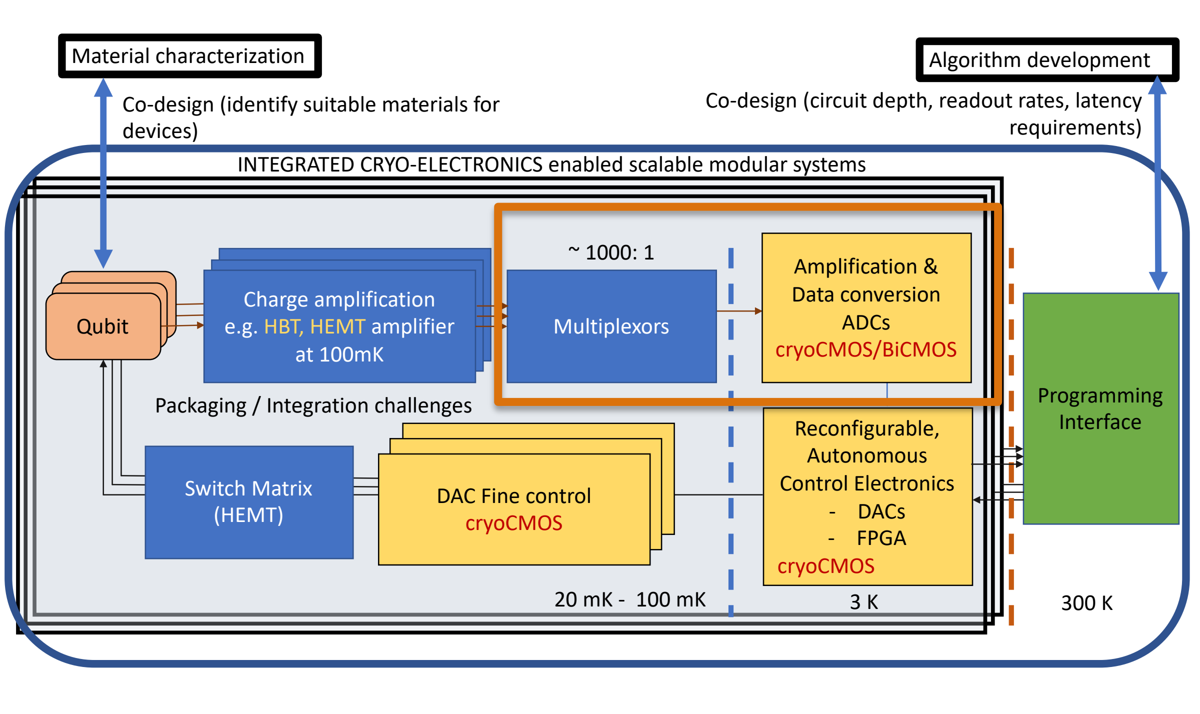
  Full initial PLL
- Chip 2, **Glebe: 2023**

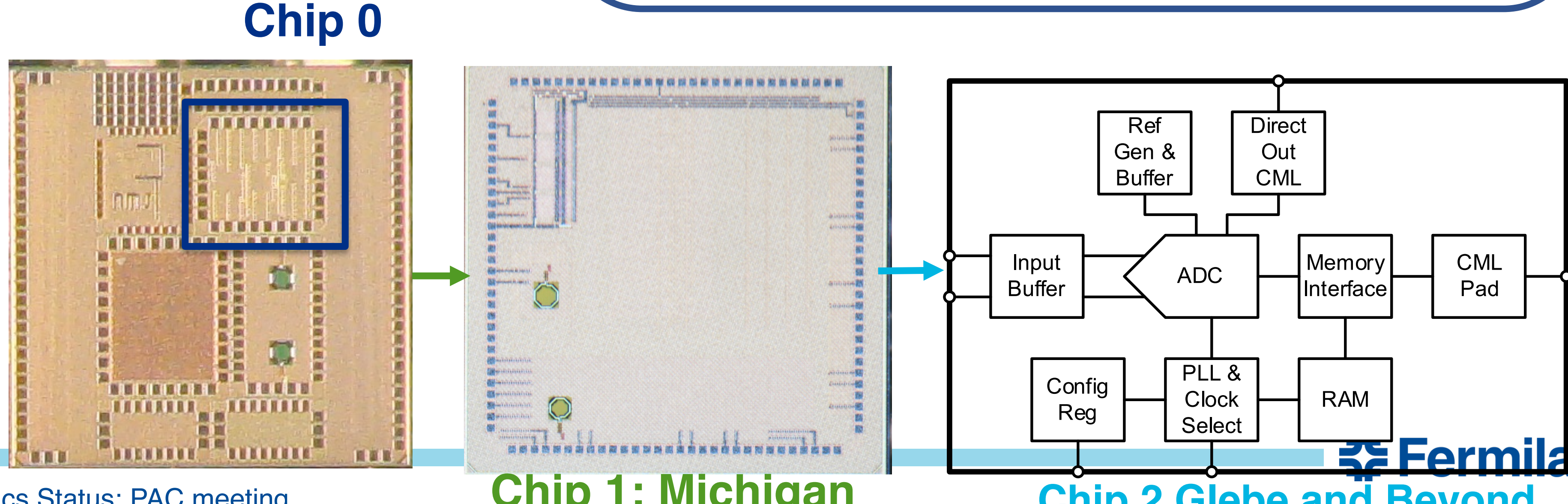
  Interleaving to 10 GSPS

  Refinement of PLL
- Chip 3: **2023**

  Final tuning to state-of-the-art

  custom backend algorithm

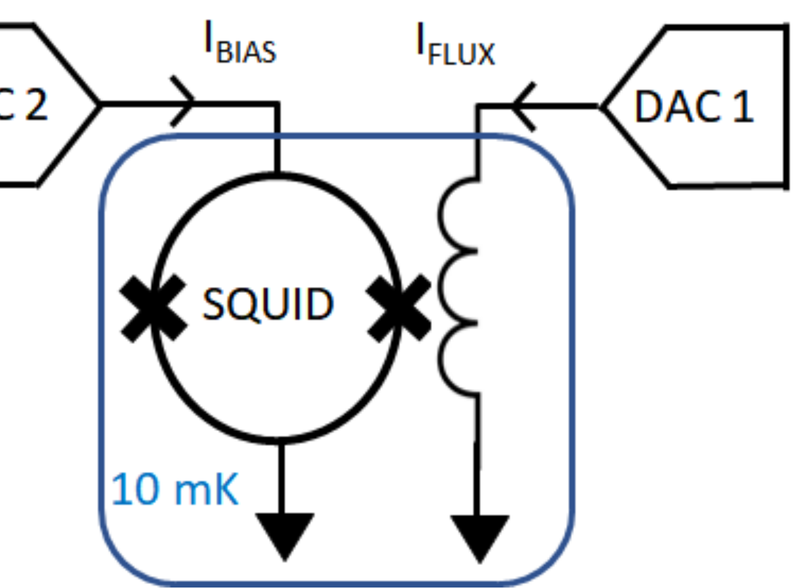




Cryogenic Quantum readout with SQUIDS: collaboration with Qolab

Objective: Design Bias DACs for optimal biasing of SQUIDs (Superconducting Quantum Interference Devices) for qubit readout

- The optimal bias current varies by over 40 % across different SQUIDs
- Independent current DACs required for SQUID current bias and flux bias
- Low power consumption to stay within limited power budget (1 W at 4 K) for 1 Million qubit readout system



- Utilization techniques from HEP pixel detectors which require trim DACs for systematic offset cancellation across large area devices
- Partnership with John Martinis and Robert McDermott

LDRD: Superconducting electronics

- Focus on design and investigate mature fab processes such as MIT LL and SkyWater
- TWPAs and JPAs for ADMX-BREAD using a super conducting fab at MIT LL
- Collaborating with Washington University at St. Louis
- Established design flow for Josephson Parametric Amplifiers (JPA)
- Using JPA design flow as a foundation to study Traveling-Wave Parametric Amplifiers (TWPA)
- Expand beyond TWPAs to other superconducting circuits
- Investigate integration with cryoCMOS for optimized hybrid platform

JPA Simulation

JPA Schematic

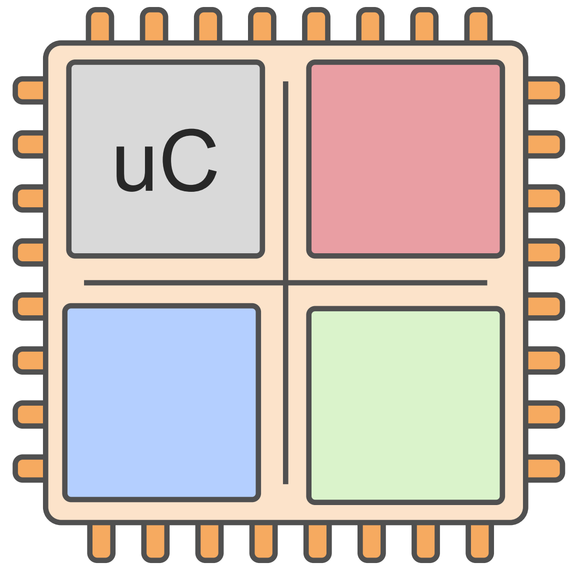
130um

120um

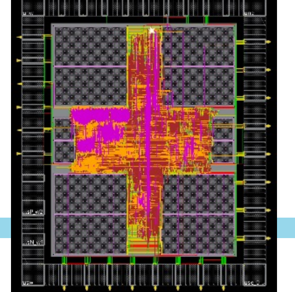
JPA Layout

Scalable Quantum Control

System-on-Chip



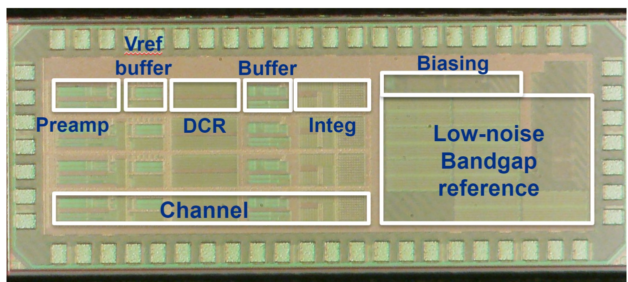
- **Platform for Scalable Quantum Control** = ESP + FlexLogix eFPGA
  - ML running on eFPGA/SoC in the cryostat for scalable quantum control
  - Methodology: hls4ml + Catapult HLS + Synplify + FlexCompiler
  - Architecture: eFPGA integration in SoC tile(s)
- **Quantum control applications**
  - Data acquisition, model training, model evaluation, hardware synthesis
    - State preparation (Control)
      - Workshop on Quantum Computing Software 2022
    - Readout, Error correction
  - Early emulation on FNAL QICK looking for collaborators for demonstration
- **CryoAI, 22nm**
  - Digital test chip to evaluate low power cryogenic performance of digital backend at lower core voltages
  - Design and integration of an ML Accelerator (AutoEncoder for Anomaly Detection – IoT MLPerf Tiny)
  - Chip & board fabricated – Ongoing testing
  - ESP simulation for future respin

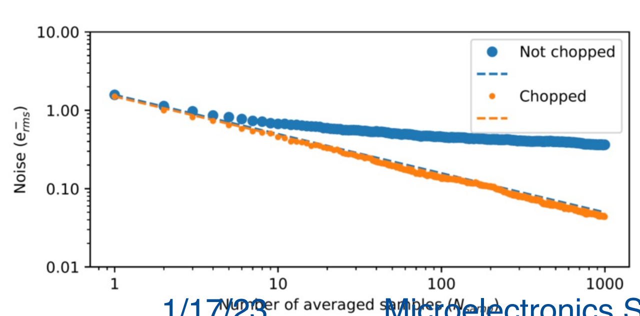


Pixel Detectors:
Skipper CCDs, Pixel detectors R&D for Photon science and next generation HEP detectors

Skipper CCD readout: MIDNA

- State-of-the-art noise performance (~3e- noise performance)
- Cryogenic operation (100K)
- On-chip pile-up up to 7000 without saturation
- 100x lower power, extremely small footprint, significantly reduced cost
- Excellent test performance
- Next: Add on-chip ADC





Skipper CCD-in-CMOS Sensor

- Collaboration with leading CMOS foundry (Tower Semiconductor) to develop Skipper-CCD in commercial CMOS process
- Prototyped ASIC has 400 variations (pixel designs/process splits) to evaluate best design
- Testing underway
- Full-reticle large area prototype to follow
- Would be ideal effect for 3D integration

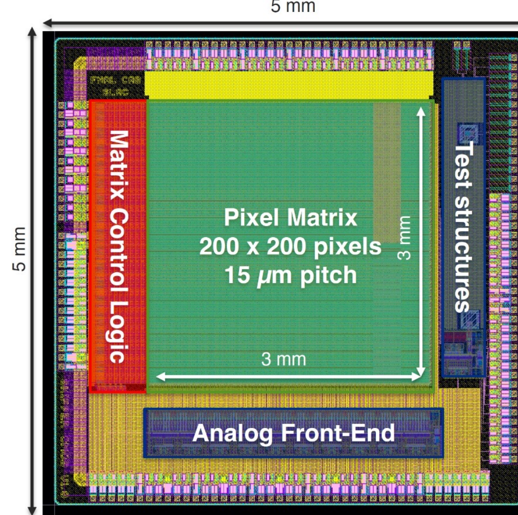
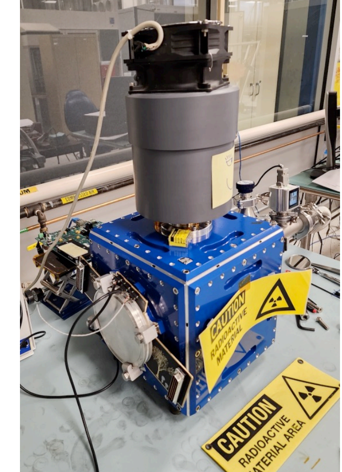
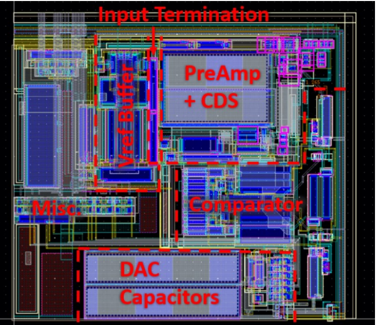


Image sensor ASIC



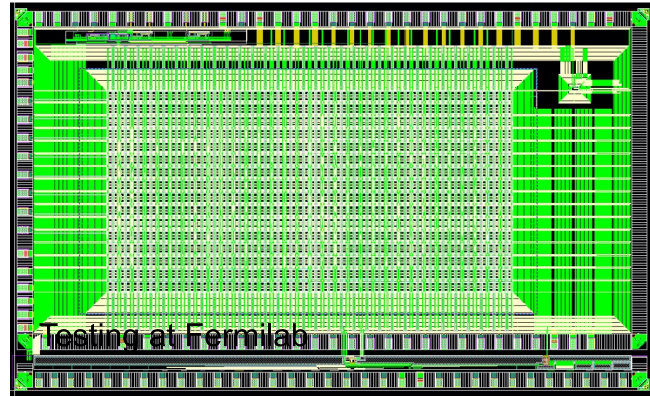
Highly-parallel readout ASIC for Skipper-on-CMOS

- Developed low-power in-pixel ADC for highly parallel readout (→ high frame rates)
- 1st prototype just received for testing
- 2nd prototype with additional features ready (12/22)
- Full-reticle ASIC in 2023



10b, 100KSPS in-pixel ADC (~30x30μm)

SPROCKET ASIC: 64x32 pixels (09/22)

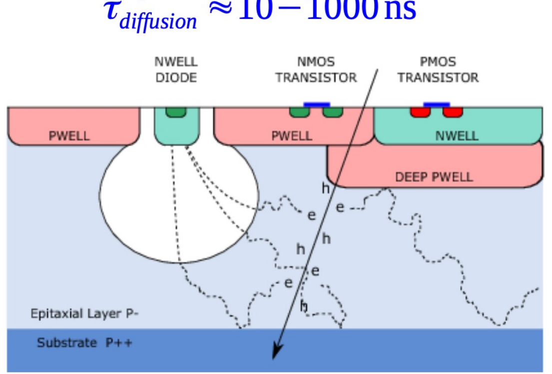


CMOS sensors – New development FY23 and beyond

- Radhard MAPS: **Skywater 90nm** in collaboration with LBL. Evaluating strategic radhard performance of US based foundry
- HV MAPS: Implement MAPS in **GF** 28nm High Voltage process to evaluate performance in deep submicron node. 3D integration provided by GF on this node
- CMOS LGADs/ 3D LGADs collaboration with SLAC and **Tower Semiconductor** in either 180 CIS or 65 CIS process

Standard MAPS

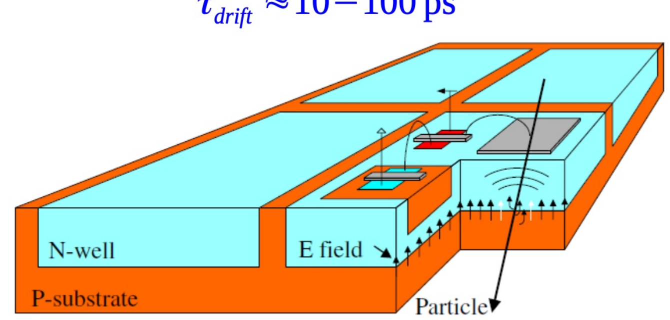
$\tau_{diffusion}^{-1} \approx 10-1000\,\text{ns}$



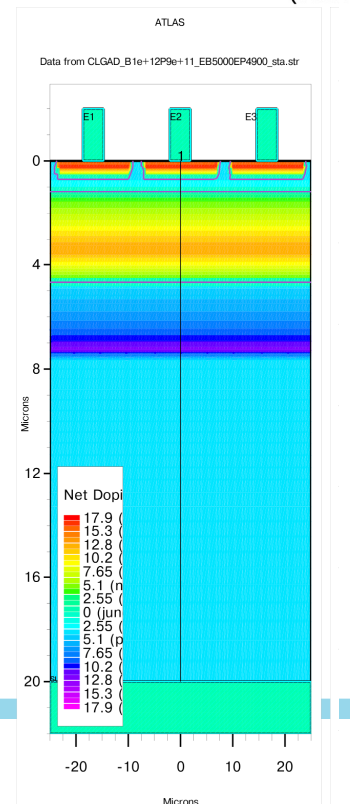
(from Besson et al. 2016)

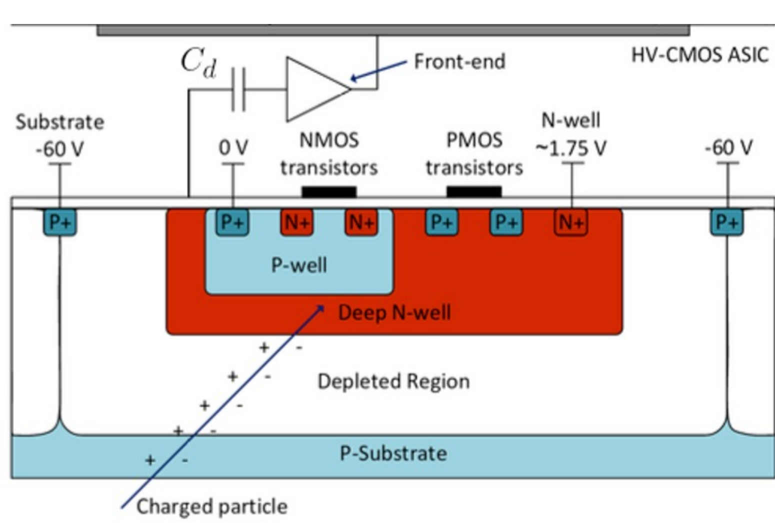
Depleted MAPS

$\tau_{drift}^{-1} \approx 10-100\,\text{ps}$



e.g. High Voltage – Monolithic Active Pixel Sensor
(I. Peric et al., NIM A 582 (2007) 876)

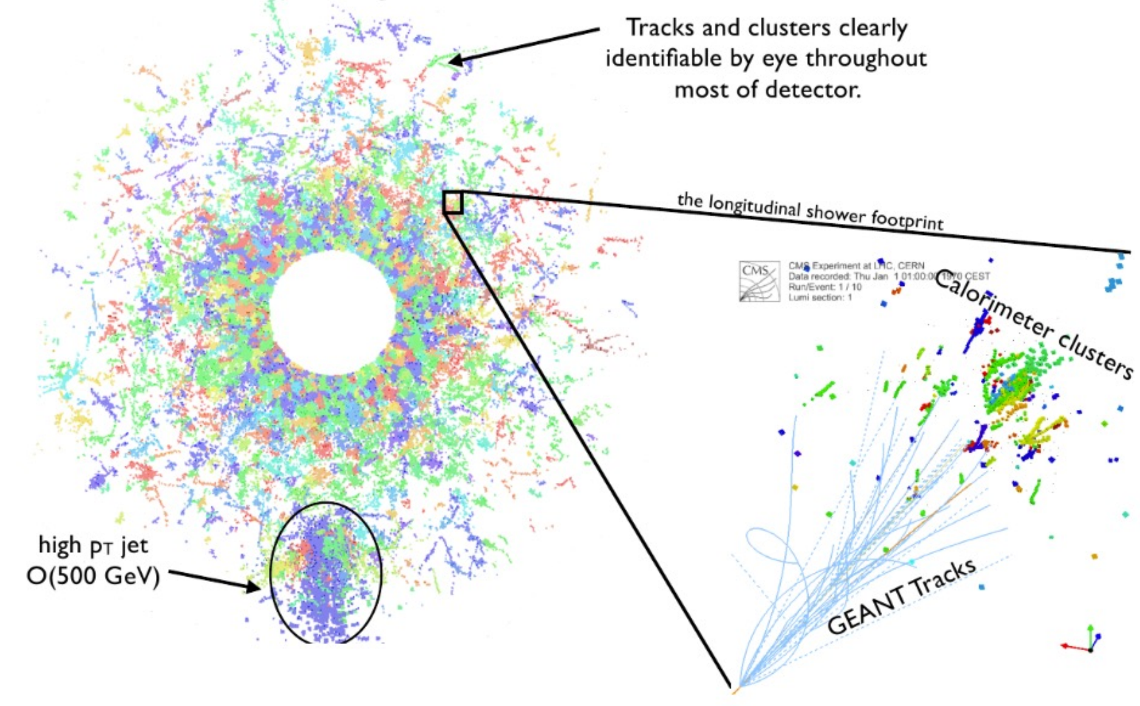


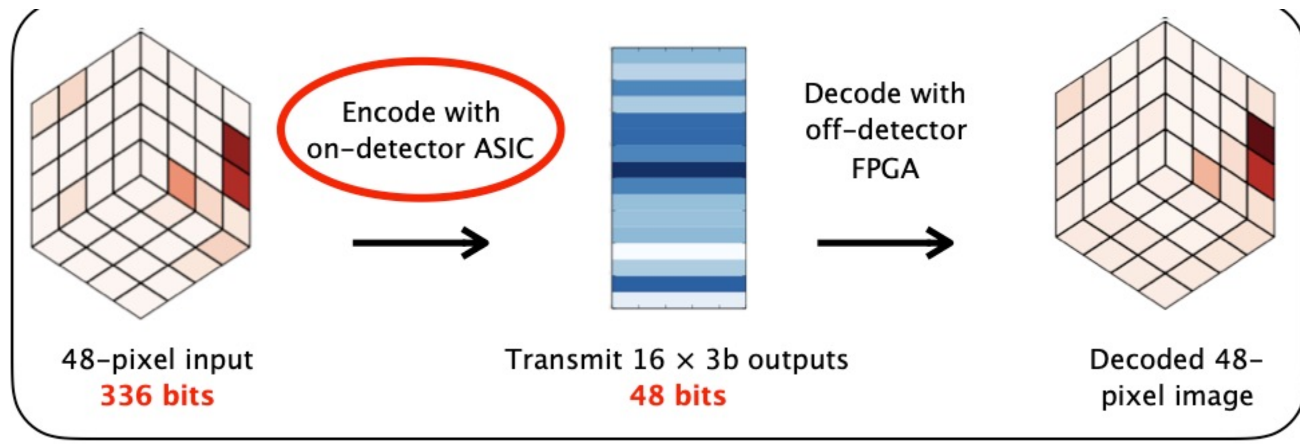


AI: AI-on-chip, Data processing at source for pixel detectors, Classical ML for Quantum readout and control

ECON NN Encoder: Radiation-tolerant data compression with AI

- 5 Pb/s raw data must be reduced on-detector to 40 Tb/s for triggering at 40 MHz.
- Important step in data reduction is 7x compression by on-detector ECON-T ASIC.
- ECON-T includes rad-hard, reconfigurable neural network (NN) encoder inspired by AutoEncoder concept and providing 3-20x compression.





- NN encoder can be retrained / reconfigured for optimized performance according to LHC and detector conditions, location in detector, etc.

Democratizing AI Hardware with an Open Source, Automated AI-Chip Design Toolkit with Discovery Partners Institute

Motivation

Machine learning has proliferated to business activities from identity fraud detection to targeted marketing

First generation AI: primarily algorithmic.

Current AI: Real-time. deployed on custom-hardware,

GPU, TPU, ASIC, etc.

The great AI disparity: Most business users are large

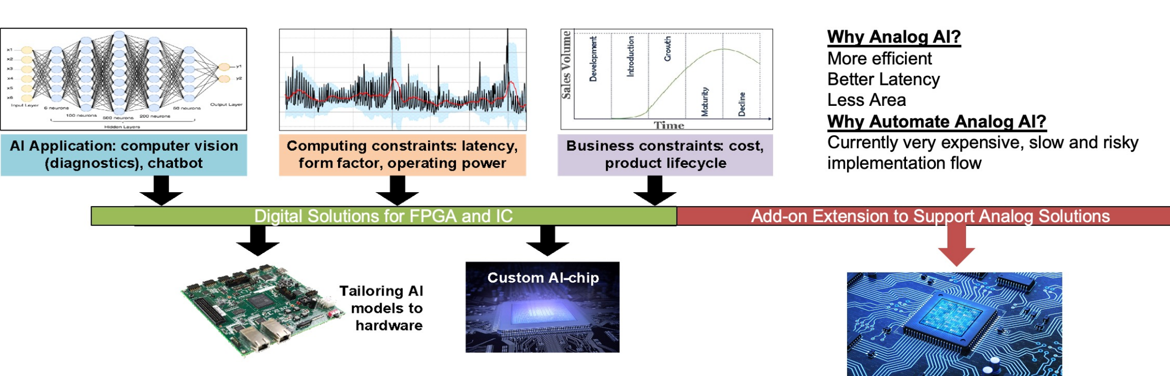
companies (Google, Walmart)

How to democratize AI for small businesses and individual users?

Machine Learning
Business Use Cases
Cognitive Services
Financial Management
User Behavior Analysis
Security Improvements
Improved Automation

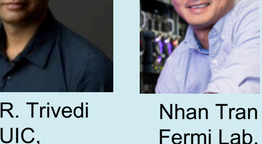
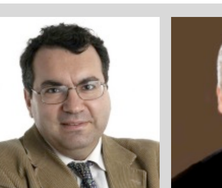
>100B market size, >40% CAGR

Innovation



We automate the automation deployments

Collaboration team

Farah Fahim
Fermi Lab,
ASIC Research & Development Head

Ben Parpillon
Fermi Lab,
Senior ASIC Engineer

Amit R. Trivedi
UIC,
Electrical and Computer Engineering

Nhan Tran
Fermi Lab,
Accelerator-based Experiments

Ahmet Cetin
UIC,
Electrical and Computer Engineering

Mark Neubauer
UIUC,
High Energy Physics

AI-Chip Prototyping and Analog Primitive Automation

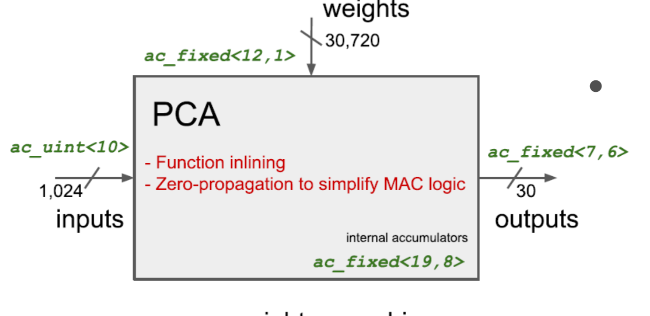
High-Level Synthesis and Digital Automation Flow

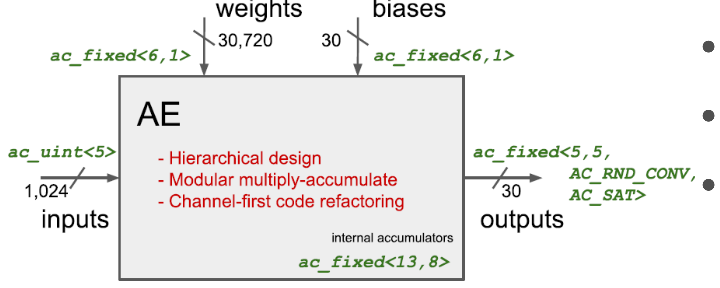
Application Studies: Low Barrier AI for Businesses and Science

Project Overview

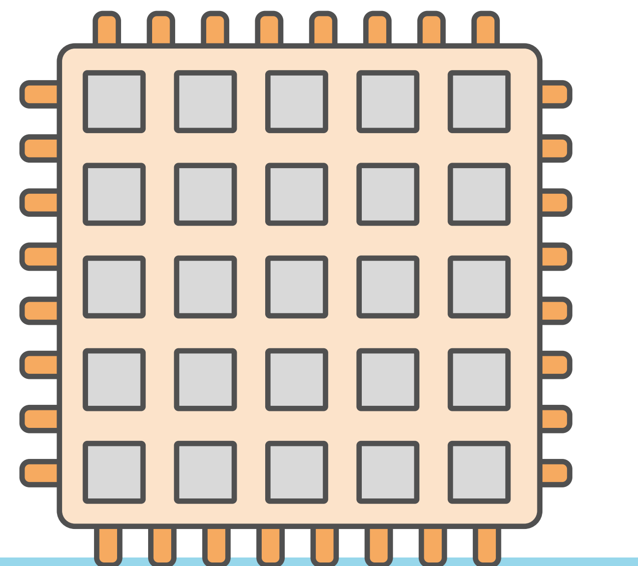
1. Build analog AI model for hardware (1.5 year)
2. Integrate models into HLS4ML tool (1.5 year - overlapping)

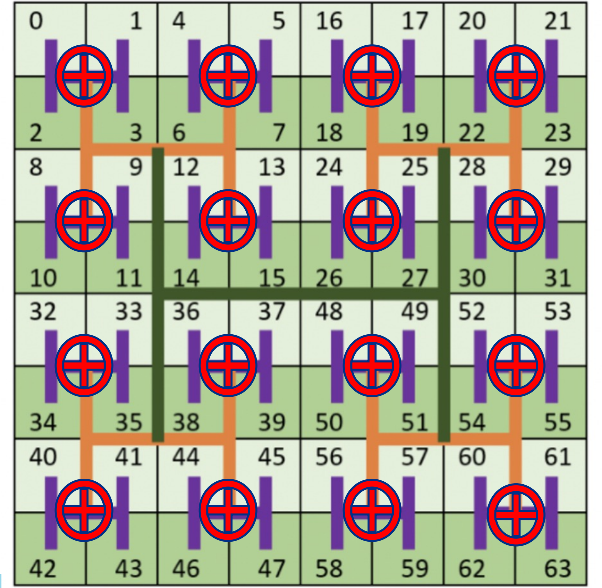
AI-in-Pixel for at-source data processing

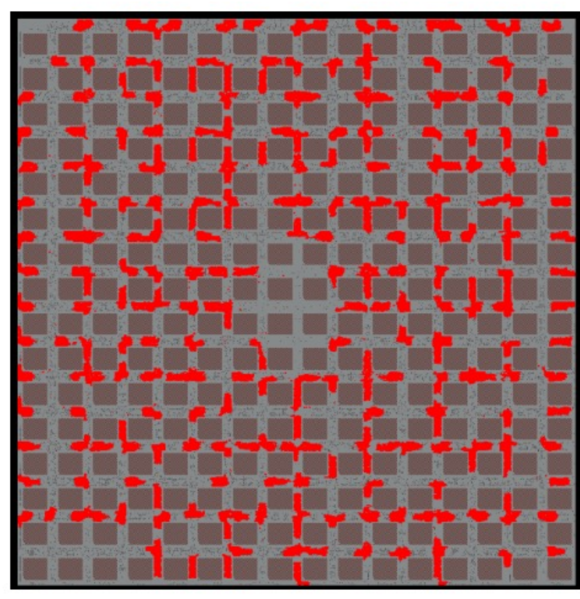




- **Lossy data compression at source for X-ray detector, 65nm**
  - Comparison of two algorithms synthesized with Catapult HLS (+ hls4ml)
    - (Auto)Encoder, 70x compression, 30 clk lat., +21% overall area
    - Principal Component Analysis, 50x compression, 1 clk lat., +44% area
  - IEEE International Symposium on Circuits and Systems 2023
  - Tapeout on Dec. 7th, 2022 → Testing Spring 2023
  - Learnt best practice for HLS and PnR



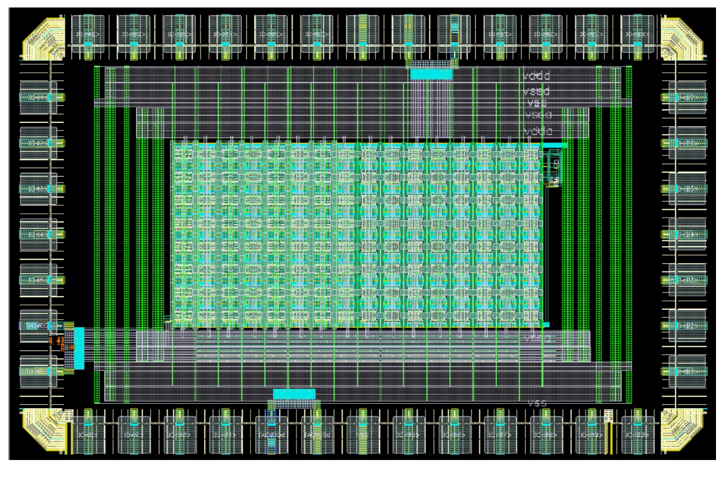




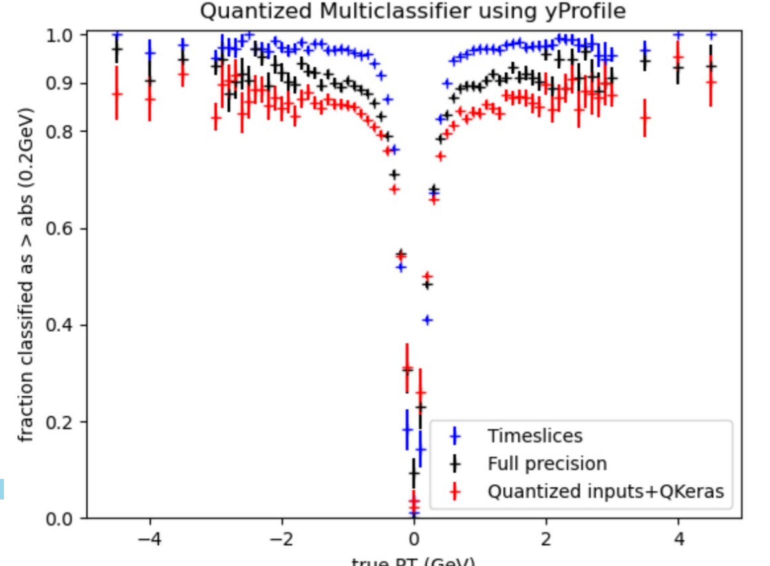
AI-in-pixel

Operation in extreme conditions – high ionizing radiation, cryogenic operation with long lifetime requirements

- Smart Pixels: CMS pixel detector replacement R&D: 25μm pixel pitch in TSMC 28 nm with on-chip neural networks for data filtering and data compression for readout at 40 MHz
- On-chip binary classifier for rejecting tracks with momentum >0.3GeV to achieve > 50% data reduction in innermost layers
- Working with Sandia National Lab for beyond CMOS ReRAM implementation of the algorithm (Sandia Grand Challenge initiative)



28 nm chip with 32 x 16 pixels



	Fraction correctly predicted	
	> 1 GeV	> 2 GeV
Timeslices	97.30%	97.60%
Full Precision	91.00%	92.60%
Quantized Inputs + QKeras	85.80%	87.20%

Conservatively reject:

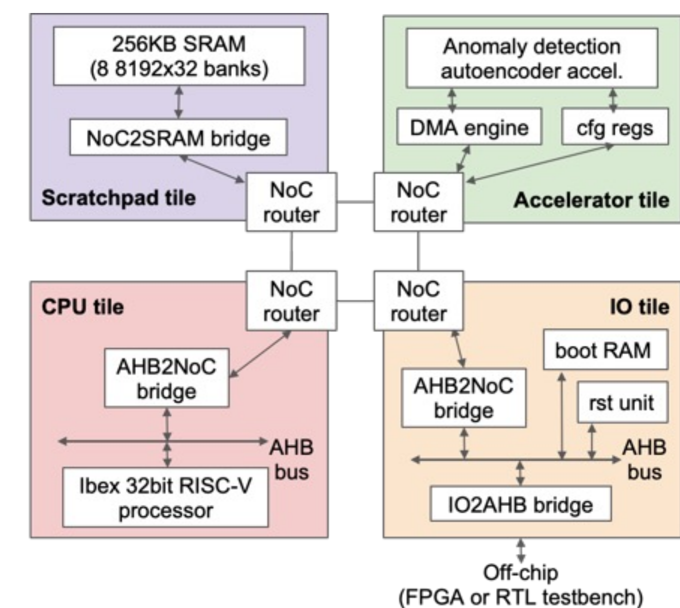
< 0.2 GeV	≥ 6%
< 0.5 GeV	≥ 36%
< 1 GeV	≥ 70%
< 2 GeV	≥ 94%

~20x reduction

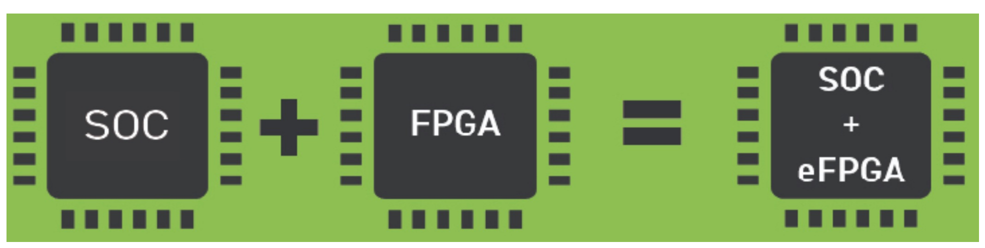
Reconfigurable Edge AI – Solve the HEP data challenge

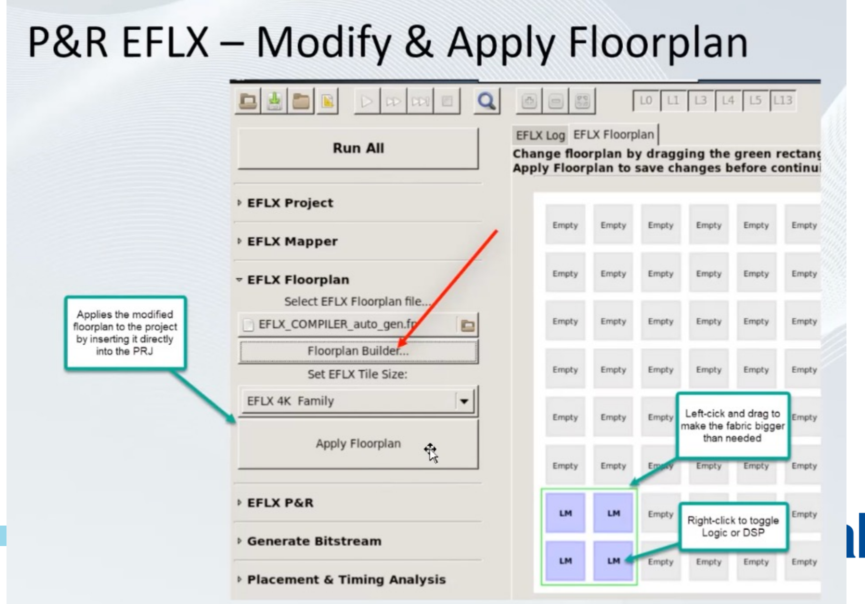
- Collaboration with Columbia U. & Northwestern U.
- Edge AI: Combining two established open-source platforms (ESP and HLS4ML) into a new system-level design flow to build and program a System on chip

  In the modular tile-based architecture, we integrated a low-power 32-bit RISC-V microcontroller (Ibex), 200KB SRAM-based memory, and a neural-network accelerator for anomaly detection utilizing a network-on-chip.



- Embedding FPGAs on detector: Radhard/ cryogenic eFPGA on-chip – with Flex Logix (22nm / 28nm). Establishing design flow and investigating extreme environment performance





DOI Microelectronics co-design

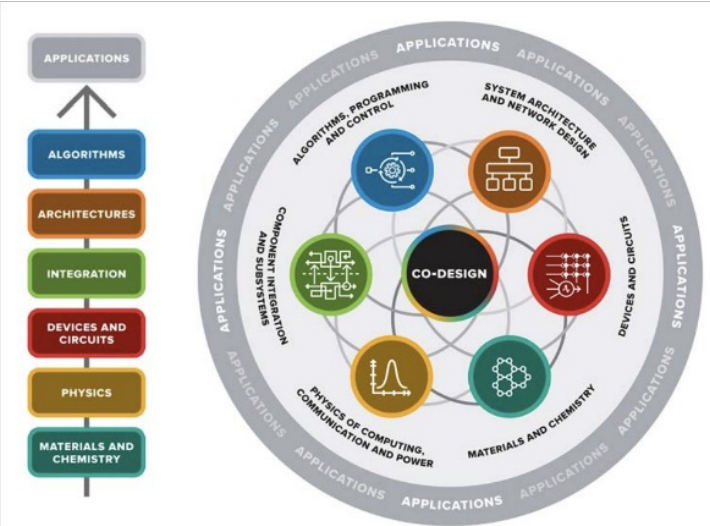
New DOE Microelectronics Initiatives

DOE Microelectronics Codesign Teams:

"Hybrid cryogenic detector architectures for sensing and edge computing enabled by new fabrication processes"

Fermilab led jointly funded by HEP + BES + ASCR + FES

- Massively parallel readout for x1000 speed improvement of Skipper-in-CMOS: SPROCKET
- Development of rad-hard particle detectors based on superconducting nanowires for fast timing (EIC)
- CryoCMOS and beyond-CMOS superconducting electronics for edge computing
- Cryogenic system integration for scaling



CMOS and beyond CMOS for rad-hard neural networks

- Rad-hard, Neuromorphic Neural Network for front-end data processing
- Beyond-CMOS: Blue Sky R&D
- CMS Pixel detector replacement R&D (TSMC 28 nm)
- Working in conjunction with **ORNL-led codesign team - ABISKO**

Abisko Codesign Overview

Collaborator

“Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes” (HYDRA)

HEP

Development of Skipper-in-CMOS and large-area, high-rate single photon imaging

Novel fast timing cryogenic detectors (e.g. high-η detectors, beam instrumentation)

Integrated sensing and edge computing.

BES New materials, synthesis, and fabrication for superconducting devices

ASCR Novel low-power computing architectures based on superconducting nanocryotron

FES Rad hard cryogenic instrumentation

NP Identified detector applications for the EIC as well as high-flux fixed target experiments (JLAB)

Cryogenic operation
Large channel count
Pico-second timing
Photon resolving
Position resolution

Particle tracking and ID
Dark Matter
Single γ imaging
Spectroscopy
Material science

ENERGY DISTRIBUTION OF THE UNIVERSE
DARK ENERGY 69%
DARK MATTER 26%
NORMAL MATTER 5%

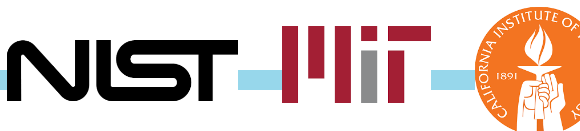
Power optimization
Multiplexing
Impedance matching
Discrimination
Event selection and feature extraction

I_{bias} I_{out} I_{gate} ON

Cryogenic sensors
Superconducting readout electronics
Physics Applications
Architecture
Fabrication
Integrated sensing and edge computing
CryoASIC
Hybrid and monolithic integration

Low-power, low-noise front-end
High speed time tagging
Large channel/pixel count
Low latency control of superconducting electronics and detector
Edge computing and feature extraction
Data buffering and high-speed links

Hybrid bonding
Monolithic integration
Superconducting interconnect technology
(Indium BB + superconducting multi-chip interposer)



Synergies with other Microelectronics Codesign Programs:

- Nitride materials and interfaces for radiation hard integrated neutron detection (Nancy Haegel, NREL):

  Design of readout ASIC to demonstrate AlGdN neutron sensing

- Abisko: Designing Neuromorphic Hardware, Software, and Applications Concurrently using AI-enabled Methods (Jeffrey Vetter, ORNL):

  Design of SNSPD and nanocryotron-based Spiking Neural Network

Recent highlights

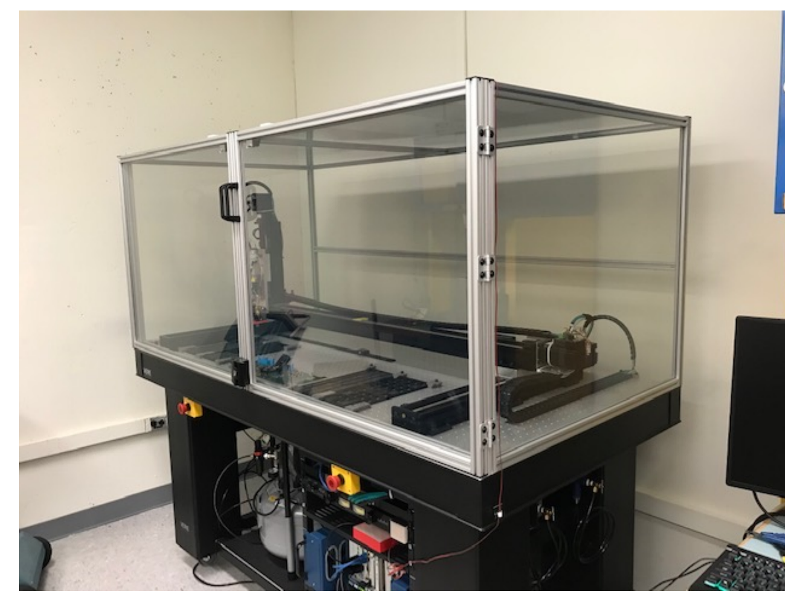
- Collaboration meeting at Fermilab
- SNSPD test beam at FTBF
- Cryogenic TDC ASIC tested at cryo (<5ps jitter)
- Several cryogenic ASICs currently in test or design phase

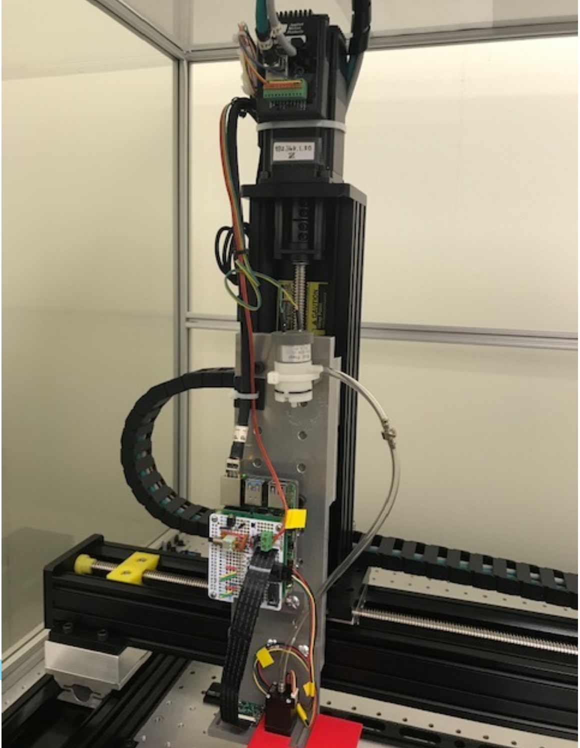
Recent Collaboration Meeting at Fermilab (Jan23)

Testing and Tools

Testing and Characterization

- Extensive expertise, equipment, and experience for ASIC evaluation
  - One stop shop for custom hardware, firmware, software
- **In-depth bench testing** and characterization
- **Cryogenic** test stands, both 77K and 4K
- **Radiation** testing at Fermilab Irradiation Test Area
  - total ionizing dose, single event effects, displacement damage
- **Robotic chip tester** for quality control for major productions
  - Test ~100k chips in 30 weeks





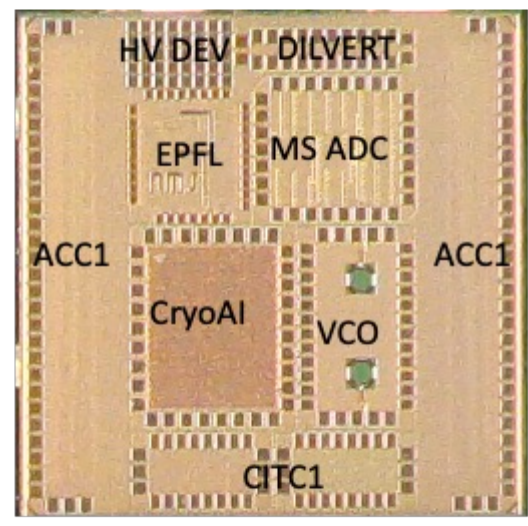
Testing

GF22TestChip1 – 8 designs

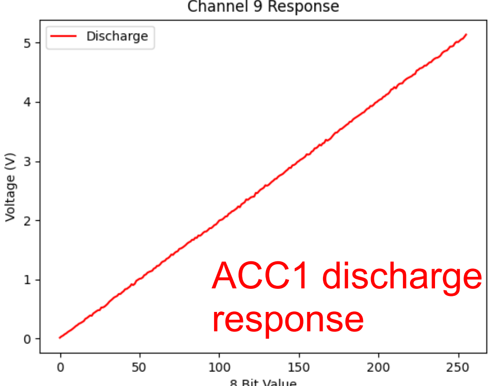
- MS ADC – complete
- CITC1 – complete, but restarting testing
- HV DEV – RT/Cryo complete
- ACC1 – RT complete, continuing at MIT-LL
- DILVERT (TDC)– RT/Cryo complete
- CryoAI – currently under test
- VCO – not working

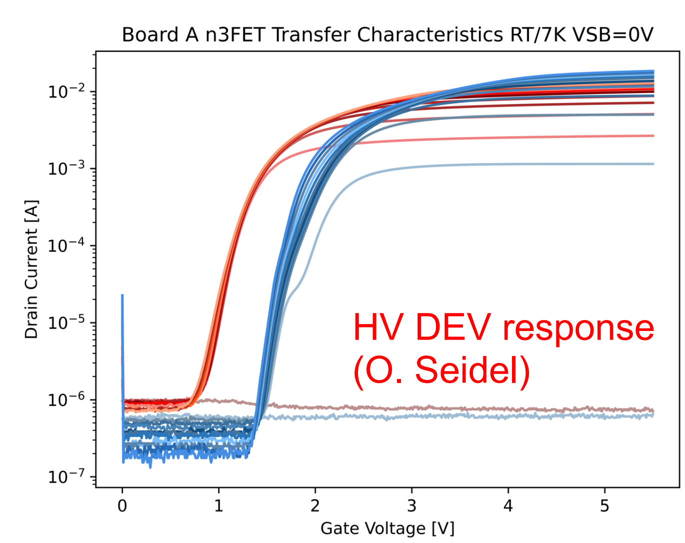
Upcoming

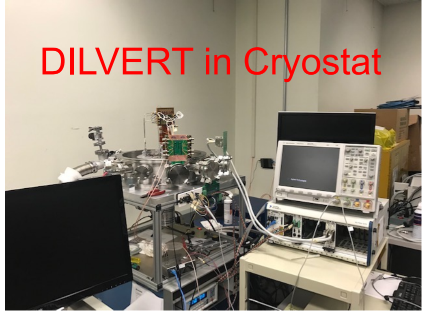
- Michigan (MS) – expect board end of Jan.
- SPROCKET1/2 – starting up
- CMS_PIX_28



HP 4145B PA for HVDEV







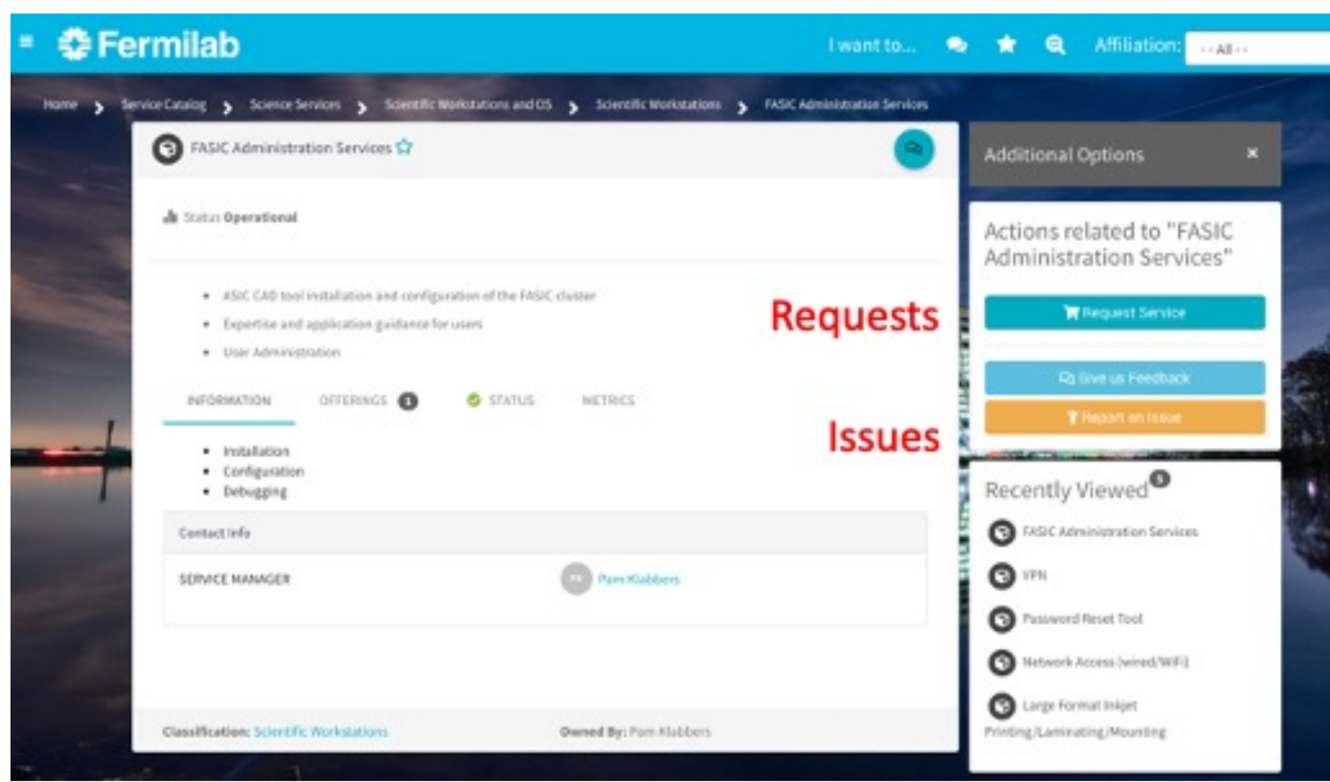
ASIC Tools Support

Please use our FASIC Service Portal in 2023!

- Search for “FASIC” in Fermilab service desk
- Requests – non urgent matter
- Issues – show stoppers

Disk Space Issues

- /asic is 91% full
  - Includes PDK, Projects, and Tools
  - Please cleanup /asic/projects – remove or tar old work areas please!
  - We will address this further in 2023 with help from SLAM team
- /tmp is getting overloaded on beast1 and beast2
  - Please clean up old files



ASIC Design for DOE – key hurdles

Electronic Design Automation – Computer Aided Design (CAD-EDA) Tools

- 3 major CAD tool vendors + other subsidiary vendors
- Cost of licenses is high (these are already discounted prices (60 – 90%
- Obstacles with growing design teams
- EU – has successfully setup "Europractice" for research licenses at education prices (<<< prices available in the US)
- Consolidated effort required to negotiate low cost – high volume licenses

Design IP

- Fundamental IP for IC design
- Basic IP provided by foundry or 3rd party.
- Free basic IP – essential for design
- Paid IP also available (e.g. building blocks such as ADC, high speed drivers and receivers etc.)
- Requires changes to legal framework as a workaround to indemnification clauses
- Multi- party NDA for collaboration

Foundry – Fabrication

- MPW vendors (IMEC, IMEC-USA, MUSE, *MOSIS* etc.)
- Large foundries – e.g. GF, TSMC, Tower Jazz
- Several smaller foundries (Skywater, IHP)
- CERN negotiated lower-price, smaller sizes, easier access for TSMC (previously similar agreement with IBM)
- Multi-party NDAs for collaboration across labs and universities
- Smaller die size to enable easier R&D

DOE microelectronics: Tools and IP access program

ICPT Agreements

Procurement Professionals wanting to buy from an existing agreement?

ICPT BOA by Alphabetical

DOE Federal Instruments for Eligible Contractor Use

The ICPT was Established to:

Aggressively pursue strategic sourcing opportunities that represent procurement leveraged spend that results in a lower total cost of ownership for DOE Complex Wide Site and Facility Contractors;

Provide long term strategies via an established Executive Steering Council, and individually chartered Commodity Teams and;

Provide communication on strategic sourcing initiatives, marketing methodology and procurement related issues to the Site and Facility Contractor community via the ICPT Site Champions.

Consists of member from each of the 17 national labs

Currently started vendor discussions with:

- Cadence, Siemens and Ansys

- Looking to start discussion with other vendors

Thank you