Preliminary Results of CRP5A Cold Runs

Shanshan Gao on behalf of BNL CE Team

12/13/2022

Overall Progress

- Previous updates on 11/22/2022
  - Volodya's presentation in DUNE TPC Consortium meeting 11/22/2022
  - https://indico.fnal.gov/event/57259/contributions/255062/attachments/161909/213826/CRP5a_update.pdf
  - Electrical safety review passed (11/18/2022)
  - Cryogenic safety review passed (11/21/2022)
  - The setup is approved for operation, both at RT and CT
- First Cold Run from 11/30/2022 to 12/03/2022
  - 11/30/2022, cold test started, LN2 filling took ~10 hours
    - cool-down monitoring, initial checkout, debugging
  - 12/02/2022, LN2-refilling
    - A complete measurement was performed
  - Data analysis is ongoing
- Second Cold Run 12/12/2022 to 12/13/2022
  - 12/12/2022, cold test started, LN2 filling took ~9 hours
- Third Cold Run scheduled on 12/22/2022
  - CRP5A will be flipped over with CRP plane face upside

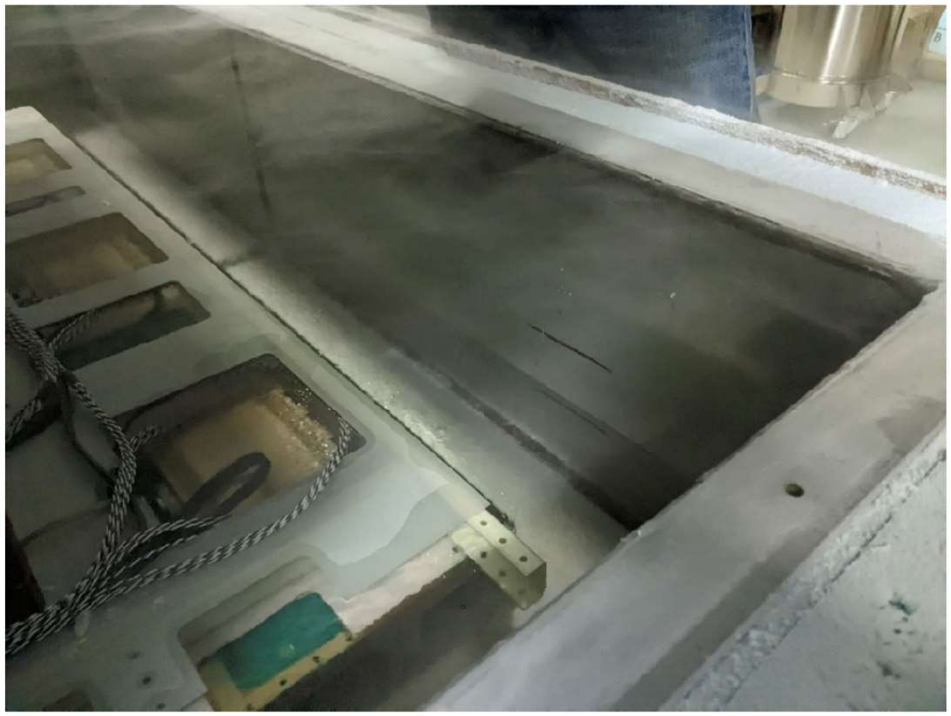
Coldbox First Filling

- The first filling started at 9:18 am on 11/30/22
- Filling for 9 hours until ~6:20 pm on 11/30/22 to ~18 cm level
- Filling direction from the 6000-gallon LN2 storage dewar outside highbay lab
- Oxygen level monitored by the lab safety with environmental measurement and personal monitoring
  - Occasionally trigger the personal monitor when close to the vent and access the CRP
  - No environmental monitor triggering
  - ODH assessment confirmed

Provided by Yichen Li

Some photos for Initial Fill

6.7 hours



9.1 hours Filling stopped

Provided by Yichen Li

https://www.phy.bnl.gov/bnlif/docdb/0003/000331/002/CRP_coldbox_fill_sum.pdf

Many thanks to Yichen to conduct the whole cooling operation

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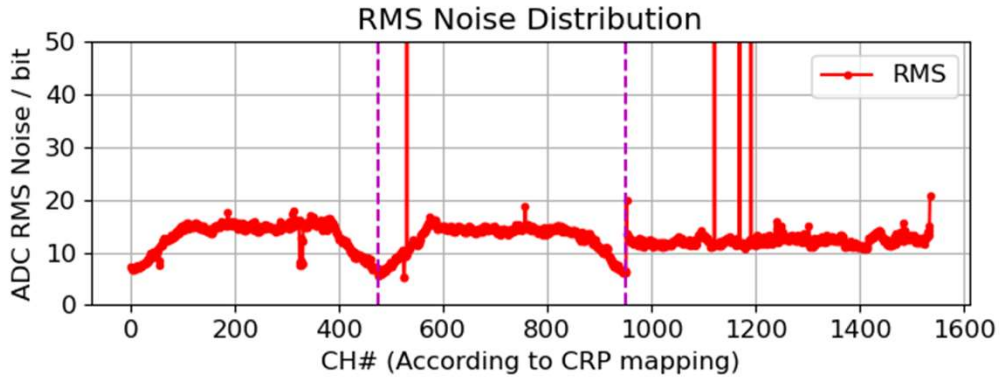
HV Bias Measurement

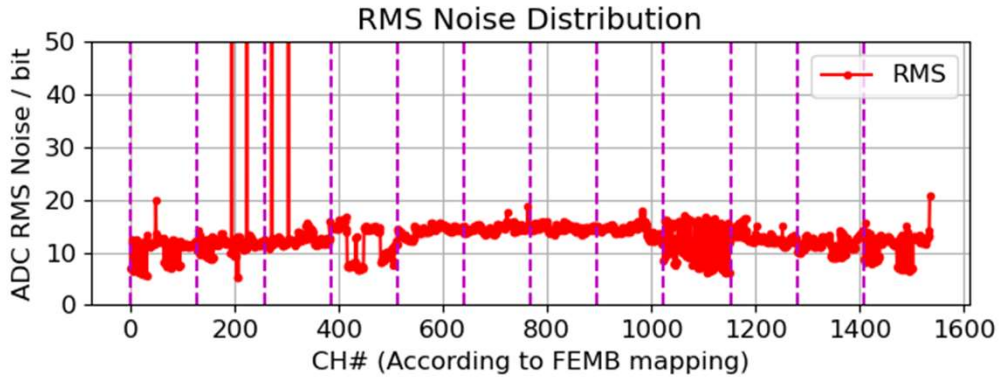
- The nominal voltage for the shield plane (S) is -1500V, for induction 1 (I) is -500V, and collection (C) is +1000V.
  - The only current drawn would come from leakage in the capacitors.
  - MPOD HV modules can measure bias current at 0.01uA resolution
- At room temperature
  - μA level currents were observed when bias voltages were raised to 10V
    - These could be humidity related
- At cold
  - 0 μA when V is less than 300V
  - Half bias voltages
    - C (500V) = 0.00 μA, S(-750V) = 0.00~0.01 μA, I (-250V) = 0.00 μA
  - Full bias voltages
    - C (1000V) = 0.01 μA, S(-1500V) = 0.02~0.03 μA, I (-500V) = 0.00 μA

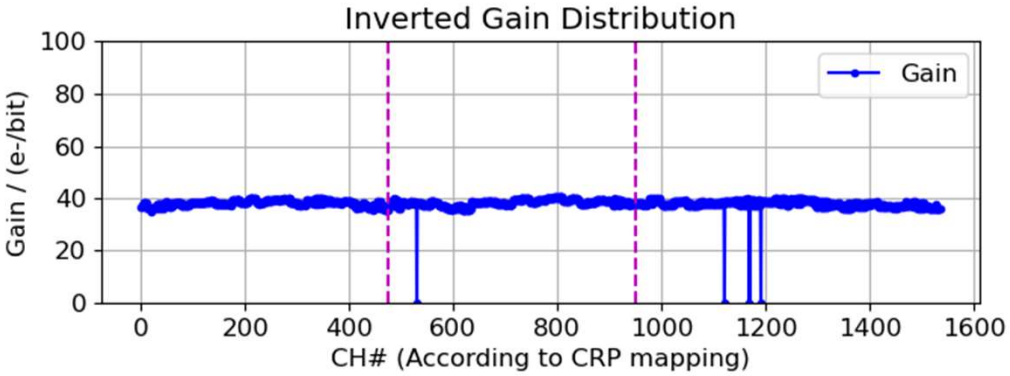
CRP5A Cold Test Result (BNL)

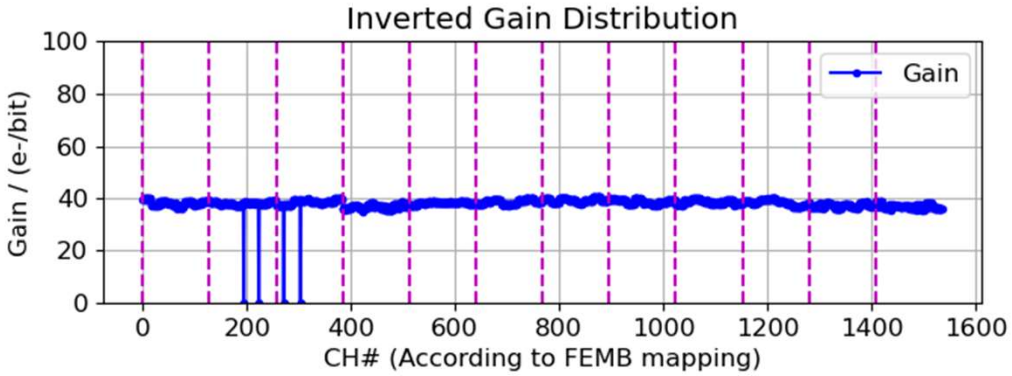
Preliminary Result

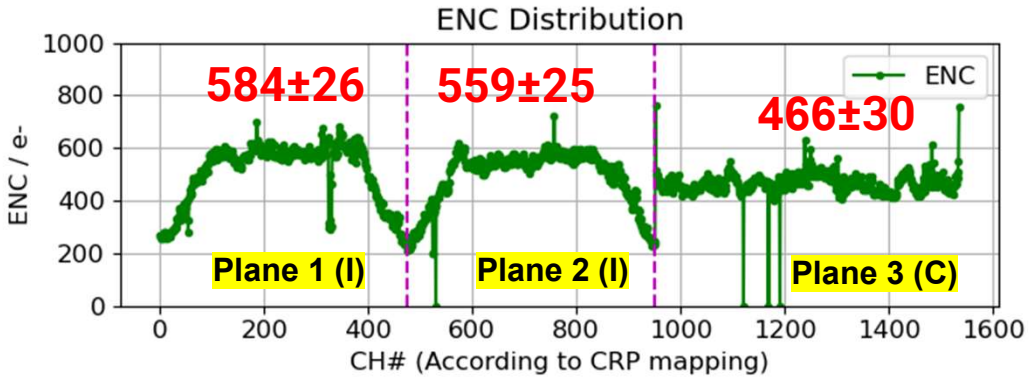
HV BIAS on, 900mV baseline, 14mV/fC gain, 2.0us peak time

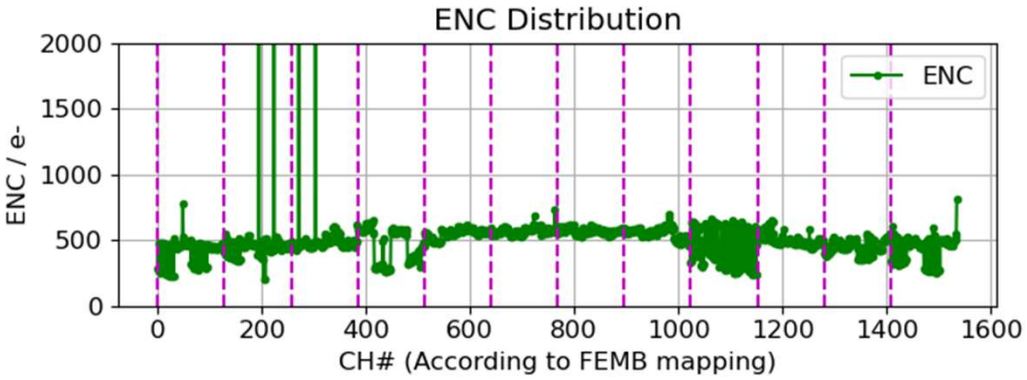










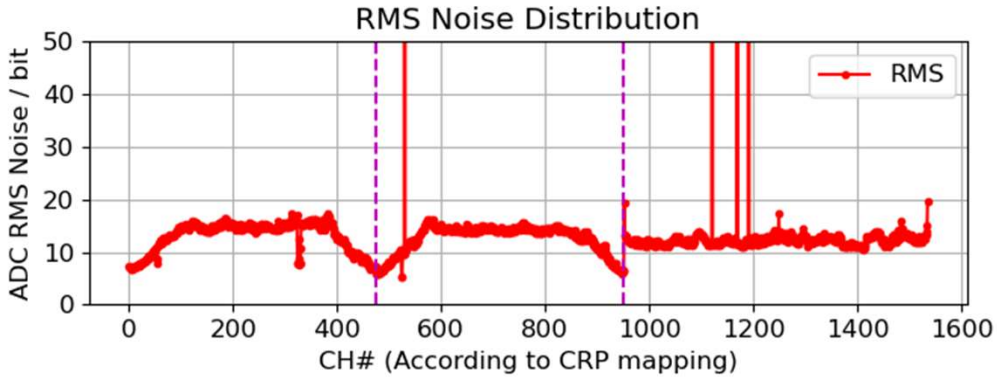


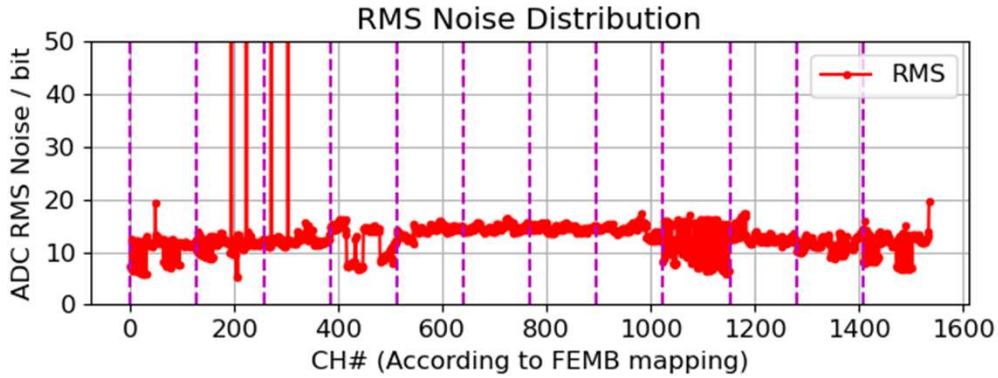
note: observed extremely large noise and abnormal gain on ch#194, 223, 271, 303. Set them gain to 0.

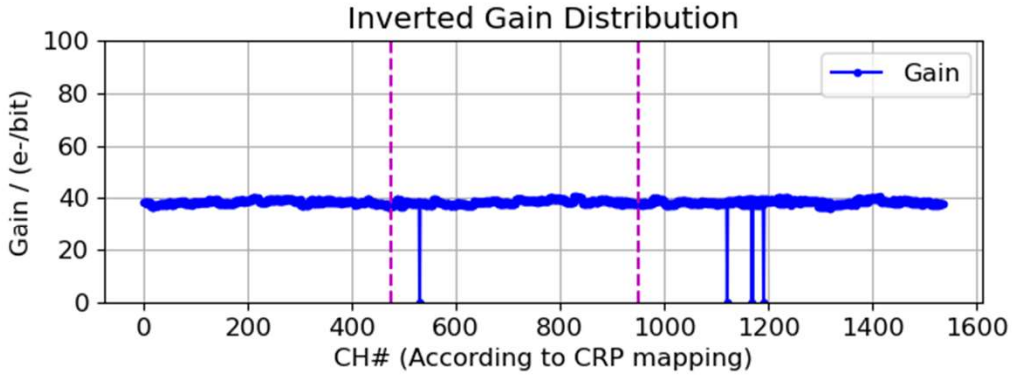
CRP5A Cold Test Result (BNL)

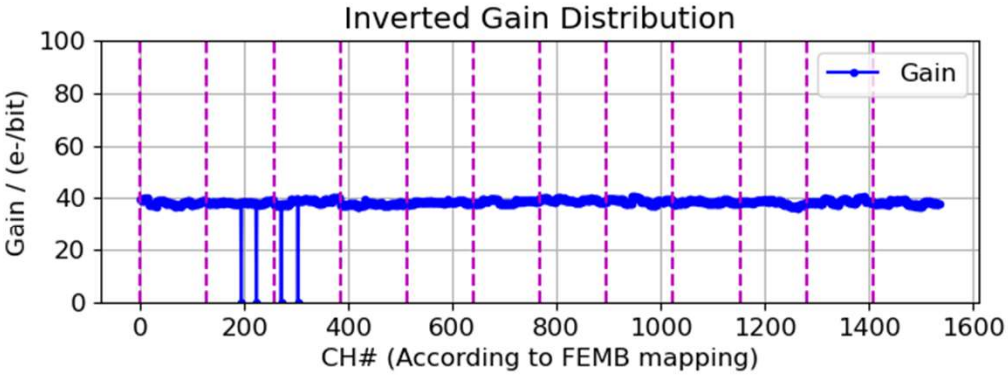
Preliminary Result

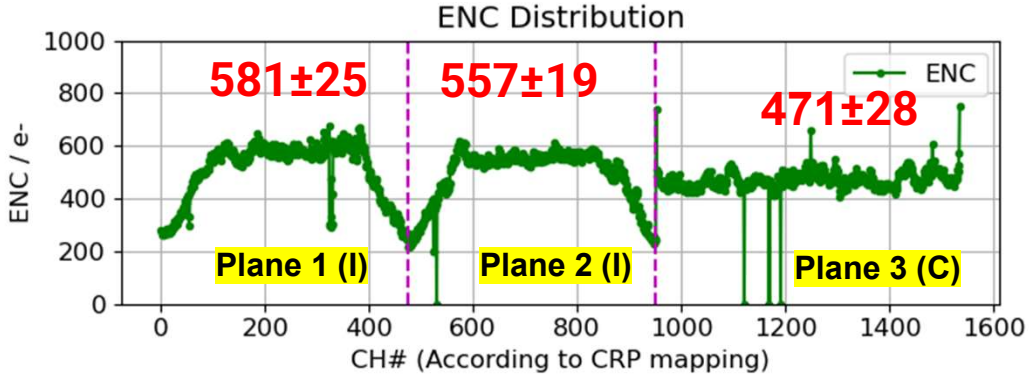
HV BIAS on, 200mV baseline, 14mV/fC gain, 2.0us peak time

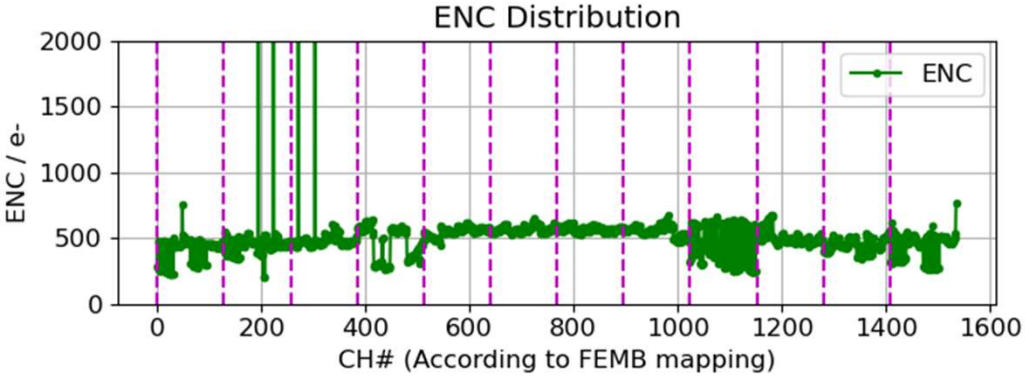










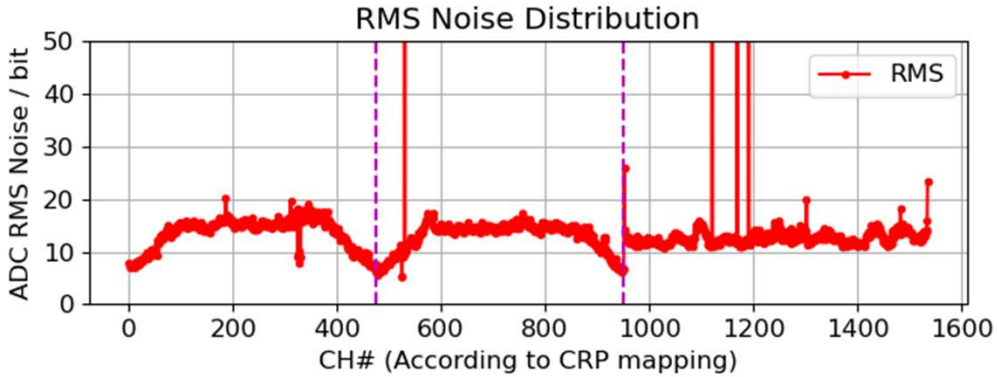


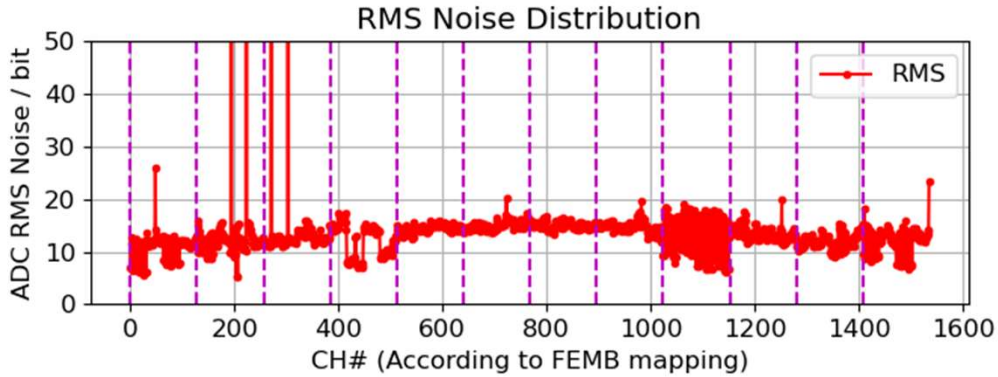
note: observed extremely large noise and abnormal gain on ch#194, 223, 271, 303. Set them gain to 0.

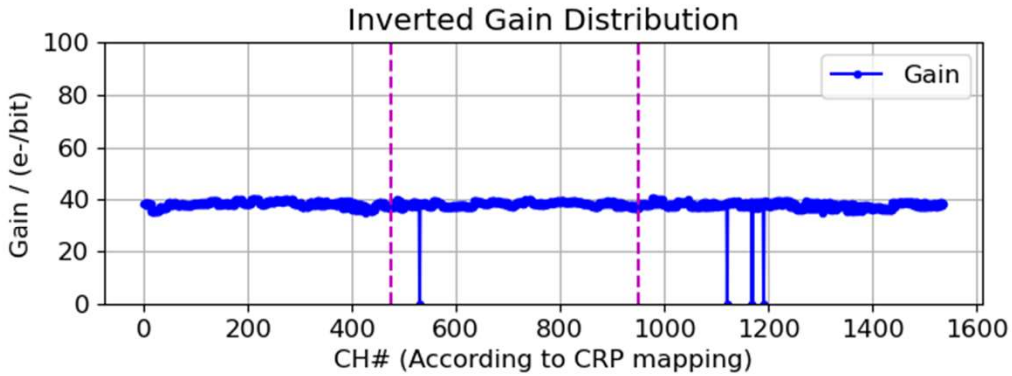
CRP5A Cold Test Result (BNL)

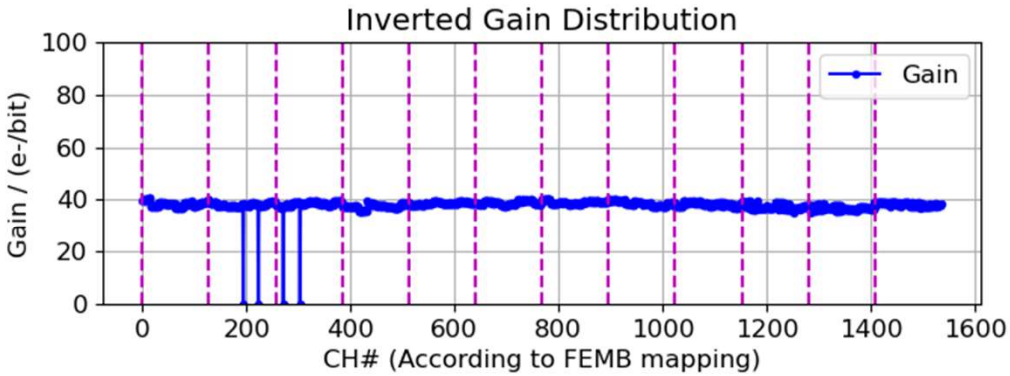
Preliminary Result

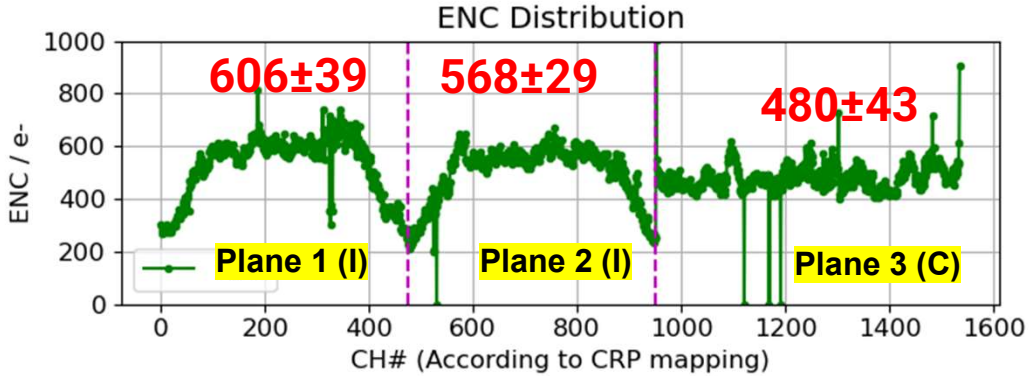
HV BIAS on, 900mV baseline, 14mV/fC gain, 3.0us peak time

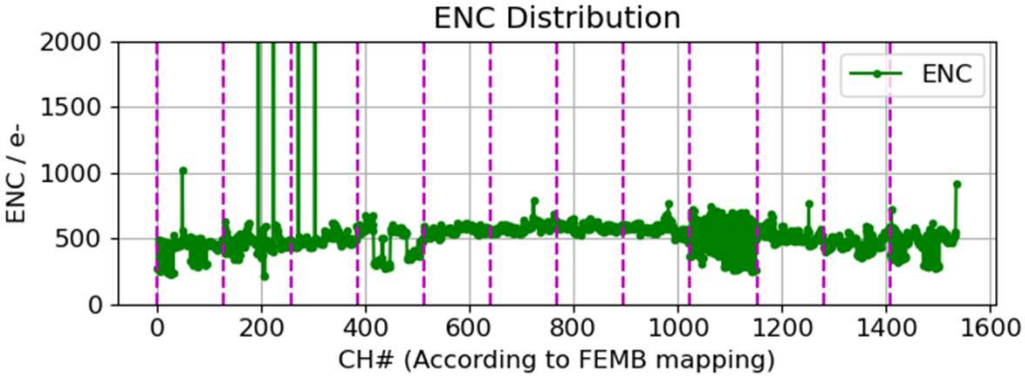










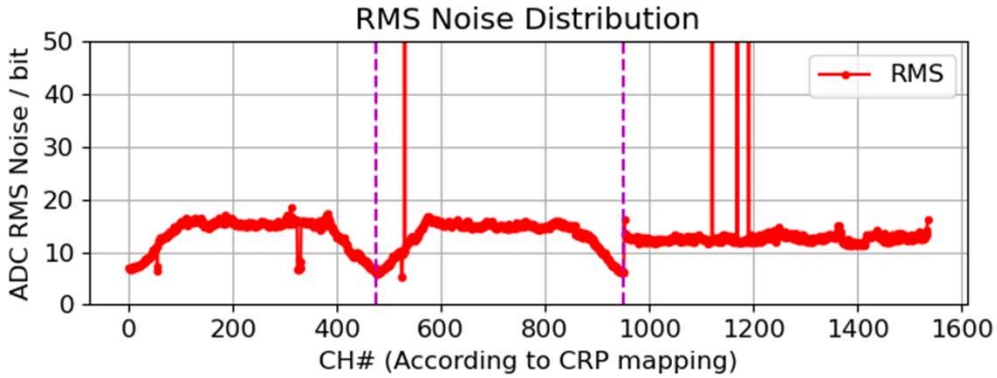


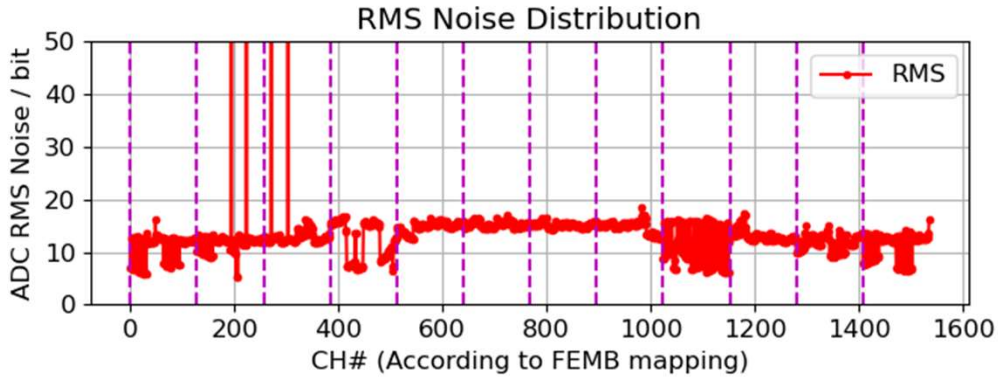
note: observed extremely large noise and abnormal gain on ch#194, 223, 271, 303. Set them gain to 0.

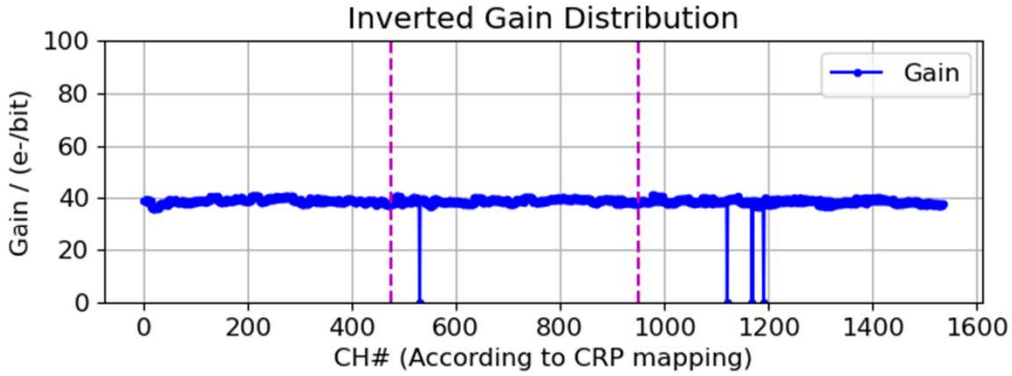
CRP5A Cold Test Result (BNL)

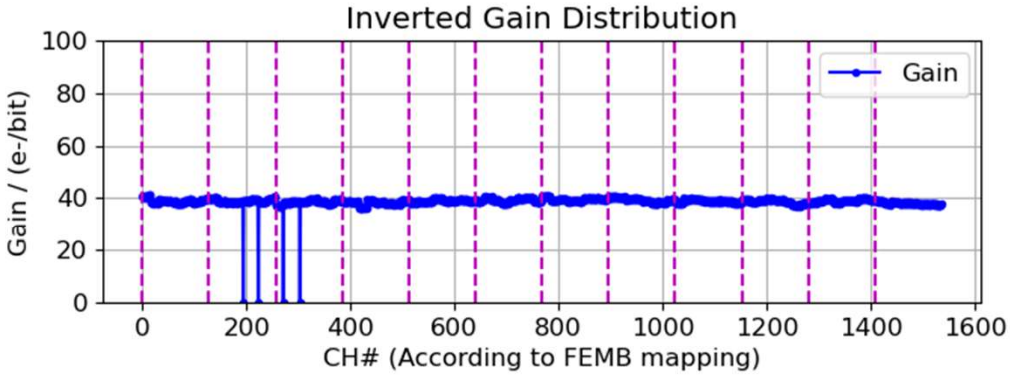
Preliminary Result

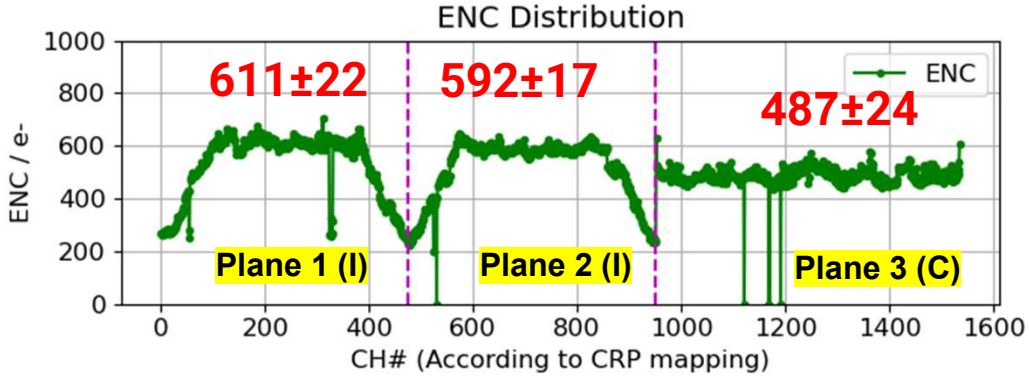
HV BIAS on, 900mV baseline, 14mV/fC gain, 1.0us peak time

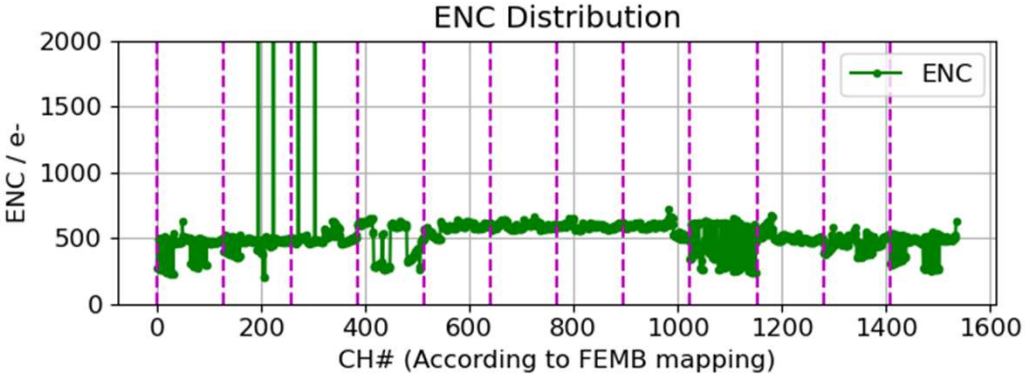










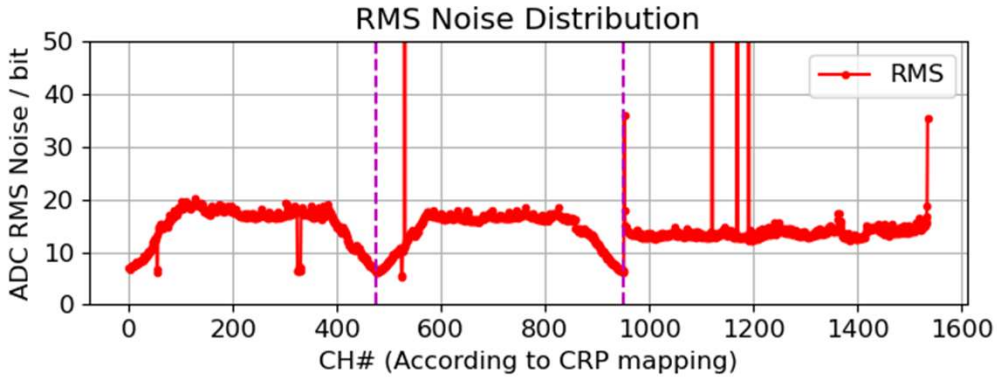


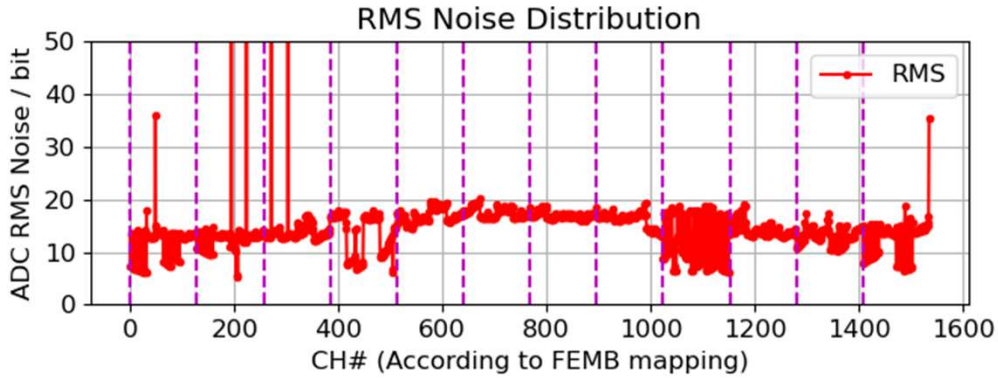
note: observed extremely large noise and abnormal gain on ch#194, 223, 271, 303. Set them gain to 0.

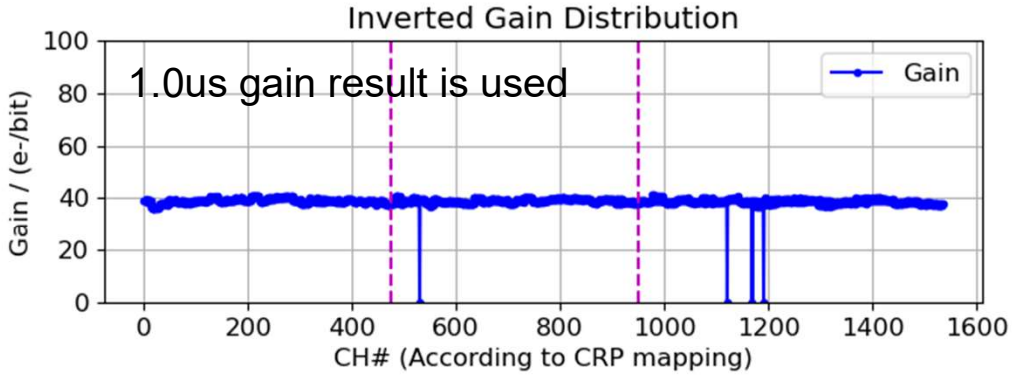
CRP5A Cold Test Result (BNL)

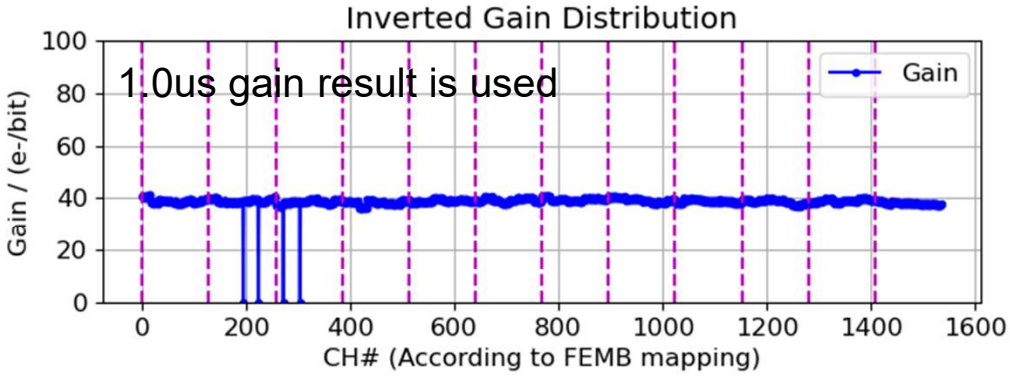
Preliminary Result

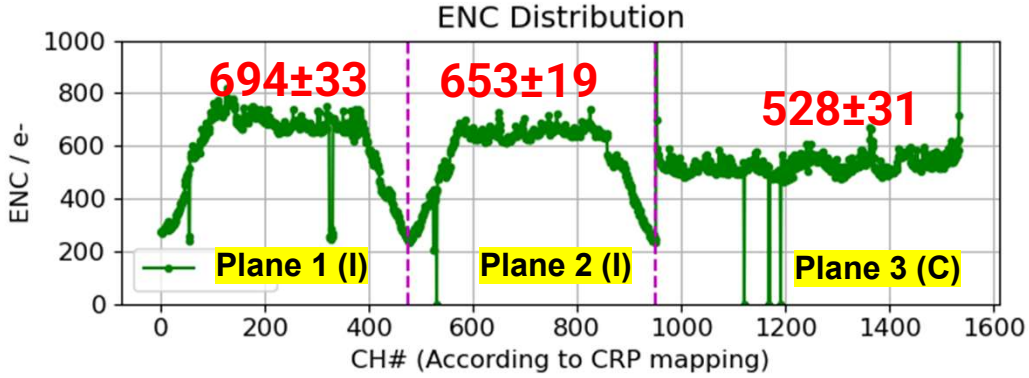
HV BIAS on, 900mV baseline, 14mV/fC gain, 0.5us peak time

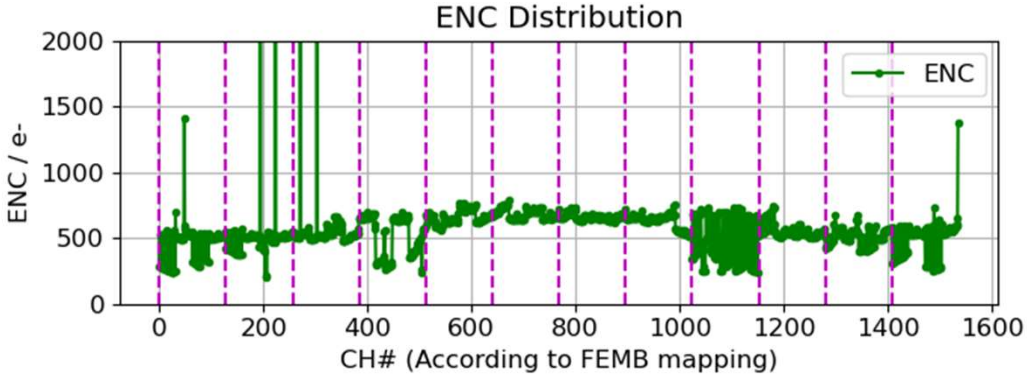








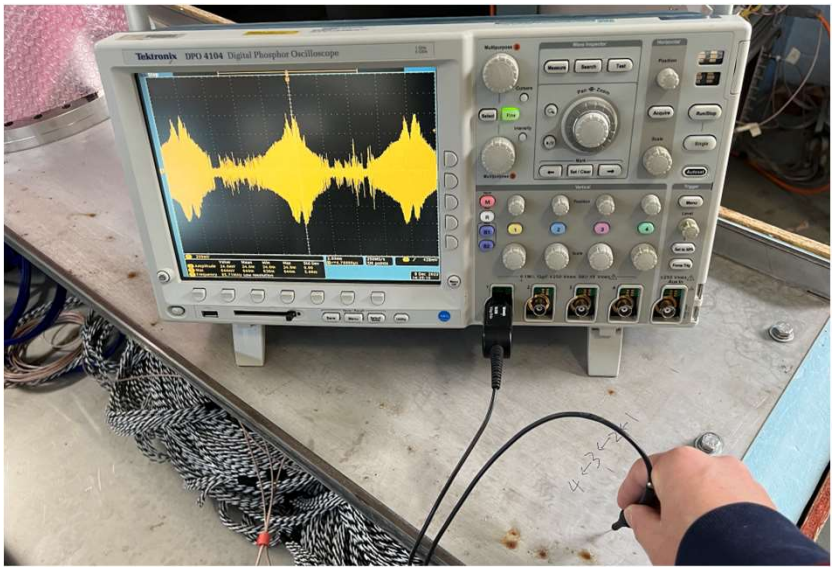




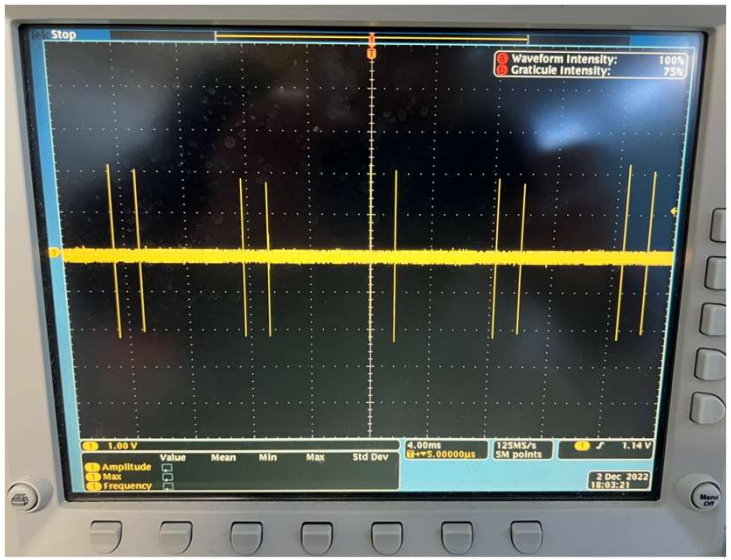
note: observed extremely large noise and abnormal gain on ch#194, 223, 271, 303. Set them gain to 0.

External Noise Sources

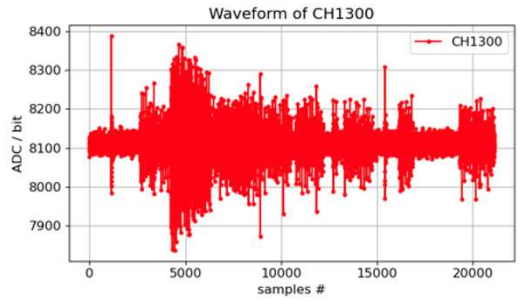
- Two external environmental noise sources were identified
  - Ceiling introduced significant noise to the building ground
  - 120Hz noise spike could be from the air handler at roof

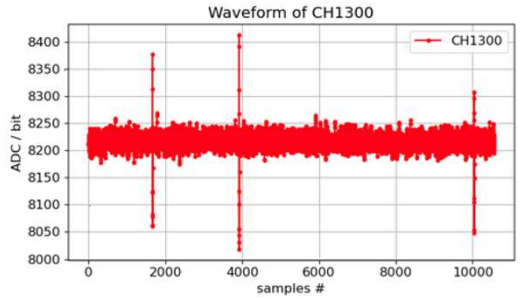


~60Hz, when ceiling lights are on



~120Hz noise spikes, unknown source





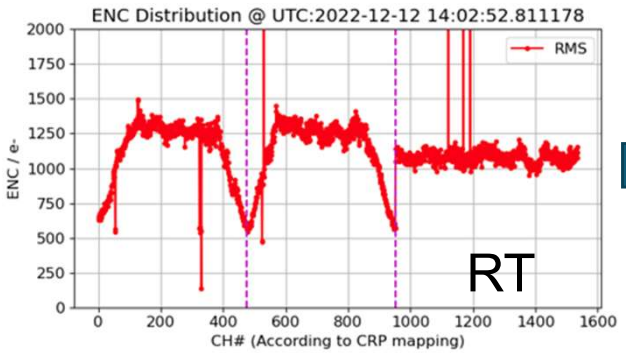
note: data is not continuous. spy buffer data (~2000 samples per trigger) are stitched together

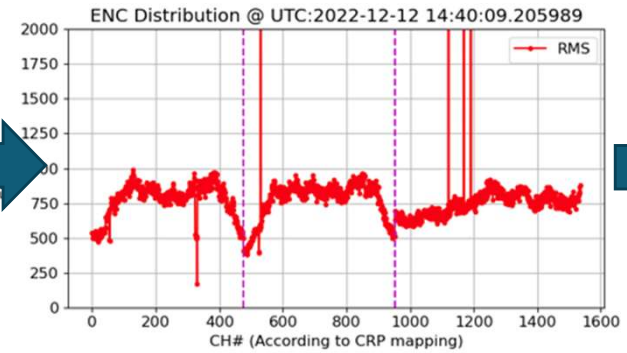
Positive Observations

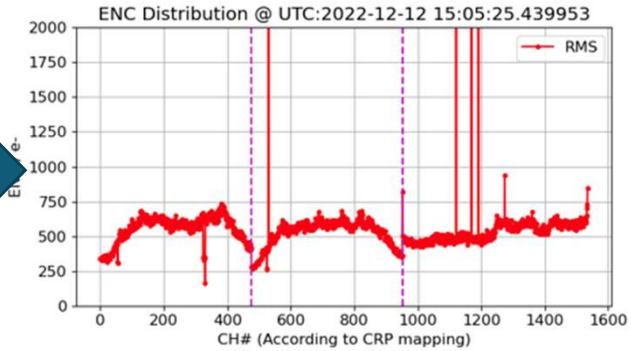
- No significant noise difference with HV BIAS ON/OFF
- Verified CERN “Noisy” WIB (4-6) on CRP5A
  - No significant abnormal noise increase is observed
- Verified many different power schemes
  - No significant difference in noise performance when V(FE) > 2.8V, V(CD) > 2.8V, V(ADC) > 3.0V with single-end interface between FE and ADC
    - Inconsistent with the APA testing at CERN
- Observed 25kHz noise bump/spike
  - However, its noise contribution is minor and negligible
- Verified both version of PTC (Linear vs. Vicor)
  - No significant noise difference is observed
  - Noise spikes from DC-DC switching frequency is observed with 0.5us peak time
- 2nd cold run shows that the floating copper layer doesn’t affect CRP5A noise performance
  - disconnect the copper braids between adapter boards and copper layer
  - separate HV filter box from the copper layer

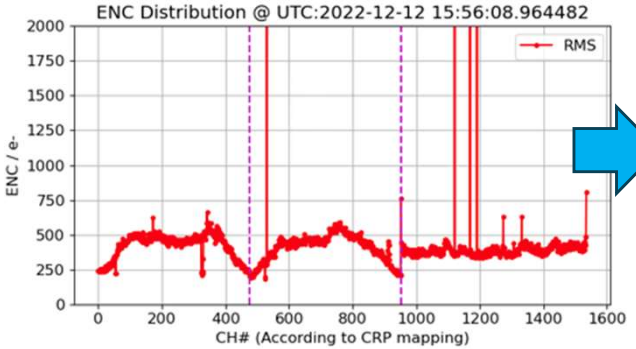
Note: Above observations are preliminary, further data analysis could reveal more details

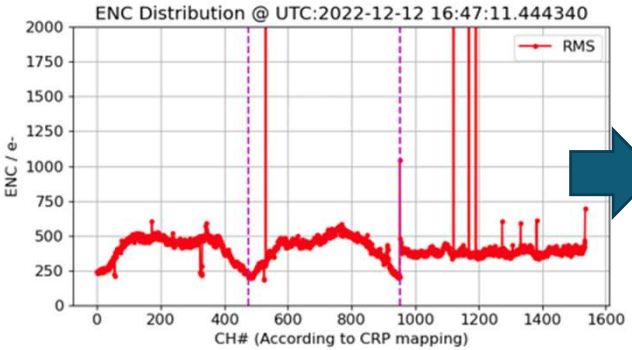
2nd Cold Run cool-down



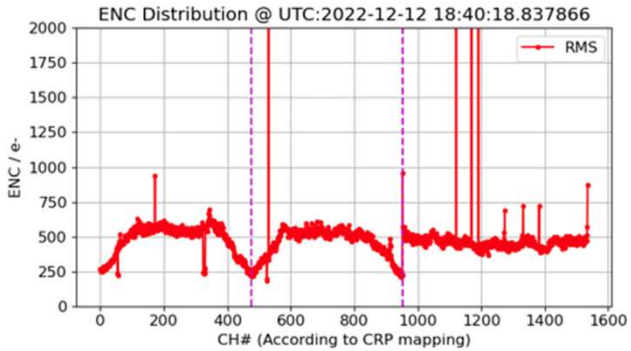




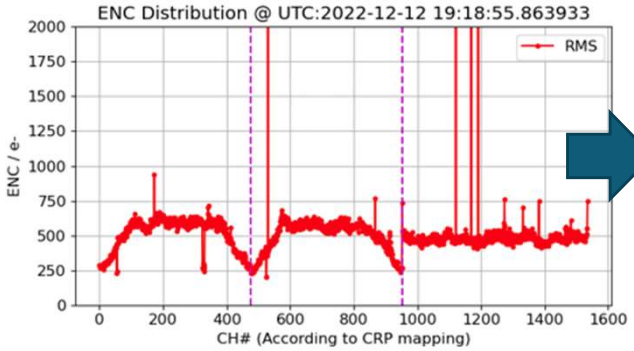


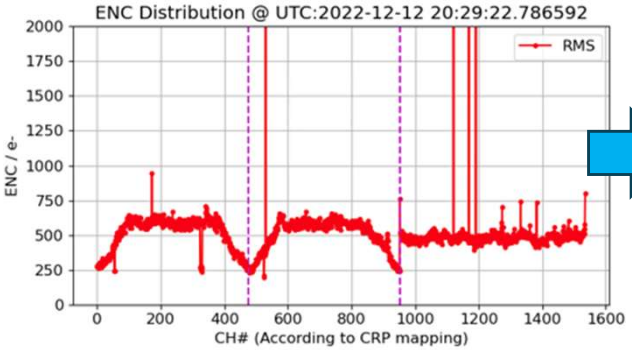


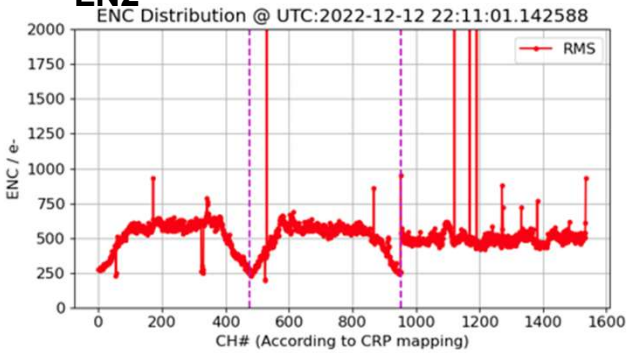
reach lowest temperature but CRP planes above LN2 level



CRP planes start to submerge in LN2







CRP planes and CE box fully submerged in LN2

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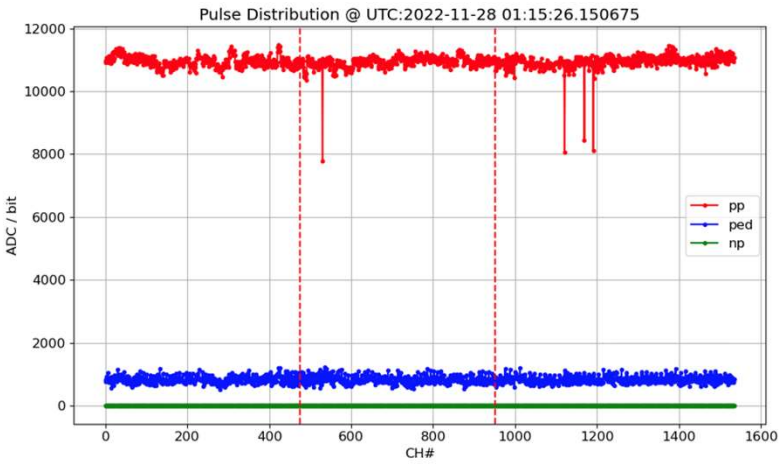
Observation during 1st cold run to be followed up

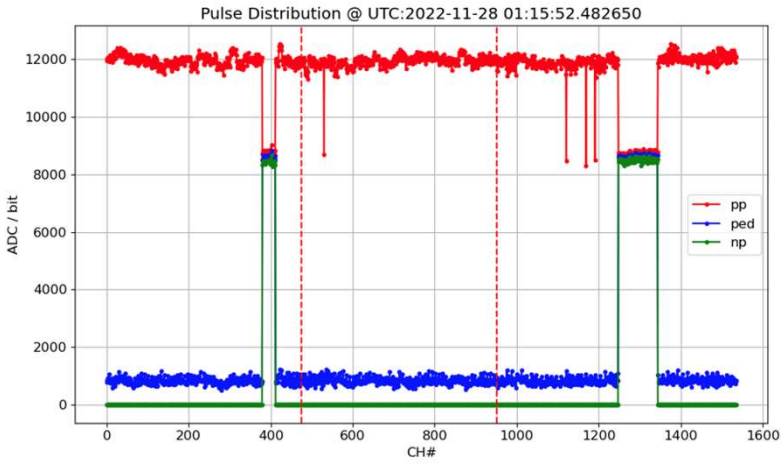
- One FEMB observed intermittent 62.5MHz clock connection
  - Lost clock during cool-down, restored after poking the mini-SAS cable near CE box
  - The issue either from FEMB data connector (poor soldering) or defective mini-SAS cable, will be investigated after 2nd cold run
- 4 channels with large noise (likely short to each other or ground)
- Several low noise channels (likely open)
- A dead FE channel observed after warm-up
  - The channel is on CE box near HV filter box
  - it is likely a discharge damage
    - Abnormal higher baseline, no pulse response
    - Input leakage current is ~1.5uA no matter the LArASIC leakage current setting
    - Back to alive at cold during 2nd cold run
      - At cold, the LArASIC has higher tolerance towards the discharge damage

Some issues related to WIB/Timing Card

- Rare fast command loss issue
  - First observed with FASTACT_LARASIC_CAL_COMMAND
    - Toggle the Start or Ending of LARASIC Calibrate signals
      - Always send one FC command to start pulser and one FC command to end pulser
  - Reproduced with fast command for LArASIC SPI configuration
    - If FASTACT_LARASIC_PROG_COMMAND doesn't configurate LArASIC properly, the FASTACT status register#2 (0x24) is not 0xFF
    - Will contact Alex to reproduce this rare fast command loss with his benchtop test setup
  - Jack's comment: Sending idle pattern continuously will ensure a DC balanced signaling and avoid unexpected DC level drift
    - This issue is not observed with Jack's FW yet



send calibrate fast command twice



Some issues related to WIB/Timing Card

- WIBs receive 62.5 MHz clock from the Bristol timing system
  - However, it can't recognize the fast command from the timing card
    - It only succeed once when I first time setup the timing card with FW supporting DCSK
  - Will seek help from both Bristol people and Alex

Next Step

- A comprehensive data analysis is in progress
- Plan for 3rd Cold RUN
  - Lift up CRP5A
  - Inspect the high (short) and low (open) noise channels
  - Inspect the cable connection
    - One FEMB suffers intermittent communication issue
  - Replace one FEMB with a damaged channel
  - Flip over CRP5A and re-cabling
  - Start the 3rd cold operation in the week of Dec 19
- Package and ship the CRP5A in the week of Dec 26