ColdADC Calibration Study

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Introduction 1

- ColdADC ASIC is the second stage of raw data processing on FEMB after LArASIC and before COLDATA
- 16-channel, 14-bit multi-stage pipeline ADC
- Two internal ADCs each processing 8 channels



Introduction 2

- Each ADC stage has 'W0' and 'W2' boundary voltage levels that determine ADC steps
- Boundary voltage levels set by internal calibration registers
- Register values are 16-bit unsigned integers
- Value indicates voltage level as fraction of maximum ADC voltage
 - 0x0 = 0 V, 0xFFFF = [max voltage]
- With incorrect calibration, ADC exhibits suboptimal linearity
- Correct calibration changes with temperature, other factors





ADSC Output	0	1	2	
Nominal Stage Output	$W0 = -2^{14-N}$	0	W2 = 2 ^{14-N}	
VDASC = DASC Output	-V _R /2	0	V _R /2	
Voltage Output (V _o)	$2(V_{in} - VDASC)$ $= 2(V_{in} + V_R/2)$	$2(V_{in} - VDASC) = 2V_{in}$	$2(V_{in} - VDASC) = 2(V_{in} - V_R/2)$	

Source: ColdADC_P2 Datasheet

Introduction 3

Default calibration constant values:

Stage	0	1	2	3	4	5	6
W0	0xC000	0xE000	0xF000	0xF800	0xFC00	0xFE00	0xFF00
W2	0x4000	0x2000	0x1000	0x0800	0x0400	0x0200	0x0100

- Because each ADC stage reads a smaller voltage range, variation in calibration constants is less in later stages.
- Calibration constants can be set manually, or ColdADC can auto-calibrate constants in hardware
 - Auto-calibration activated by writing to a register
 - Complete calibration occurs in a fraction of a second
 - Auto-calibration can be run for one sub-ADC at a time, or for both at once
- Auto-calibration is only applied to the first 6 stages
 - Even if it were not, past stage 6, in practice, constants would never differ from defaults

Calibration Constant Comparisons

- Data from ProtoDUNE II APA 2 and APA 4 runs in August 2022
- Here presenting data compared from three pairs of runs
 - Time Difference
 - Single vs. Both pipeline calibration
 - Voltage Settings difference (reference)
- All plots normalized
- Plots of difference (between two runs) of auto-calibrated constant

Time Comparison Data

- Time Comparison data shows magnitude of natural drift in "correct" calibration with time
- Data from one full APA (APA2)
- 5 WIBs = 20 FEMBs = 160 ColdADCs
- Warm condition (~300 K)
- Comparison of constants for the same chips from two runs
- Run 1: 8/24
- Run 2: 8/26

"Single" vs. "Both" Calibration Data

- "Single" vs. "Both": comparison of constants for two runs:
- "Single": one ADC pipeline calibrated at a time
- "Both": both ADC pipelines calibrated at once (normal calibration)
- Data from only one WIB
- 1 WIB = 4 FEMBs = 32 ColdADCs
- Both warm (~300 K) and cold nitrogen gas (~160-190 K)

Voltage Settings Data

- "Voltage Settings" data: only DC/DC input voltage settings differ (4.0 V vs. 3.0 V)
- Voltage setting should have no effect on calibration, so this dataset is used as a reference for random variation in autocalibration
- Two calibration runs, 4 minutes apart
- Data from one full APA (APA4)
- 5 WIBs = 20 FEMBs = 160 ColdADCs
- Cold nitrogen gas condition (~160 190 K)

Plots



Plots 2



Conclusions

- Reference "Voltage Difference" distribution tighter (as expected)
 - Runs were only 4 minutes apart
- "Time Difference" and "Single vs. Both" distributions similar, not much wider than reference
- Calibration constant drift over two days is only slightly greater than random variation over 4 minutes
- No significant difference between calibrating both sub-ADCs together and calibrating one at a time