Cold and warm electronics

F. Terranova on behalf of the PDS Consortium

Final Design Review, Mar 14, 2023

Overview

SiPMs and SiPM boards: not in the scope of this review. Production Readiness Review passed on Dec 2022.

Cold electronics:

- **System:** design completed in 2021
- **Validation:** validation completed in 2022
- **Procurement:** no special issues (see below)
- **QA/QC:** See Gustavo's talk

Warm electronics:

- **System:** design completed in 2022
- **Validation:** analog completed in dec 2022, digital to be re-tested for v3 in 2023 (see below)
- **Procurement:** no special issues (see below)
- **QA/QC:** See Gustavo's talk

Grounding and cables: see full documentation in EDMS

Recap of the SiPM and SiPM boards

In 2019-2021, DUNE carried out an R&D in collaboration with two vendors (Fondazione Bruno Kessler – FBK – and Hamamatsu Photonics - HPK) to develop **custom cryogenic SiPMs**

- Prototype downselection completed in 2021: NUV-HD-Cryo Triple Trench from FBK and S16517 from HPK are within specs and will be installed in FD1-HD
- Full test and production chain validated in 2022 for ProtoDUNE-HD. 40 modules (about 50%-50% per vendor)
- Mass test facility ("CACTUS") commissioned and tested during the construction of ProtoDUNE-HD
- Production Readiness Review passed on Dec 2022
- Tender and contract signature in progress
- Mass production (300,000 SiPMs in 6-SiPM boards) starts in 2023

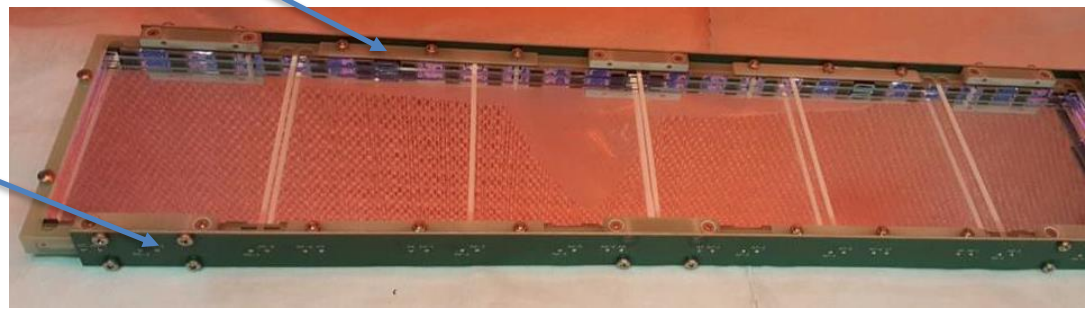
A spin-off of relevance for this review: the SiPM specifications included the overall performance in ganging mode (48 SiPMs in parallel) and, therefore, we needed to **bring (at least) the cold electronics at PRR level, too!**

Cold electronics

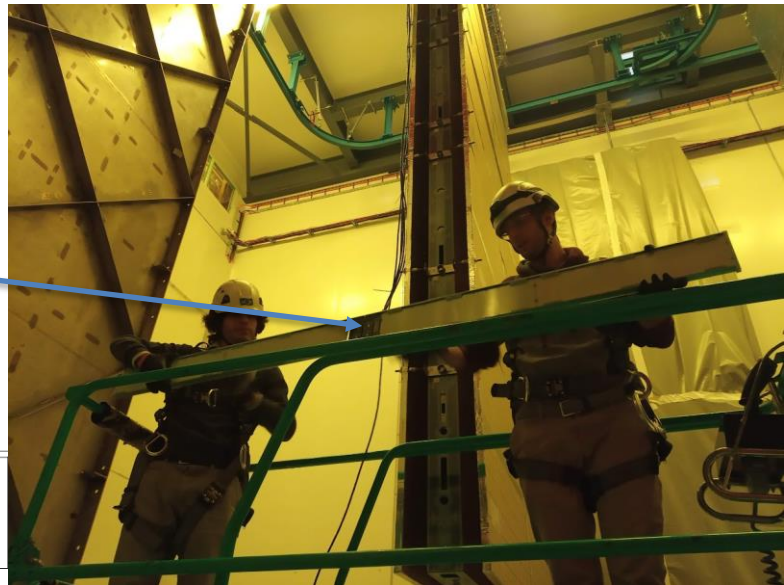
The system is made of four components:

The SiPM boards (8 per supercell/channel, 32 per module)

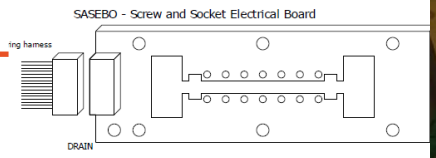
The signal routing boards



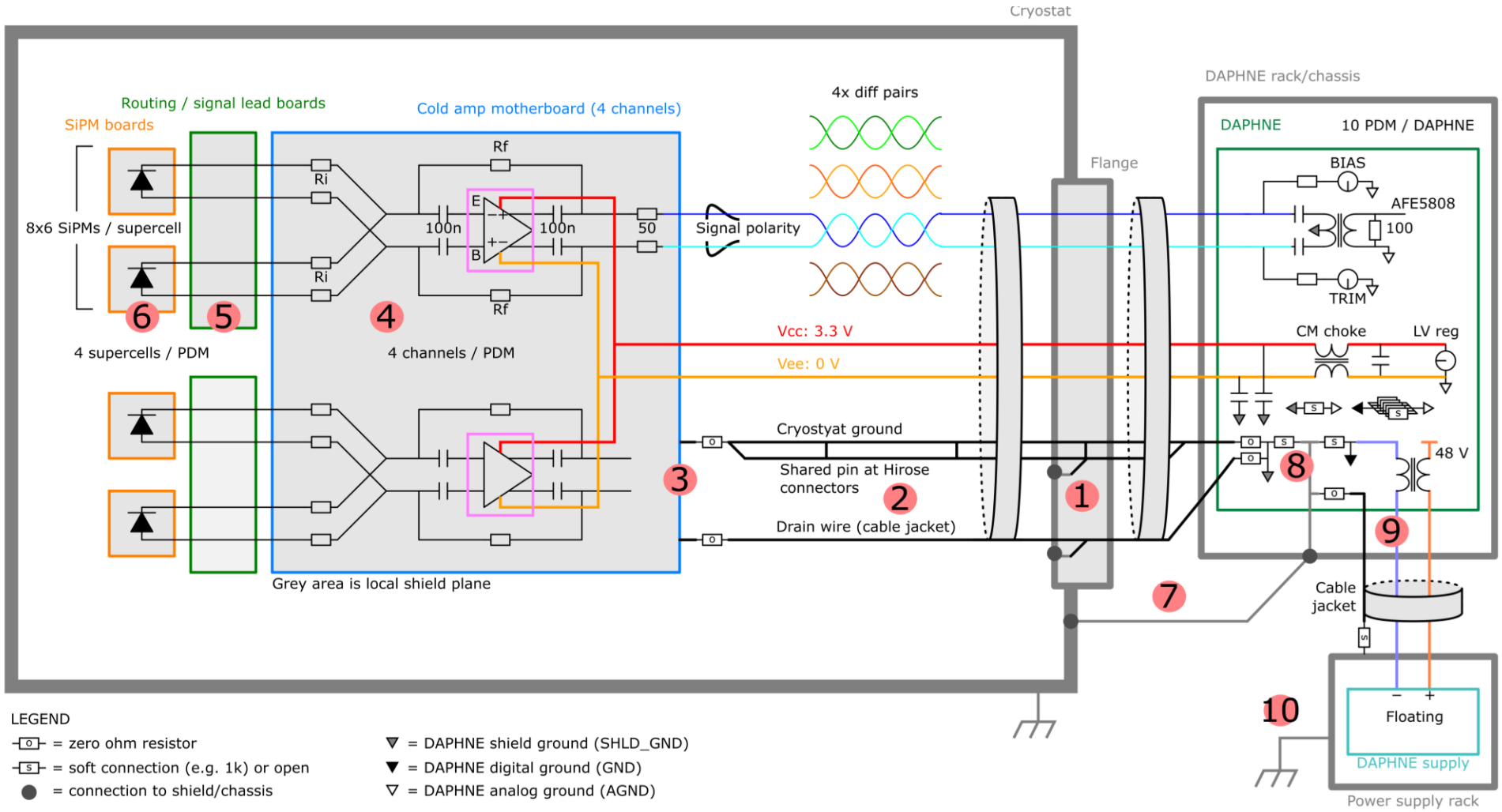
The motherboard hosting the cold amplifiers
(one amp per supercell/channel, 4 per module)



The PDS module-to-APA connector (SASEBO)



Cold-Warm electronics and grounding



Full grounding plan documentation: https://edms.cern.ch/document/2383681/4
(sytem is in a star-ground configuration with the hub at the cryostat flange)
Cables: https://edms.cern.ch/document/2383682/4

Cold amplifier

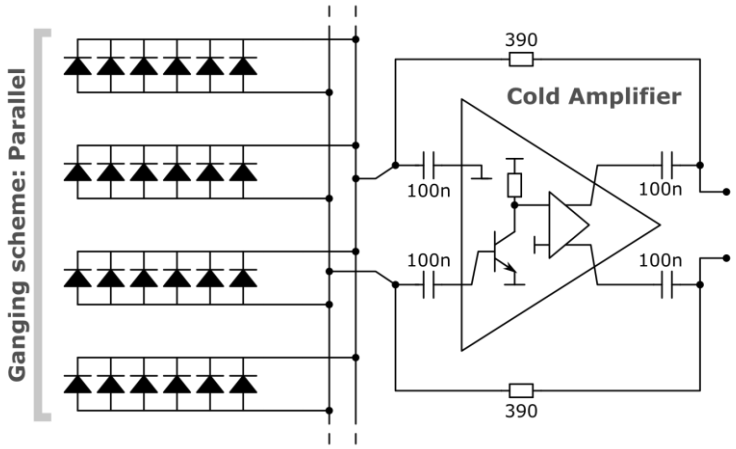
Design: based on commercial components qualified for operation at 77 K. Best performance achieved with a silicon-germanium input transistor and a BiCMOS fully differential operational amplifier -> **0.37 nV/√Hz**

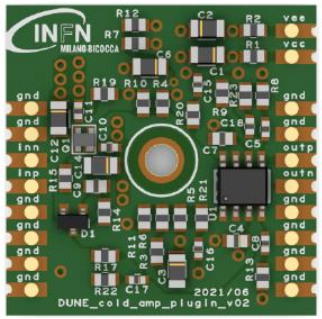
Validation:

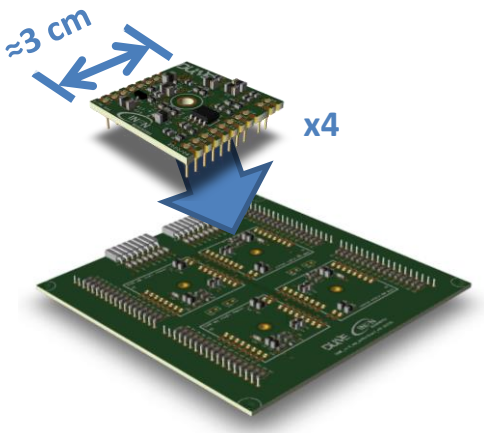
- Test bench with 8 SiPM boards
- Test of a whole supercell in LAr and LN
- Test at the cold box at 170 K
- Aging tests of the opamp (THS4531), the transistor and the whole amplifier

Requirements:

- **≈2000 p.e. dynamic range**
- **<100 ns signal rise time**
- **S/N>4**







Results and references

JINST
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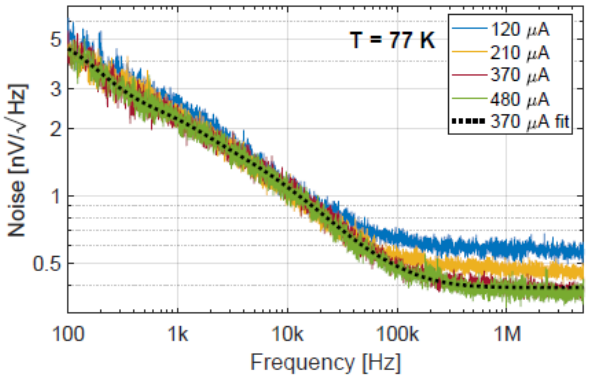
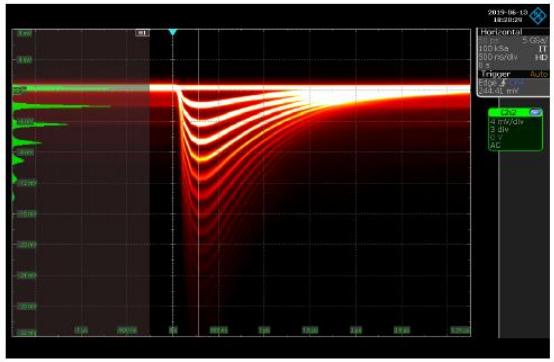
A low noise and low power cryogenic amplifier for single photoelectron sensitivity with large arrays of SiPMs





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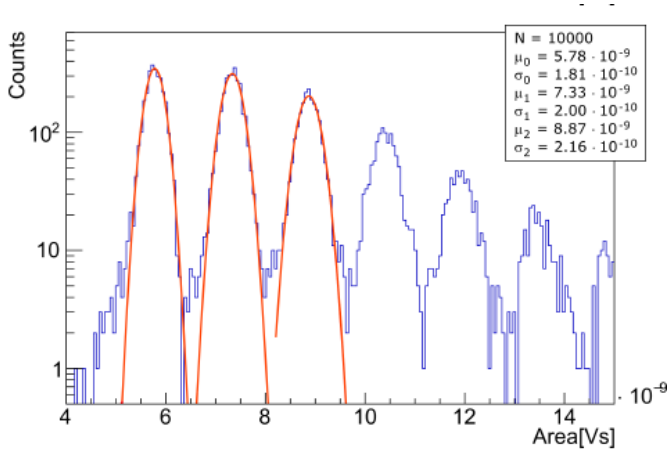
Cryogenic front-end amplifier design for large SiPM arrays in the DUNE FD1-HD photon detection system



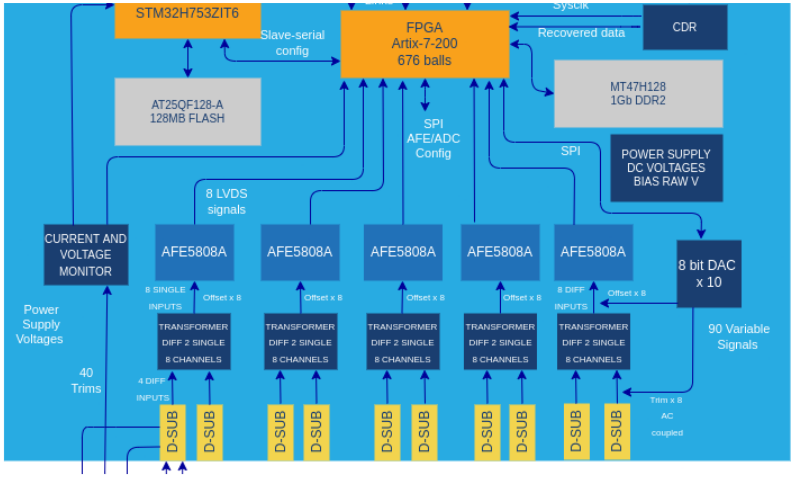
S/N = 8 at 45% PDE and 2000 p.e. dynamic range for both FBK and HPK SiPMs
Power consumption: 0.7 mA/channel at 3.3 V, i.e. 2.4 mW/channel

Warm electronics

The warm electronics of FD1-HD (and FD2-VD) is based on the DAPHNE board developed by FNAL, Colombia, Paraguay, Perù, and Milano Bicocca

Channels per board	40	1 board per APA
Resolution (bits)	14	
Sample rate	62.5 Msps	16 ns per “thick”
Bias to SiPM	30-70 V	Adjustable in real time. Cover FBK and HPK operation in warm and cold
Bias to cold electronics	3.3 V	
Data link	4.8 Gbps	(10 Gbit link in V3, see below)
Slow control	I, V	OPC-UA server
Firmware	FPGA+MC	Artix-7 FPGA, Migen/LitexCore/STM32H753 Microcontroller in V2 (system-on-module in V3, see below)

The DAPHNE analog front-end



Core device: Texas Instruments AFE5808A. The AFE5808A was designed for use in ultrasound machines. The combination of two amplifiers and a voltage-controlled attenuator allows a wide range of input voltages to be matched to the dynamic range of the analog-to-digital converter (ADC). The device can operate at sampling rates up to 80 MSPS (for DUNE the sampling rate will be 62.5 MSPS) and has a dynamic range of 14 bits. **The cost effectiveness of this device was one of the main driver for the development of DAPHNE**, and was inherited from Mu2e

Design completed in 2021 (v1). Some modification implemented during validation that brought to the **final design** implemented in V2 and V3.

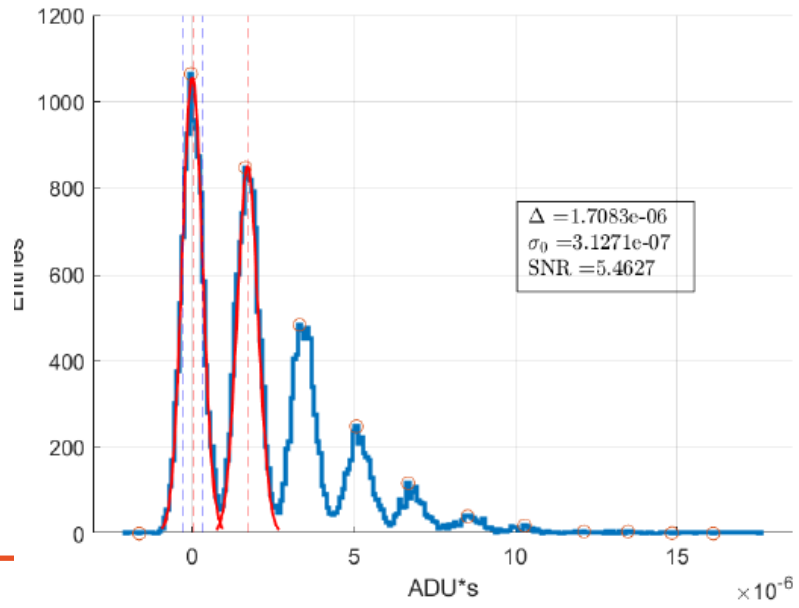
Validation

The analog front end, including signal filtering in the FPGA was validated in 2021-22 by:

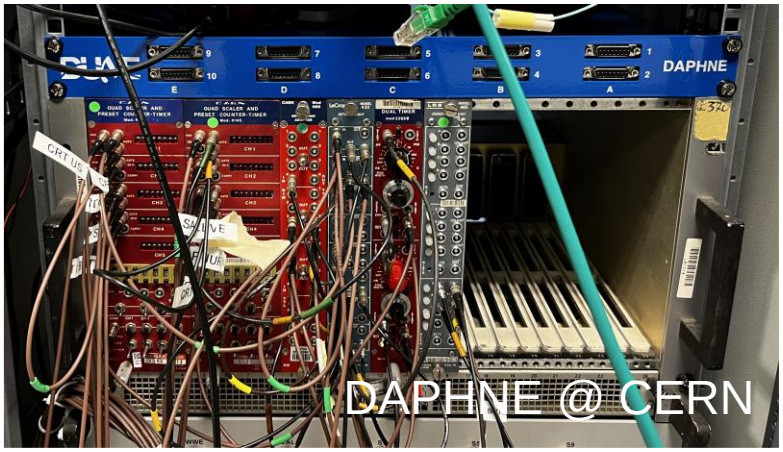
- A dedicated setup (test-bench) in Milano Bicocca using the cold electronics + 8 SiPM boards (electrically equivalent to a supercell)
- Using the PDS test facilities of Milano Bicocca with a real supercell
- During the cold box tests at ProtoDUNE-HD (170 K, 10 m cables) with a real module in the APA

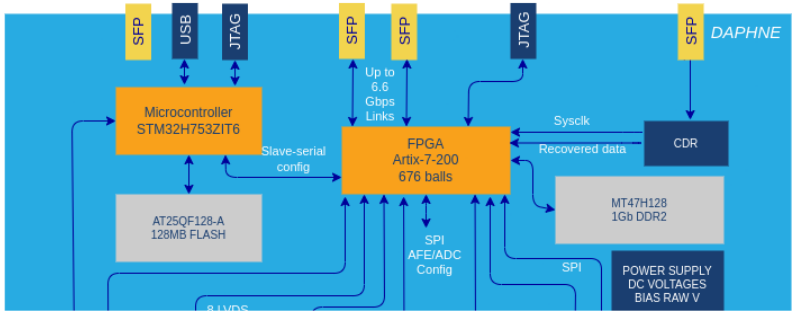
Results demonstrate S/N>5 at 45% PDE with 2000 p.e. dynamic range


DAPHNE @ MiB



The DAPHNE digital system



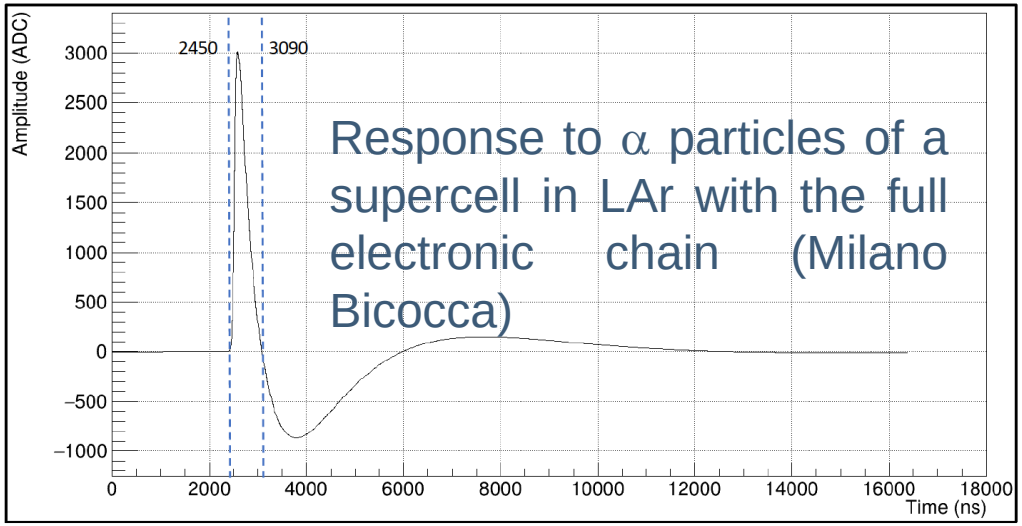


- The core device for the DAPHNE digital system is the Artix-7 + microcontroller + ethernet connection to FELIX, which is an intrinsic limitation at 4.8 Gbps. This configuration fulfills the specifications for DUNE (DAPHNE Version 2)
- In 2022, DUNE decided to drop the FELIX architecture to mitigate procurement risks, which opened up an opportunity to upgrade the DAPHNE digital system (DAPHNE Version 3) to:
  - Support a full system-on-module running a linux-based operating system
  - Remove the 4.8 Gbps limitation and exploit 10 Gb links
  - Implement more sophisticated trigger strategies
- The current firmware design and implementation does not need a major revision to run in a system-on-module but it will have to be re-tested as soon as version 3 is available (from May 2023 to Nov 2023)

Requirements

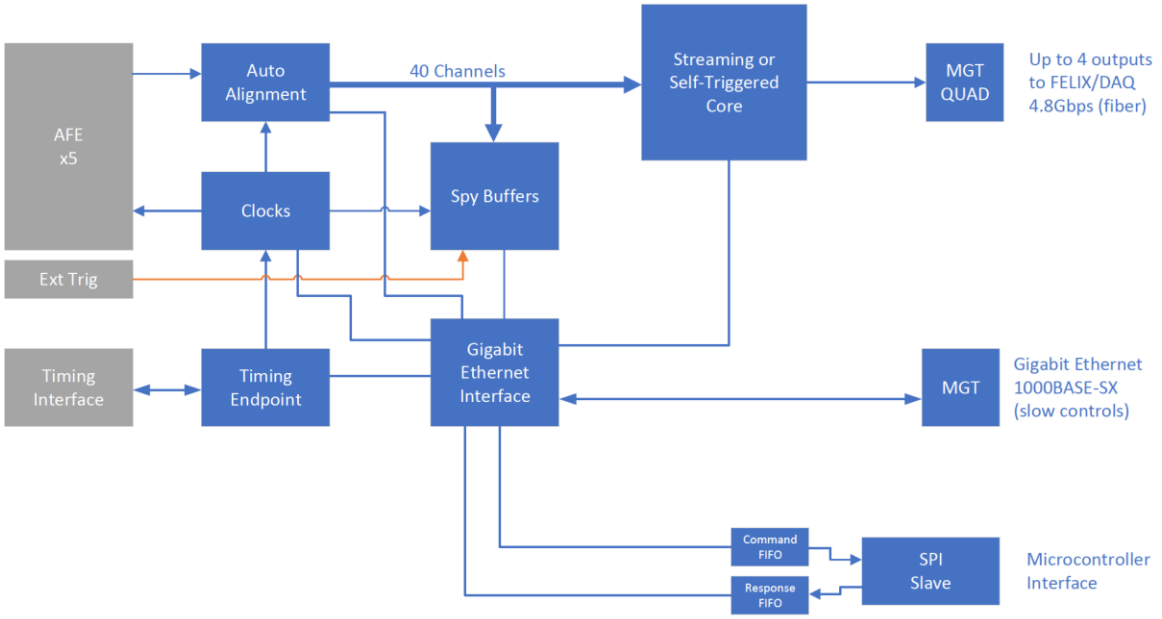
- Implement the trigger logic in DAPHNE. The PDS channels (“supercells”) are operated in **self-trigger mode** and a waveform is recorded and transmitted to FELIX if the signal exceed 1.5 p.e. Waveforms are (conservatively!) sampled for 16 μs (1024 thicks) for baseline restoration. The waveform size is thus 14336 bits
- Transfer the triggered waveform to FELIX/DAQ at a sustainable throughput. The trigger rate per channel (supercell) is <4 kHz and it is dominated by SiPM cross-talk (+ contributions from radiogenic and radioactivity in the supercell materials). The throughput at SURF (no cosmic rays) is then 4 kHz * 14336 bits *40 channels = **2.3 Gbps** in DUNE and about 2.9 Gbps in ProtoDUNE-HD before 8b10b encoding (3-3.5 Gbps after 8b10b encoding)

- Timestamp of each waveform with a precision of a few tens of ns (i.e. negligible w.r.t. the risetime of the signal
- (optional) Possibility to work in streaming mode for debugging purpose



DAPHNE V2 Firmware & Software

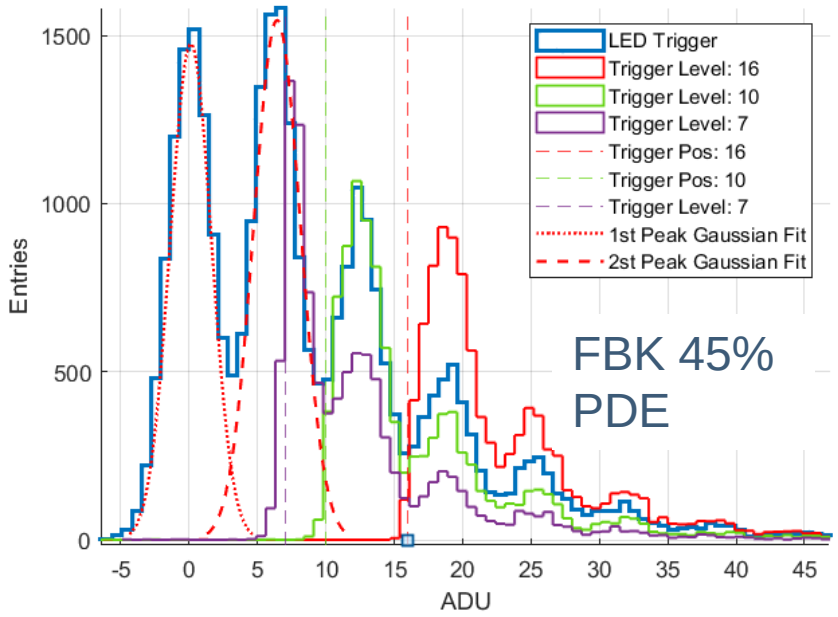
- Firmware acquires data from AFEs and sends selected data to DAQ (FELIX) on up to four 4.8 Gbps links.
  - Streaming data from 16 channels
  - Or self-triggered data from 40 channels (beta version)
- Firmware controlled through gigabit Ethernet (Python scripts or C/C++ programs)
- GigabitEthernet also provides I/O to microcontroller for control of analog sections of DAPHNE

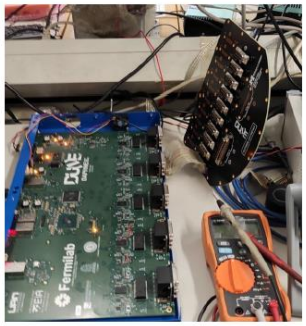


The microcontroller receives commands (text strings) through the Gigabit Ethernet interface. This replaces the microcontroller 100 Mbit Ethernet interface.

Validation of the digital system

- Self-trigger: validation of the firmware (version beta in DAPHNE v2) performed in Milano Bicocca and EIA-Colombia
- Hardware simulation reproduces the results observed at the test bench
- Data streaming to FELIX tested at FNAL and validated at CERN in 2022
- Original DUNE timing endpoint integrated into DAPHNE firmware & tested at CERN in October 2022.
- New (duty factor encoded) timing endpoint integrated into DAPHNE firmware & tested at Fermilab (with the ICEBERG DAQ) in March 2023.
- Tests with 30m cold cables confirm signal preservation (checked at the cold box tests of ProtoDUNE-HD, too)





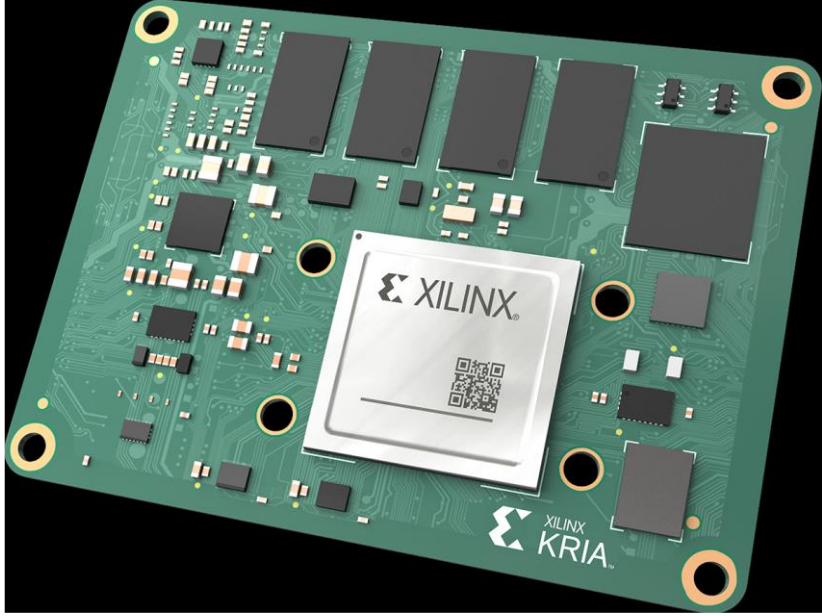
Toward version 3

Core device: Kria K26 System-on-Module (SoM) by Xilinx

Zynq UltraScale+ MPSoC (XCK26)

4GB 64-bit wide DDR4 memory

Integrated non-volatile memory devices



- DAQ integration with FELIX demonstrated only in streaming mode in late 2022. To be completed including the self-trigger module
- Delivery of the intermediate board (Kria dev Modules) to study DAQ integration with the system-on-module (April 2023)
- Repeat validation tests already done for v2 at CERN, FNAL, and Milano Bicocca

Transition to DAPHNE v3 expected to be completed by the end of 2023

Procurement

Procurement for electronic components is critical in these years and had some impact in other DUNE subsystems (e.g. FELIX). In our case, we do not expect any item to be on the critical path because the PDS construction is driven by the delivery time of the SiPM boards and the mounting of the modules. In particular:

Item	Quantity	
SiPM boards	48000	Produced together with SiPM (OK, not in the scope of this review)
Signal lead boards	12000	Design at PRR level. Not critical
Cold amplifier	6000	Suggestion: early procurement of the THS4531 OpAmp
Motherboards	1500	Design at PRR level. Not critical
DAPHNE analog	150 boards	Suggestion: early procurement of AFE5808A. Other components not critical
DAPHNE digital	150 boards	Kria K26 SoM

Conclusions

The design and validation of the cold and warm electronics for the PDS is mature either at PRR level (SiPM, SiPM boards – PRR passed on Dec 2022) or at FDR level (this review)

- The cold electronic design has been completed in 2021 and validation tests confirms suitability for FD1-HD
- We achieved a S/N>4 for 45% PDE at 2000 p.e. dynamic range in laboratory tests (“test bench”), with the full system connected to a real supercell (“supercell tests”) and in the cold box tests at CERN
- The design of DAPHNE is in spec because it retains those features with the sampling rate and depth (n. of bits) of the AFE5808A
- The full chain (DAPHNE, cable, Sasebo, supercell/module) was tested in laboratory tests at FNAL, NIU, EIA, Milano Bicocca, and CERN and confirm expectations
- The DAPHNE throughput is appropriate for DUNE and the key digital modules (self-trigger, data streaming, time synchronization, DAQ integration) are either final or close to completion
- We are exploiting the opportunities offered by the post-FELIX transition migrating the DAPHNE digital system to a System-on-Module and we aim at a PRR-level DAPHNE board by the end of this year.

Power density