

DUNE FD1 PDS final design review

Replies to Q6 (noise) and Q7 (aging)

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For the DUNE FD1 PD consortium

Q6. Questions on S/N with respect to noise environment

(i) How was noise characterized in the measurements of S/N in each case? How much random and how much correlated in each setup?

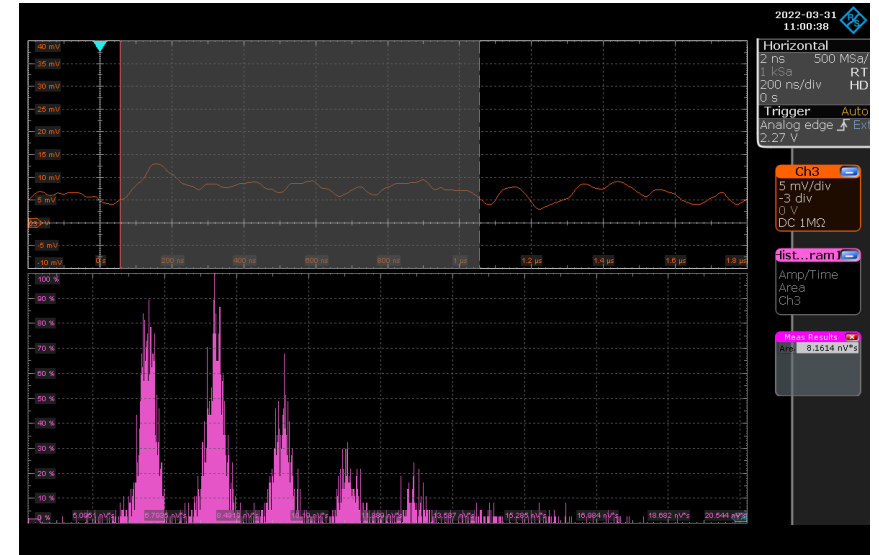
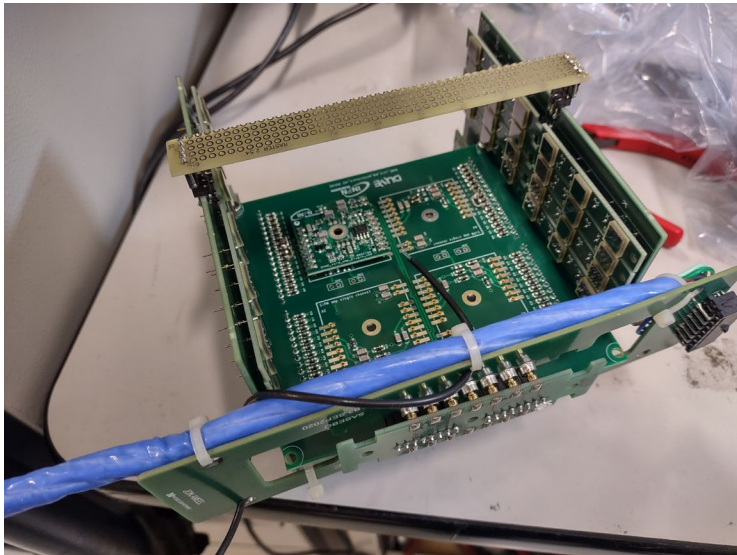
A. 48 SiPMs + cold amplifier in LN2, read out with oscilloscope

Results give $S/N \approx 8$ for both SiPM models at overvoltage corresponding to 45% PDE ([Slide 7](#) of F. Terranova's talk).

The S/N here is given by the series noise of the amplifier (0.37 nV/ $\sqrt{\text{Hz}}$) and thermal noise of the SiPM quenching resistor (48 SiPMs in parallel are equivalent to a source impedance of about 7 Ω , which at LN2 gives ≈ 0.2 nV/ $\sqrt{\text{Hz}}$).

The measured S/N matches what is calculated from these sources, as detailed in this paper, section 6, doi:10.1088/1748-0221/17/11/P11017.

This is intended as the upper limit that can be reached with this design of SiPMs and cold amplifier, at overvoltage corresponding to 45% PDE.



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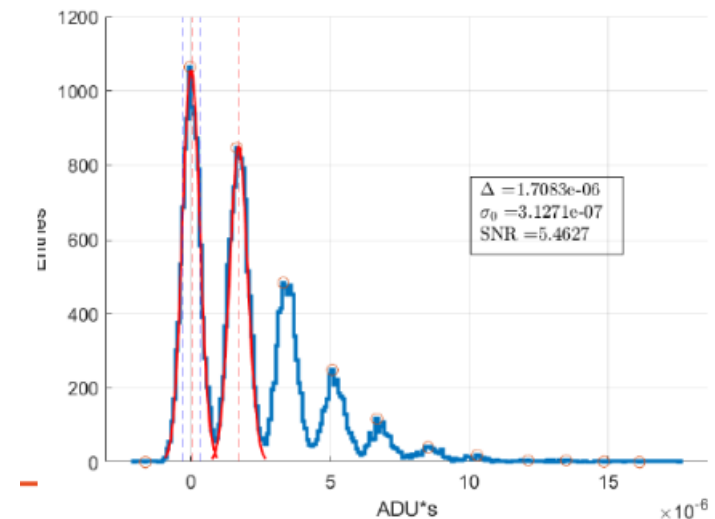
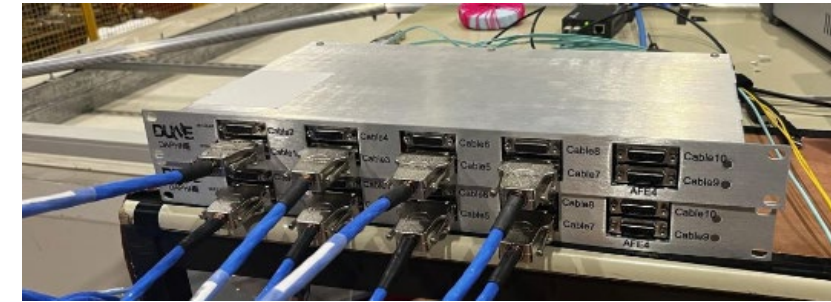
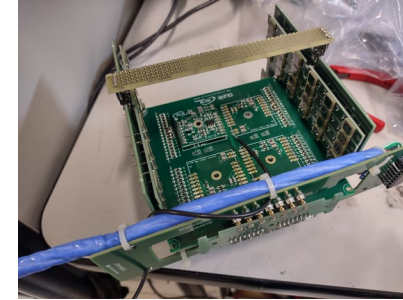
B. 48 SiPMs + cold amplifier in LN2, read out with DAPHNE

Results currently give $S/N \approx 5$ for both SiPM models at overvoltage corresponding to 45% PDE ([Slide 10](#) of F. Terranova's talk).

The S/N here is degraded compared to case "A". This can be due to:

- Quantization noise of the DAPHNE digitizer (amplitude of 1 p.e. corresponds to 8 ADU, so that 2000 p.e. fit in its 14 bits nominal dynamic range). A slight improvement is indeed observed if the internal gain of the AFE5808 chip is increased (this involves an obvious trade-off with dynamic range)
- $1/f$ noise in the AFE5808 front-end circuitry. This can be slightly reduced by enabling the AFE5808 baseline integrators (this involves a less-obvious trade-off with dynamic range, which reduces by a factor ≈ 2 with integrators on)
- EMI or environmental disturbances, since in these measurements the DAPHNE grounding was not yet in its final configuration.

Although the target $S/N > 4$ has already been reached, this is still under study.



Q6. Questions on S/N with respect to noise environment

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C. Supercell + cold amplifier in LAr, read out with oscilloscope or digitizer

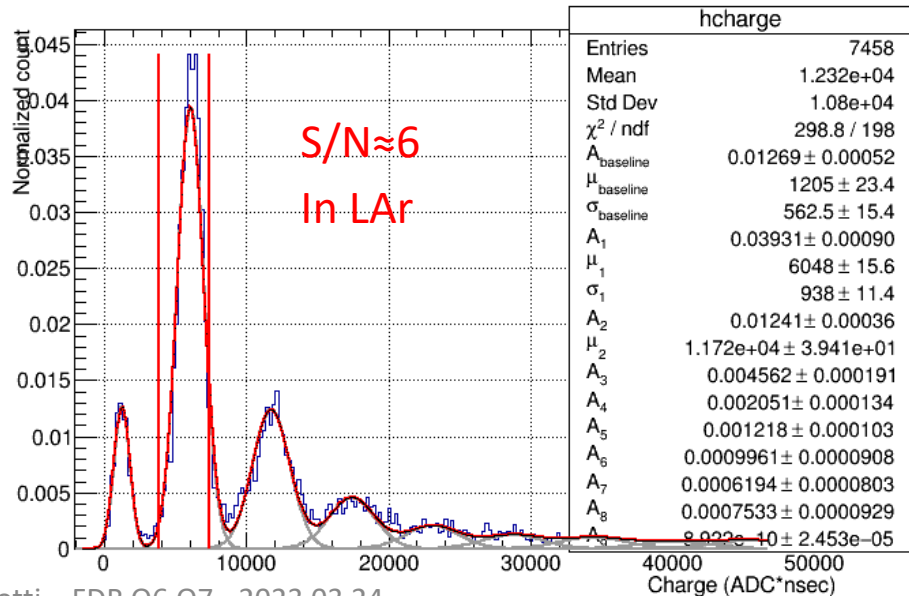
This was tested in different labs. Results give $S/N \approx 4-6$ depending on conditions.

The S/N here is degraded compared to case "A". This can be due to:

- Higher signal rate in LAr (39Ar, cosmics, ...)
- EMI or environmental disturbances

Still under study. Measurements with Supercell in LAr + DAPHNE are planned.

(They have been done, but the pulsed LED was not available at that time, so the S/N cannot be easily estimated from that dataset.)



FBK + Eljen

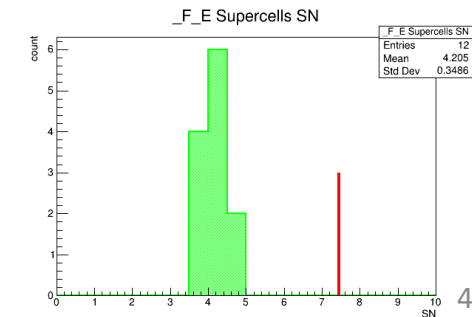
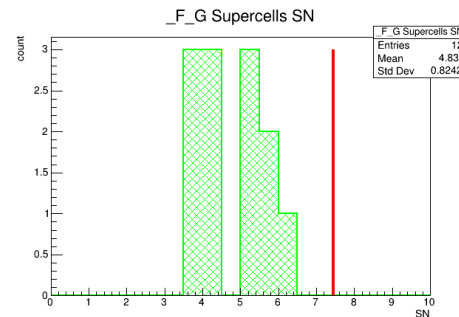
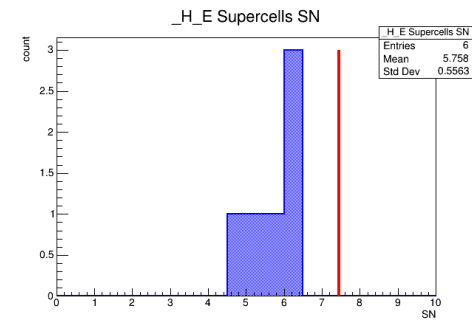
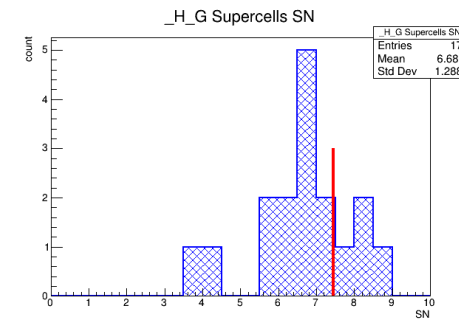
OV	SN0	Ajuste	STD 0	DSN0
4.5	3.46	0.03	0.05	0.06
6.5	4.92	0.03	0.14	0.14
7	5.42	0.03	0.08	0.08

HPK + Eljen

OV	SN0	Ajuste	STD 0	DSN0
3	3.54	0.07	0.41	0.42
4	4.58	0.05	0.26	0.26
5	5.25	0.05	0.33	0.33

HPK + G2P

OV	SN0	Ajuste	STD 0	DSN0
3	4.40	0.02	0.07	0.07
4	5.50	0.02	0.05	0.06
5	6.55	0.02	0.03	0.04



Q6. Questions on S/N with respect to noise environment

(ii) How does the noise environment of ProtoDUNE I compare with lab tests? Is it different in an active environment (e.g. large event) than in the lab?

The configuration in ProtoDUNE I was significantly different from the present design. SiPMs were a different model, in a different ganging configuration (8/channel), with no cold electronics, read out at warm with the DAPHNE precursor named SSP (similar in some respects, but different in others). Due to all these differences, measurements of S/N obtained in ProtoDUNE **cannot be easily compared** with the present system.

We don't have specific information on the possible impact of large events. Saturation in one PDS channel is not expected to affect the others. No interaction was so far observed between charge and light readout in the cold box during ProtoDUNE 2 installation.

When reading out a large volume of LAr, we expect a **higher rate of single photons due to ^{39}Ar** and other sources compared to what can be seen in the lab. A high rate of single p.e. will cause baseline fluctuations which could degrade the S/N even if the acquisition trigger is set above the single p.e. level.

With the present system **we estimate that the S/N will be preserved up until at least a photon rate of 100 kHz** per channel. This is above the current estimate of single p.e. rate coming from simulations. Dedicated tests of S/N at increasing background photon rates are planned to better understand the limits of the system.

All this assumes that the S/N is calculated with a simple integration (or moving average or digital low pass filter) on the acquired signals. Additional robustness of the S/N against high rate of single p.e. could be gained by employing more sophisticated filtering and analysis algorithms.

Q6. Questions on S/N with respect to noise environment

(iii) Any issue in cross-talk with CALCI or other systems sharing the cable tray?

The CALCI cables carry DC signals (a constant 1 mA current feeding the sensors continuously). Voltage reading is multiplexed but does not involve voltage fluctuations in the cable. The risk of CALCI cables injecting disturbances onto signal cables in the same trays is therefore minimized.

All CALCI cables are shielded, and the grounding scheme follows the guidelines and recommendations. Each cable has an individual shield up to the flange. The RTD (sensor) side of the shield is floating.

From the PDS side, each signal cable carries 4 channels (one PDS module). Each of the four pairs is individually shielded from the others. **Between shielded signal pairs in the same cable, we measured a crosstalk level below 0.05% (or 1/2000) for signals with 50 ns edges on a 30 m length.** The possibility of injecting crosstalk from a neighboring cable should then be much below 0.05%, even if the neighboring cables carry signals with fast edges.

No specific measurements have been done yet in the system deployed for ProtoDUNE II.

Q7. Aging tests on cold electronics

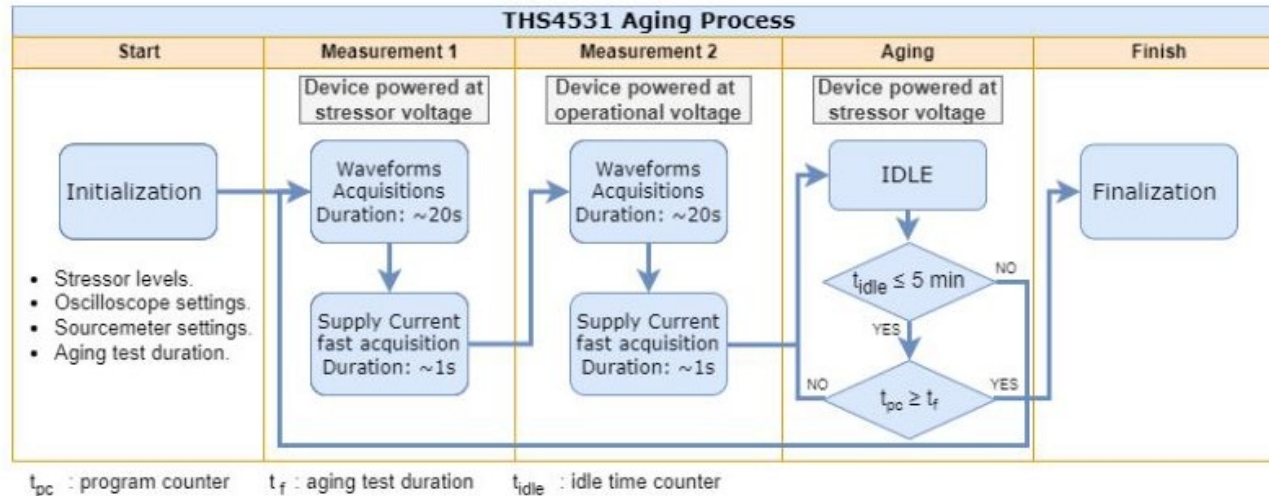
(i) Provide detailed procedure for aging tests, including op amp in addition to transistor and how power supplies were operated during the tests.

The measurement and results are described in the QA/QC document EDMS 2847126, chapter 2. The opamp is covered in section 2.1.4.

https://edms.cern.ch/file/2847126/1/FD1_PDS_Preliminary_QAQC_Plan.pdf

The document is being updated since the review, to include more details on the procedure.

It now includes the diagram below, illustrating the procedure, and a paragraph discussing (absence of) self-heating effects.



Aging is estimated based on a 1% variation of the current measured at the stressor voltage.

No degradation is observed when the power supply is lowered to the operational voltage.

The current measured at the operational voltage is constant, except for periodic variations on a timescale of hours, which are due to fluctuations in the temperature of the room. The current measurement at operational voltage is used to cancel these fluctuations from the current measured at the stressor voltage.

Measurements of the power supply current can be affected by thermally related behaviors as the device power consumption increases at high stressors voltage values. These behaviors can be mainly attributed to self-heating effects caused by carrier mobility reduction in the individual transistors of which the device is built, among other parameters that depend on the channel temperature. The average power consumption at the selected stressors values of 6.5 V and 6.0 V are 11.2 mW and 10.2 mW, respectively. Considering the device data sheet parameter ϕ_{JB} (Junction-to-board characterization parameter) of 73 C/W, the average junction temperature is 0.82 C above the PCB board temperature, which is the main heat dissipation path of the device. Given that the measurement of the current is performed after 5 minutes of aging giving enough time to the device to achieve thermal equilibrium, and the small temperature difference between the device junction (transistors channels) and the ambient, the impact of thermal effects are not

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Assuming exponential dependence of lifetime on $1/V_s$, extrapolation to the operating supply voltage of 3.3 V results in a lifetime estimate of 10^{17} .

This is still a conservative estimate, because aged devices only show the 1% current variations when still at the stressor voltages, and the variation is no longer present when the supply is lowered to the operating voltage.

