DUNE timing system (DTS) update

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DUNE UK meeting

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University of BRISTOL

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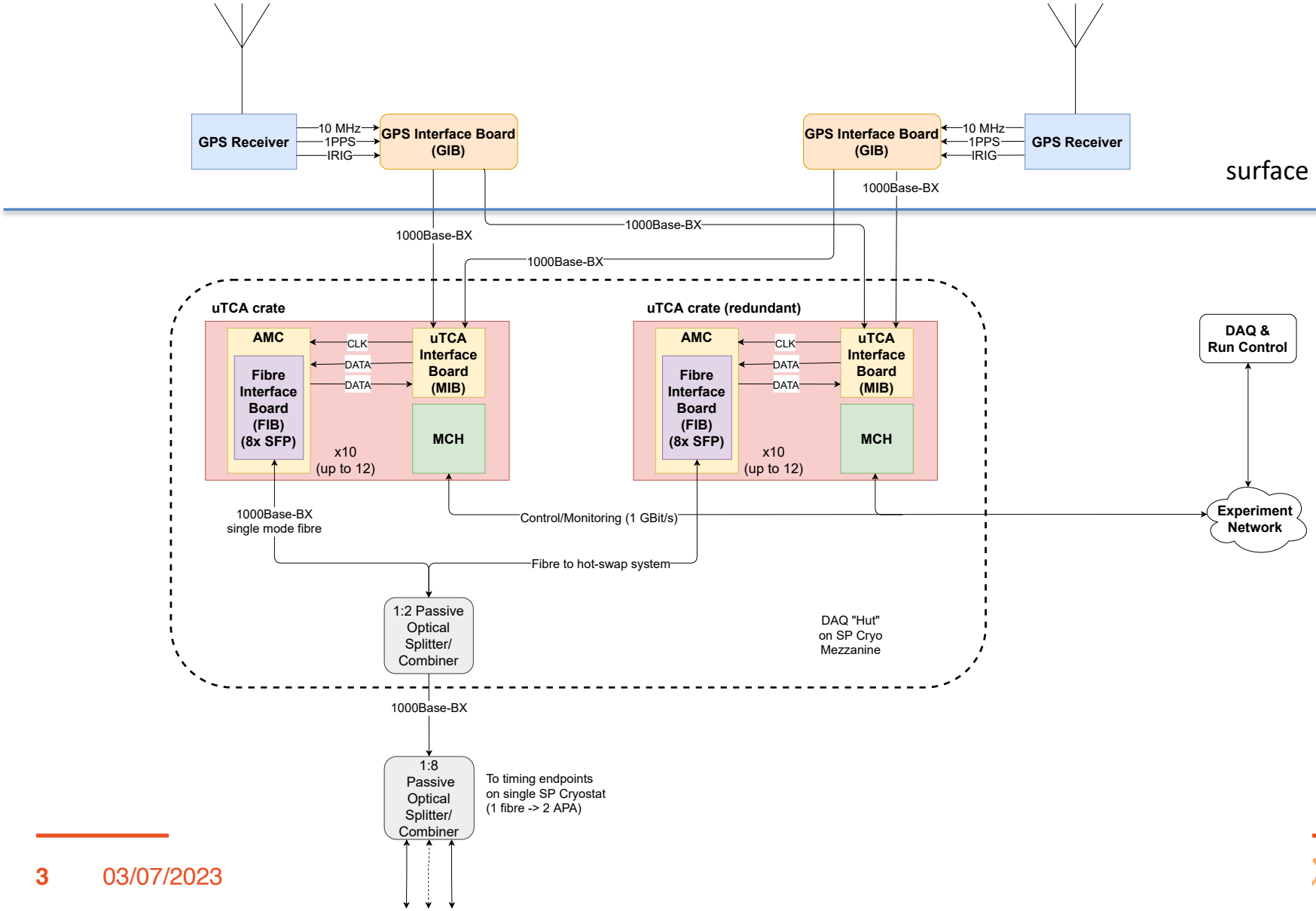
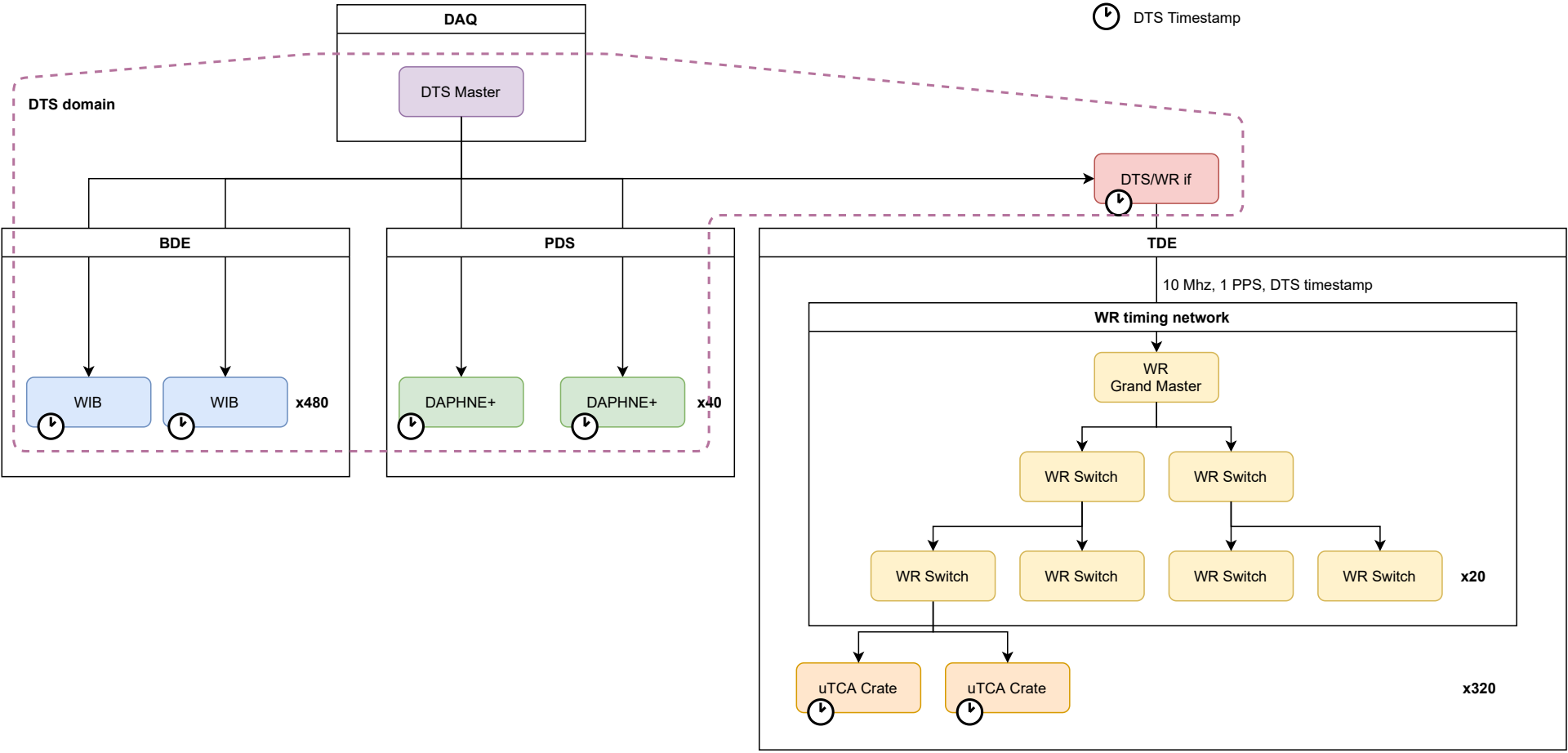
- Status overview
- Hardware status
- Firmware status
- Software status
- DTS-WR integration update
- Regression/release testing update
- Rest of 2023

Timing system – HD module



Timing system – VD module



Timing system custom hardware reminder

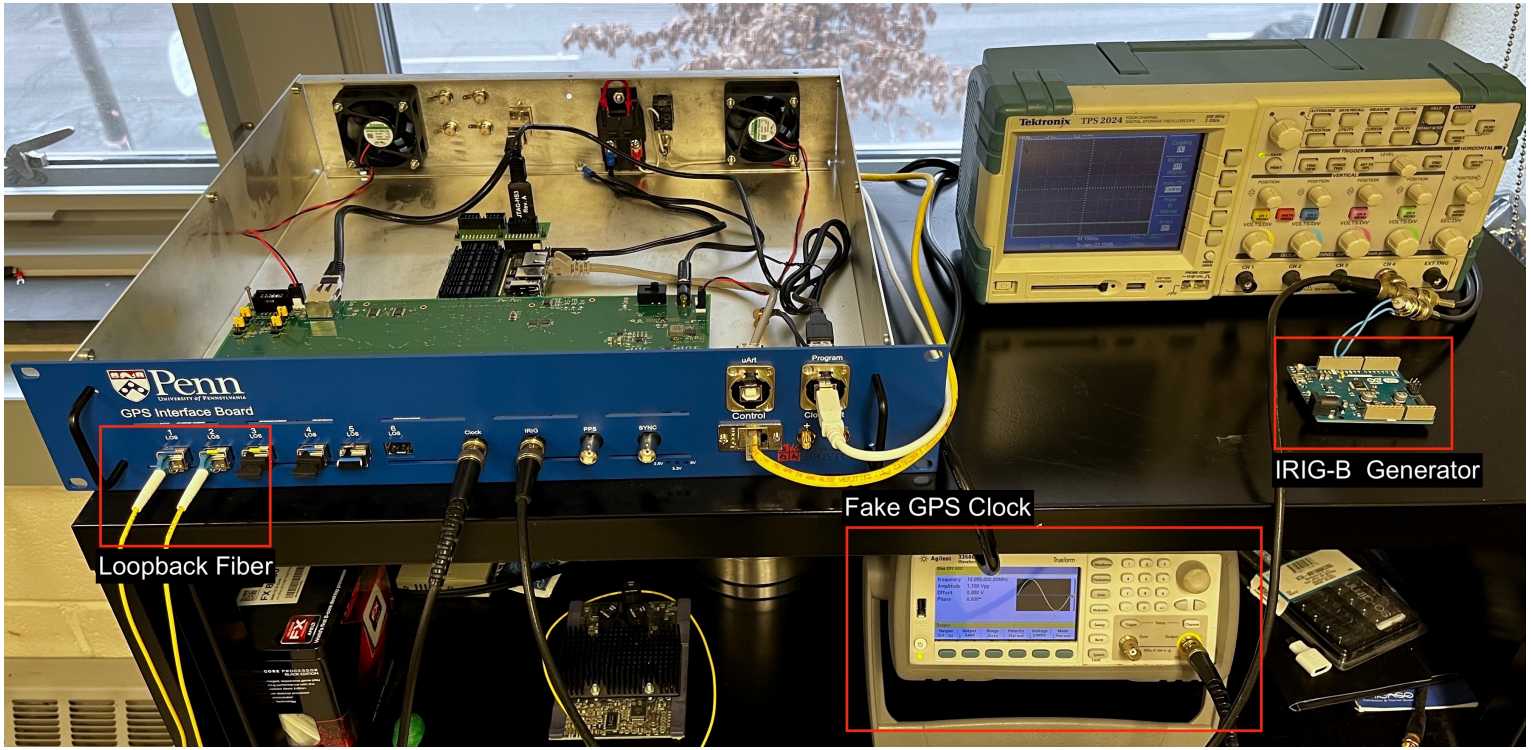
- **GPS interface board (GIB):**
  - Receives clock and time from GPS receiver
  - Generates DUNE timing system timestamp
  - Transmit to MIB using the DTS protocol
- **uTCA interface board (MIB):**
  - Receives data-stream from GIB
  - Fan out clock and data to FIBs (via the AMCs)
- **Fibre Interface Board (FIB):**
  - An FMC with 8 SFP modules
  - Hosted by an AMC in a uTCA crate
  - Fans out timing data-stream to timing endpoints

Status overview

- **Transition to new DTS data-encoding for detector RO complete**
  - All electronics at test-stands use new DTS endpoint firmware block (synchronised with PD-I hardware)
  - New scheme allows clock recovery to happen inside FPGA
- **Working towards full chain at CERN by Q4 2023**
  - Requires co-ordinated hardware, firmware, and software efforts
  - Assembled hardware prototypes for each custom board in hand
  - COTS hardware in hand
  - Firmware development underway
  - All of above needs software support and integration
- **DTS-WR integration tests with TDE experts performed at CERN last week**
  - Re-affirmed that WR master be locked to electrical signals provided by DTS endpoint (using DTS reference hardware)

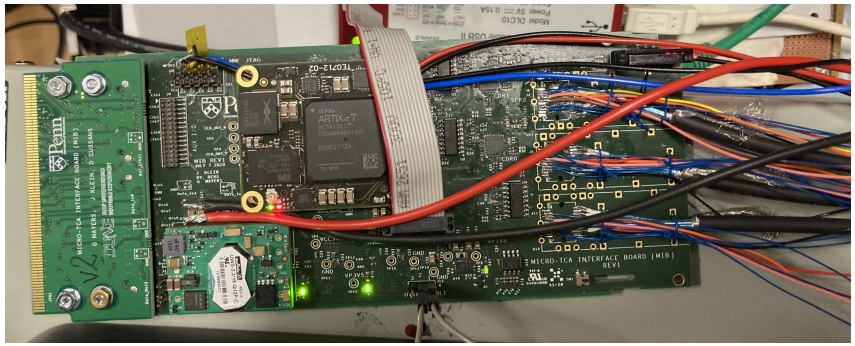
GIB status

- **Board prototypes fabricated, assembled, and commissioned at Penn**
- **Prototype firmware (based on previous data-encoding designs) tested in hardware**
  - Migration to current serries of DTS firmware on-going

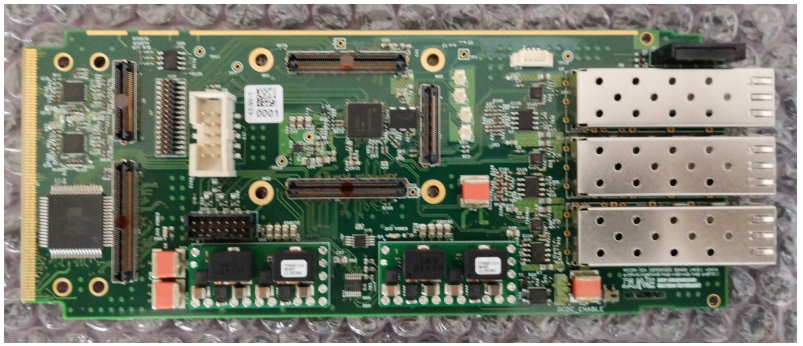


MIB status

- **First hardware prototype had a number of issues**
  - Significant fixes would have been required to allow board operation for PD-II
- **Second prototype of hardware has now arrived in Bristol**
  - Initial hardware tests done: no major issues discovered so far
  - Firmware design using new-series DTS firmware under development
  - uTCA module management firmware needs testing
    - Proceeds in parallel with more general DTS functionality testing

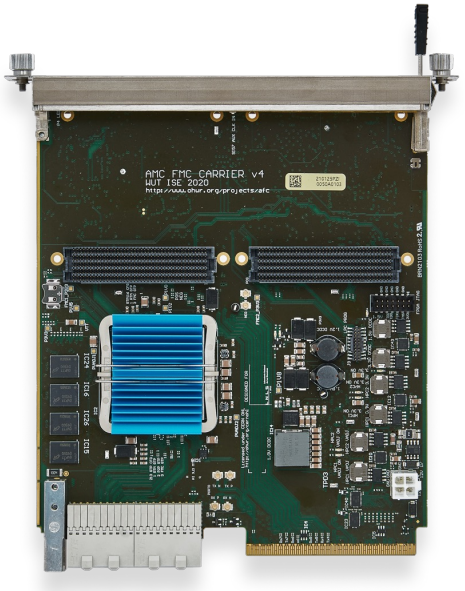


MIB v1

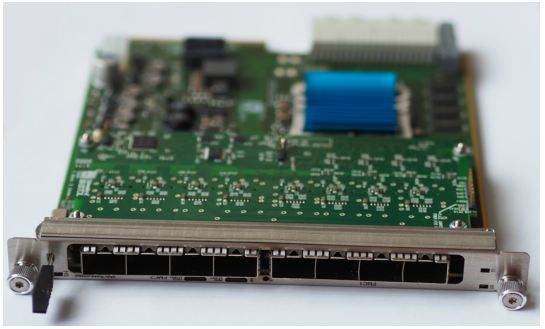


MIB v2

FIB+AFC status



- **First FIB prototypes tested with AFC v3**
  - No major issues with FIB hardware discovered
  - Downstream clock+data path of MIB -> uTCA backplane -> FIB+AFC v3 verified
    - However AFC v3 is obsolete
- **AFC v4 available in Bristol**
  - Significant changes to clocking scheme → needs testing
  - Firmware under development to allow testing with FIB v1
- **FIB v2 hardware design under way**
    - New version removes now unnecessary CDR chip
    - Lower priority

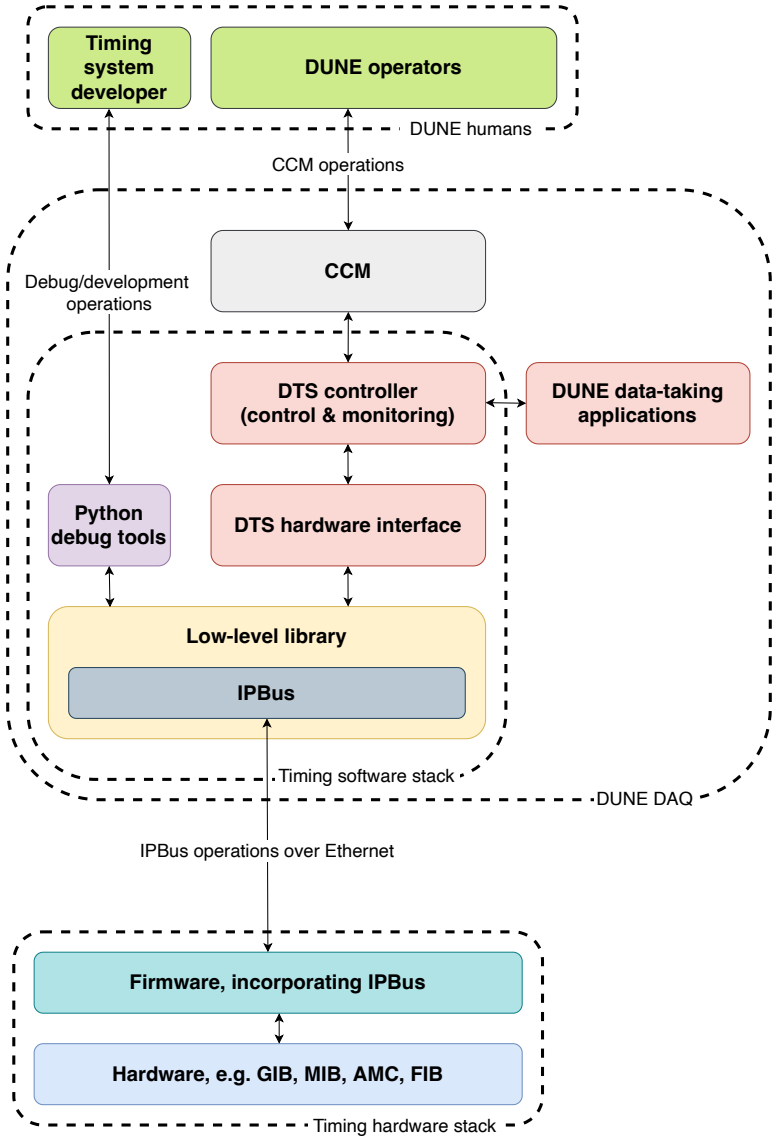


Firmware status

- **Reminder: new series DTS firmware changed the data-encoding over the fibre**
  - External CDR chip no longer need → done in DTS firmware
- **GIB firmware being migrated to new-series DTS firmware**
  - Being done by DUNE group at Penn
- **Designs for new hardware MIB v2 and FIB+AFC v4 are under development**
  - Not as simple as translating old firmware designs to new data-encoding scheme and new hardware pin locations
  - Brand new functionality being developed, e.g.: GIB redundancy support
  - MIB effort: firmware developers at Montreal
  - FIB+AFC v4 effort: firmware developers at Bristol
- **New timing protocol firmware mostly debugged**
  - Outstanding issue with fine (2 ns) endpoint round trip time measurement, and endpoint delay adjustment
    - Under investigation

Software design reminder

- **Low-level C++ library provides software access to DTS firmware+hardware**
- **Python bindings to low-level C++ classes and methods provide a debug/development interface**
- **For each timing device, there is a dedicated high-level timing controller module**
  - It accepts higher level commands from CCM and translates them into the relevant lower-level library calls
- **The DTS controller modules send the lower-level commands to the hardware interface module**
- **The hardware interface makes the appropriate calls to the hardware via IPBus**
  - It also collects operational monitoring information, which is sent back to the controllers



Software status

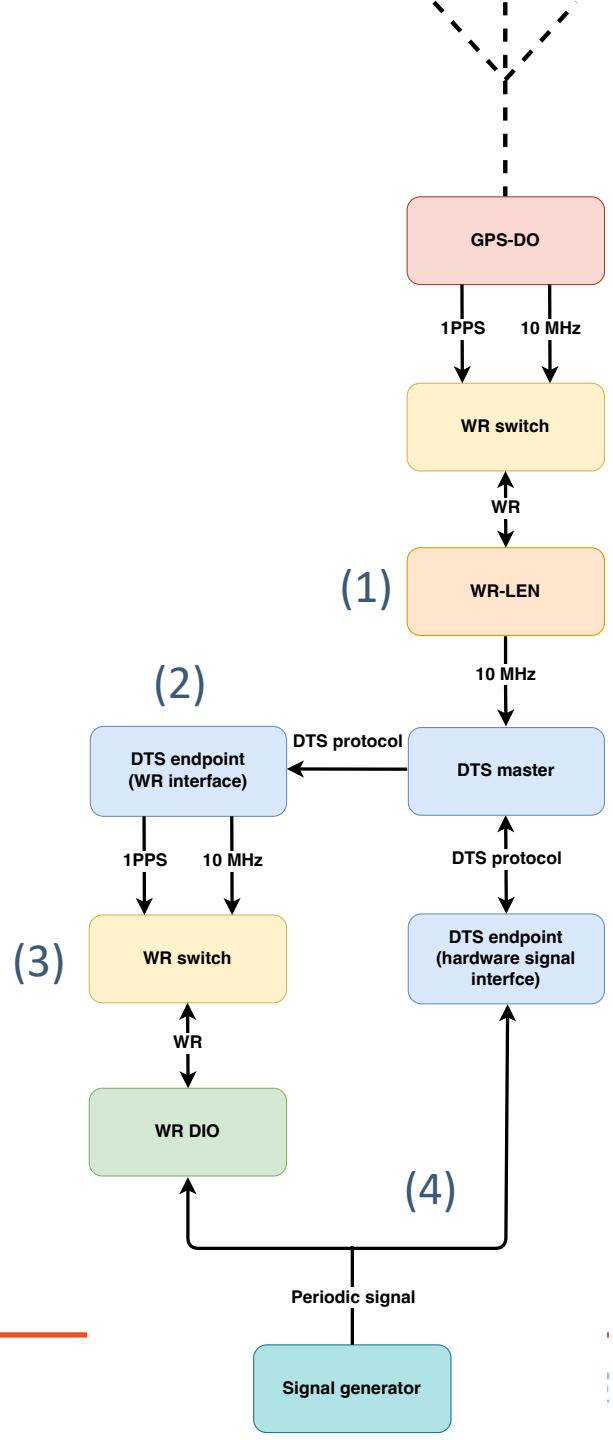
- **Recent developments (DUNE DAQ v4.0.0)**
  - Software state recovery: allows controller application restart without hardware being reset
  - Endpoint monitoring service: monitor DTS endpoints, and log their status
  - Transition to new series DTS firmware as default: electronics and software now assume new series DTS firmware, e.g. default configuration parameters
- **Upcoming features**
  - MIB v2 hardware and firmware low-level support
  - FIB+AFC v4 hardware and firmware low-level support
  - GIB hardware and firmware low-level support
- **Upcoming features – longer term**
  - High-level support for new hardware+firmware: i.e. control, configuration, monitoring interface DUNE DAQ/run control
  - Endpoint round trip time monitoring and equalisation algorithm with new hardware+firmware
  - New endpoint portioning scheme

Timing for Vertical Drift

- **DTS provides a uniform interface to readout systems in DUNE**
  - Timing received by readout and transferred to “front ends”
- **Vertical Drift Top Electronics uses White Rabbit (IEEE-1588 2019) for synchronization**
  - Need to derive WR from DTS, and synchronise the two systems
- **DTS→WR interface proposed**
  - Hardware tests with VD TDE conducted to re-affirm that WR can be synchronized from DTS
  - Next steps:
    - Study stability of timestamp synchronisation: on-going
    - Develop procedure of delivering DTS-WR timestamp offset to TDE
    - Verify DTS timestamp correctly applied to TDE data

DTS-WR interface test

- DTS generates its 62.5 MHz clock from 10 MHz clock provided by WR-LEN (1)
- DTS endpoint provides 10 MHz and 1PPS to WR (2)
  - WR switch time of day taken from NTP
  - **Verified WR switch able to lock to 1PPS and 10 MHz coming from DTS endpoint (3)**
- Signal from independent pulse generator timestamped by both WR and DTS (4)
  - Demonstrated that DTS and WR are locked together (with an offset)
  - The offset between timestamps shown to be stable between WR master reboots



Timing in 2023

- Aim to provide full DTS chain at CERN by Q4 2023
- Continue DTS-WR integration at CERN
- Continue supporting other hardware integration at CERN

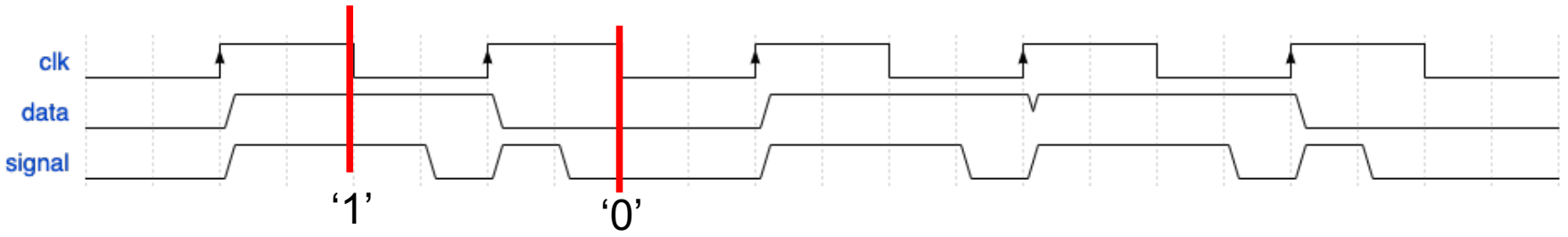
Back-up

Timing system current data encoding

- Timing system protocol currently uses 8b10 encoded NRZ data at 312.5 Mbit/s (for 62.5 MHz master clock)
- Clock, data recovered using an ADN2814 CDR chip
- **ADN2814 not available from regular suppliers**
  - No stock promised before 2023
  - Not declared obsolete – victim of global Silicon Chip Shortage
- Only available device with suitable data rate and zero configuration
  - i.e. only component in timing system that can't be replaced by alternative device
  - Would be good to remove this single point of failure even if short term remedy available
  - Want to support DUNE for lifetime of experiment. Including development of ND
- **Introduce data encoding which does not need a CDR chip**

New timing system data encoding

- Transfer data by modulating duty cycle of a “clock” signal
  - **Duty Cycle Shift Keying**
- Using 25% = 0 , 75% = 1 , 50% = “Z”



- Not naturally DC-balanced → Use 8b10b encoding
- **No external CDR chip required**
  - Future board designs remove or bypass ADN2814
  - Thought to be backwards compatible (CDR in signal path)
- Discussions between DAQ and other consortia under way

DTS-WR interface test results