NSLS-II BxB BPM and EPICS Interface using RFSoC FPGA

EPICS

EPICS Collaboration Meeting in April 2023

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Fermilab

EPICS Collaboration Meeting at the Fermi National Accelerator Laboratory.

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Brookhaven National Laboratory

National Synchrotron Light Source II

Outline

- ❑ BxB BPM
  - BxB BPM and RFSoC
  - BxB BPM supported functions
  - New BxB BPM data processing
  - Measurement data review
- ❑ FPGA CPU and EPICS
  - FPGA and IOC interface
  - ARM CPU threads
  - OPIs
- ❑ RFSoC applications for NSLS-II
- ❑ Summary

NSLS-II RF BPM vs. BxB BPM

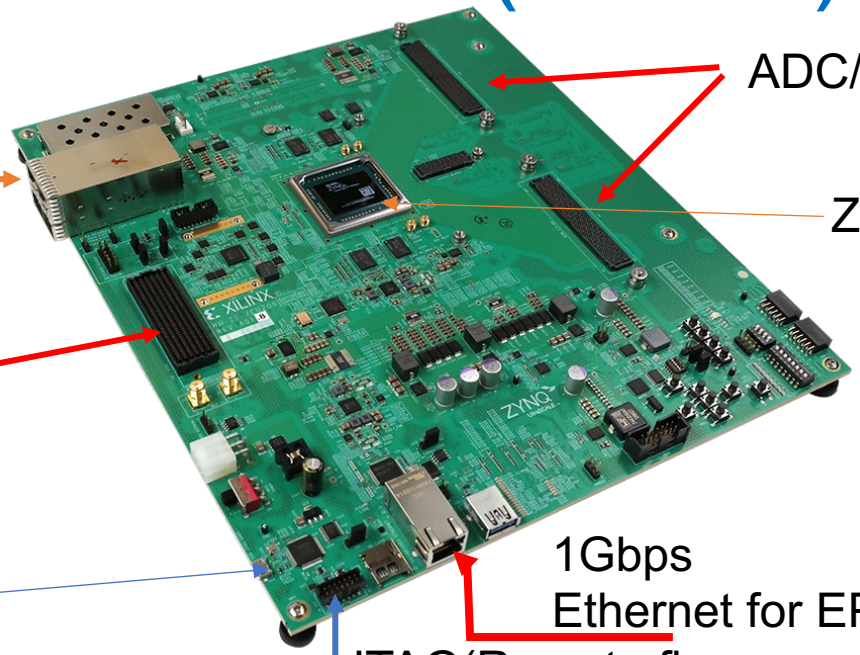
- Analog LPF&BPF (500 MHz +/-5M)
- ADC sub-sampling ~117 MHz (RF=500 MHz)
- Digital Down Conversion
  - I/Q demodulation
- Decimation low pass filter(FIR, CIC, Averaging) for TBT, FA, SA
- Narrow band high resolution

- Analog LPF > 1GHz (No BPF)
- ADC direct over-sampling 5 GHz (RF=500 MHz)
- Negative peak bunch amplitude processing(No I/Q)
- Direct conversion bunch amplitude to BxB position
- Decimation low pass filter(FIR, CIC, Averaging) for TBT, SA
- Wide band(~3 GHz), include Image signals

BxB BPM applications

- BxB transverse beam position measurement
- Calibrate beam oscillation
- Model independent lattice characterization(needed 2 BxB bpms)
- Bunch charge measurement
- Injection transient measurement
- Coupled bunch instability
- Beam dump analysis

Xilinx ZCU208 RFSoC (GEN3)



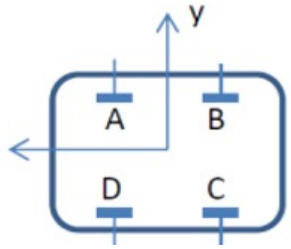
- Zynq Ultrascal+ FPGA, ARM CPUs(x4), and high-speed ADC/DAC combined in one chip, and it is called RFSoC (System On Chip)
- Comprehensive RF ADC/DAC development platform
- 14-bit 8 Channel ADC, max 5 Gsps
- 14-bit 8 Channel DAC, max 10 Gsps
- NCO, DDC/DUC and ~x40 decimator

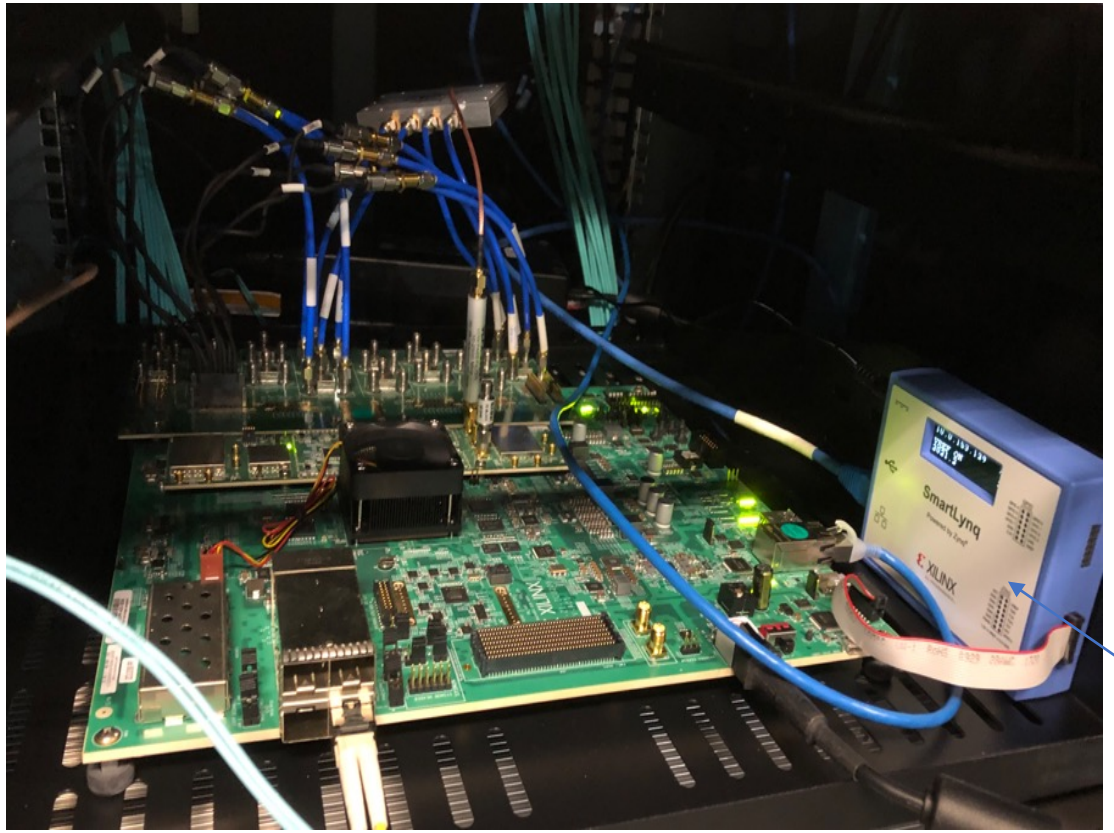
RFSoC BxB (500 MHz) BPM

- ZCU208 board for prototype(firmware development, beam test)
- 5 Gsps ADC sampling each bunch (bunch space is 2ns)
- Extracting Positive/Negative peak bunches from X10 sampled ADC raw data
- 500 MHz BxB x/y position calculation
- BxB Gate function for select interested bunches from 1320 buckets
- The FPGA processing clock is 499.680 MHz (Sync with RF frequency)
  - Peak bunch amplitude sampling and processing
- External and Internal PLL for clock Sync and tracking the RF changes (by RF feedback)
- 10 k turns x/y PM data capturing

Cell 14 Test setup for Beam test

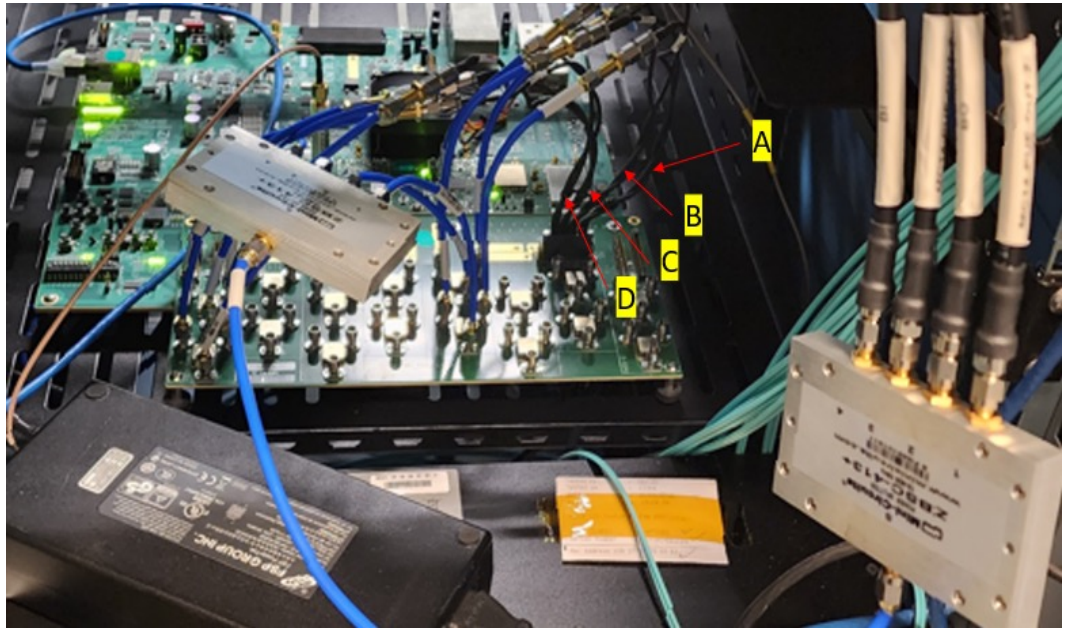
- TO (A)
- TI (B)
- BI (C)
- BO (D)





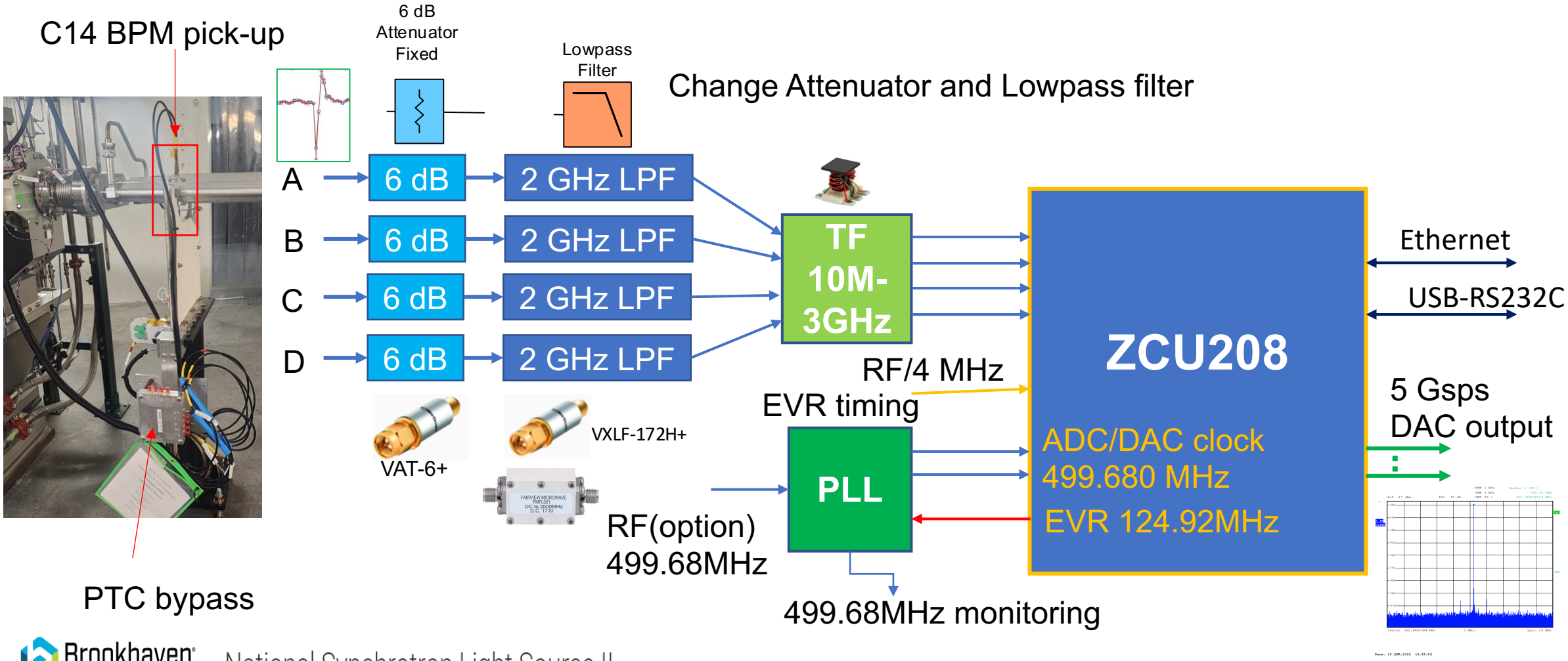
Front

JTAG



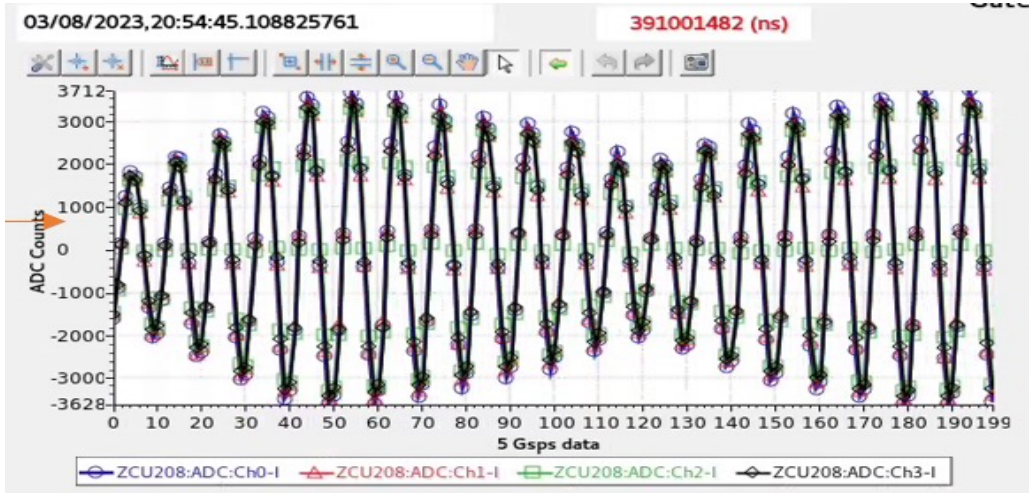
Rear

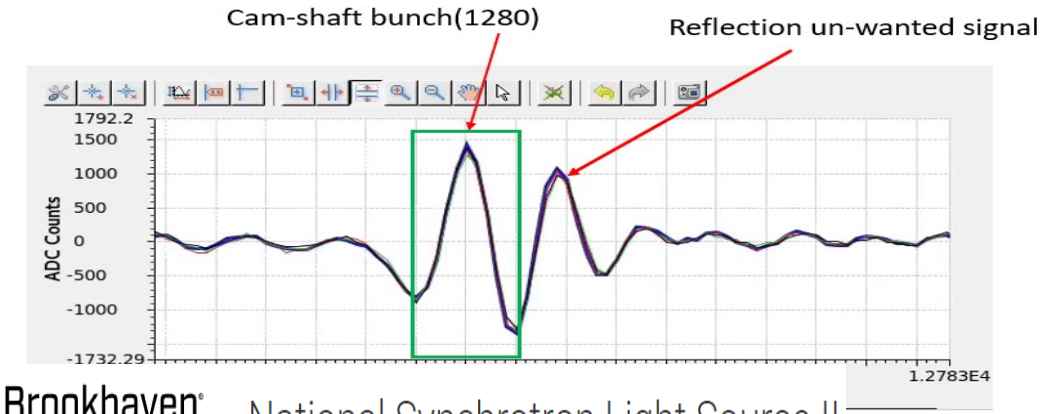
Cell 14 Setup for beam test – Rev. 2



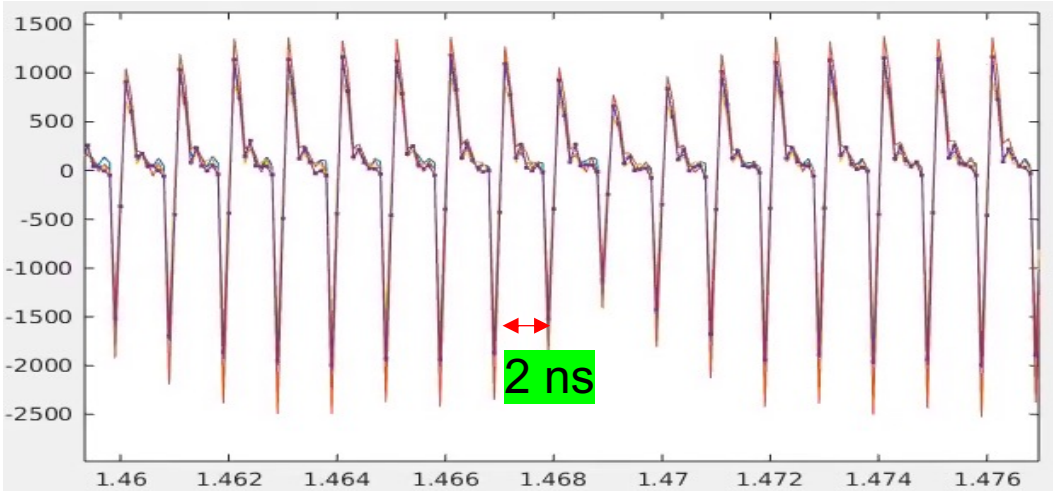
RF front-end changes and response

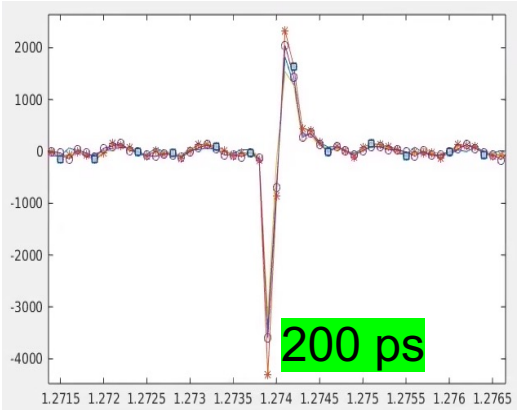
Rev. 1: With PTC and Splitter box (< 1GHz BW)

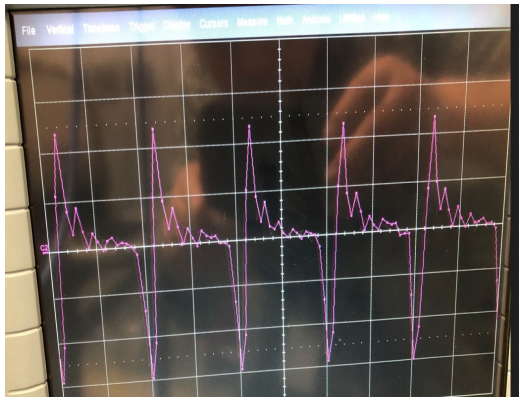




Rev. 2: Bypass PTC and Splitter box
6 dB attenuator and 2 GHz LPF (4/5/23)





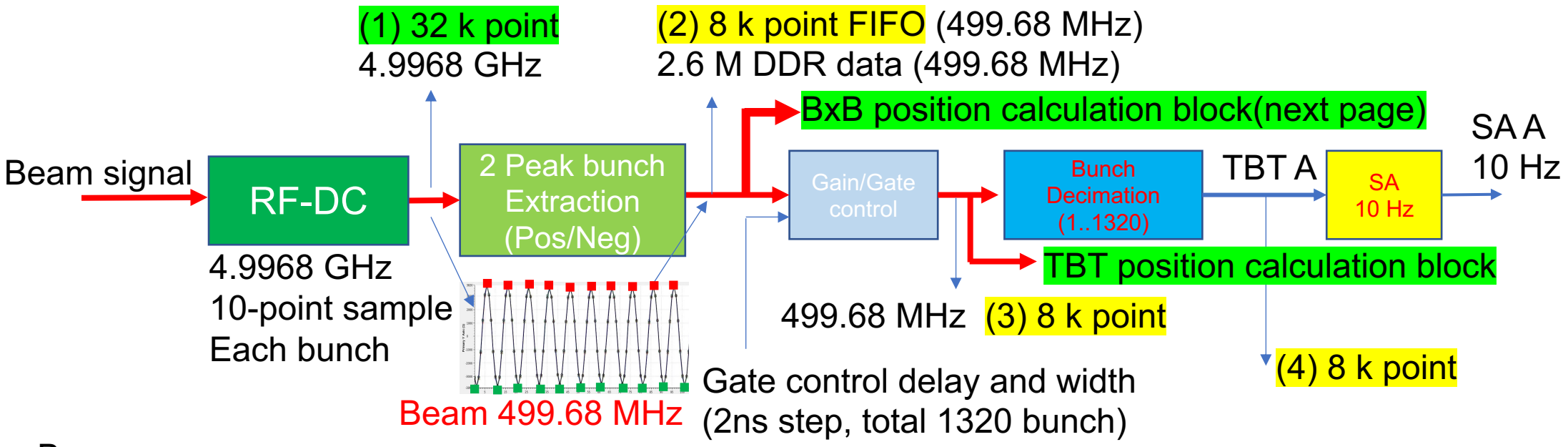


Oscilloscope

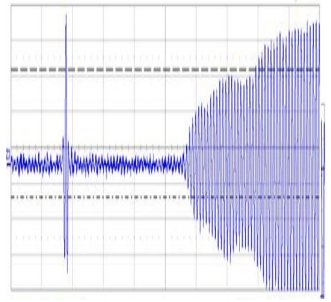
Supported EPICS data

- 5 Gsps A/B/C/D raw data – 32 k point (~3 turns) waveform
- BxB: 500 MHz A/B/C/D peak bunch – 2.64M (2000 turns) waveform
  - Individual bunch (0-1319) A/B/C/D – (1320*2000) - 2000 turns
  - Individual bunch (0-1319) X/Y (1320*1000) – 1000 turns
- BxB x/y PM waveform ~1320*2*10k turns(26.4M points)
- TBT: A/B/C/D/X/Y – 8 k turns waveform
  - Available select bunch numbers(gate function)
- SA: A/B/C/D/X/Y/S - 10 Hz stream
  - Long-term stability measurement
  - Gain/BBA Offset calibration

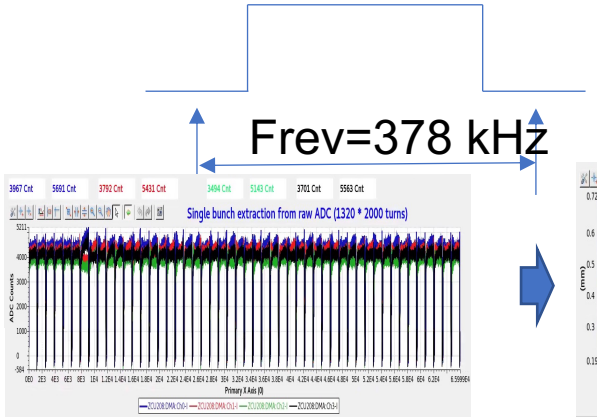
FPGA data processing for BxB (Channel A, B/C/D are identical)



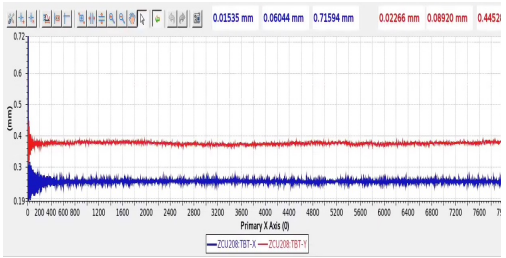
Beam



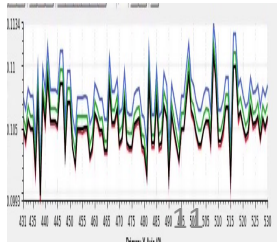
5 Gsps ADC raw



TBT(378 kHz)



SA(10 Hz)



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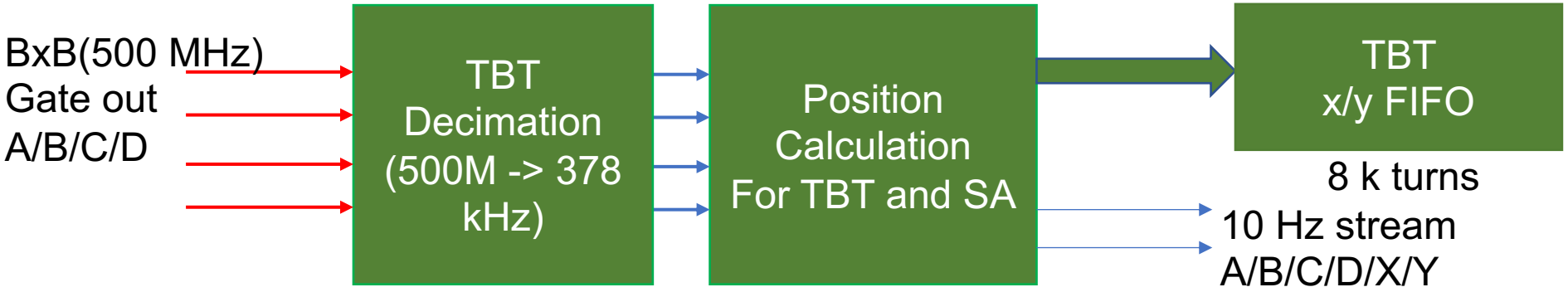
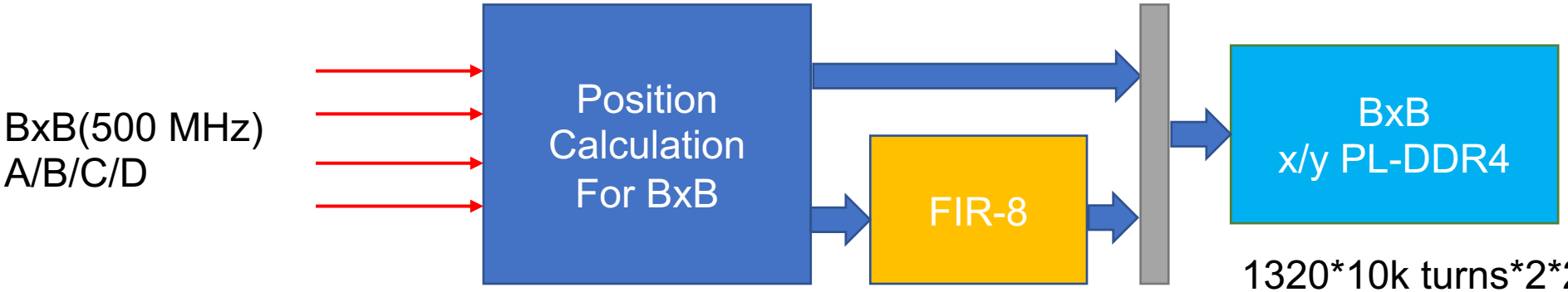
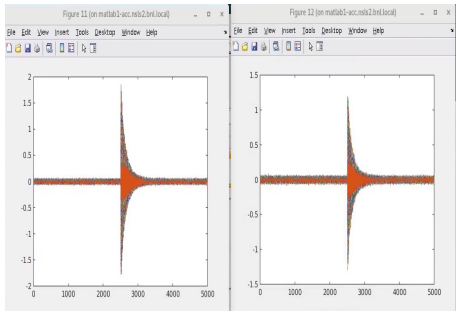
FPGA X/y position calculation for TBT and BxB PM

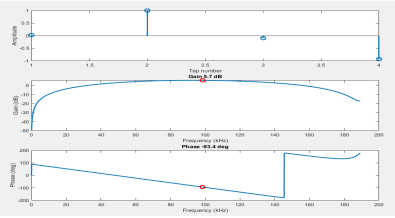


- Stream data processing

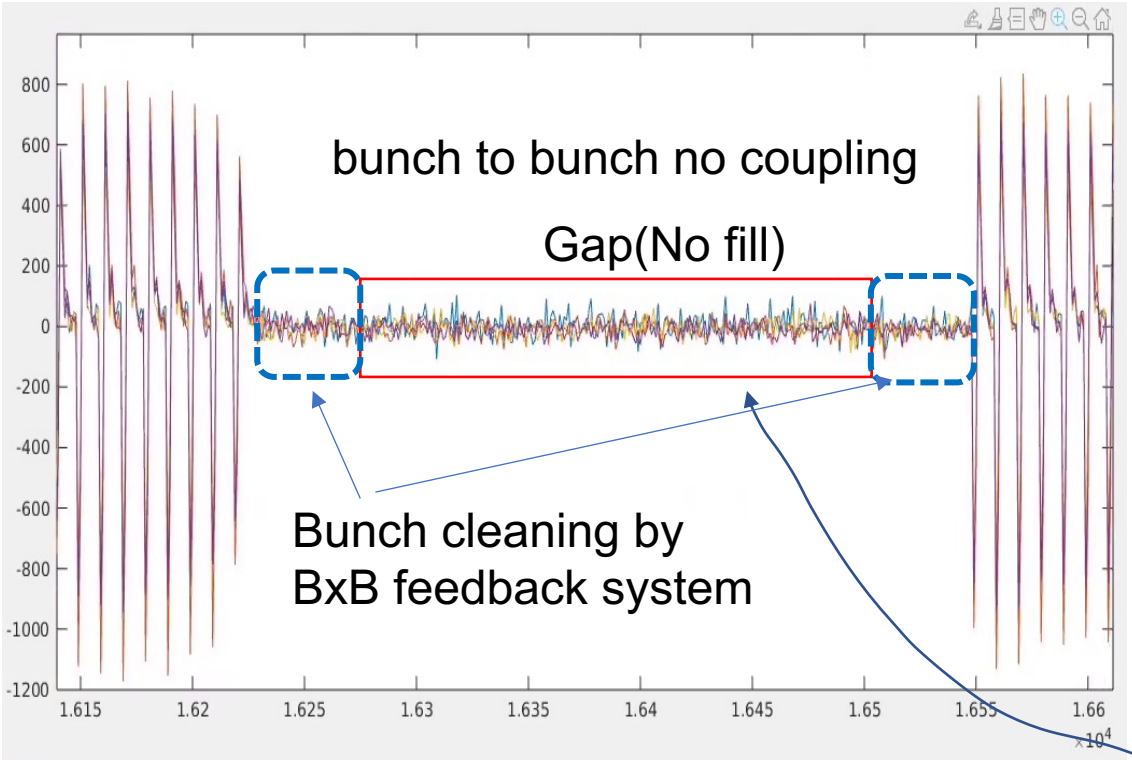




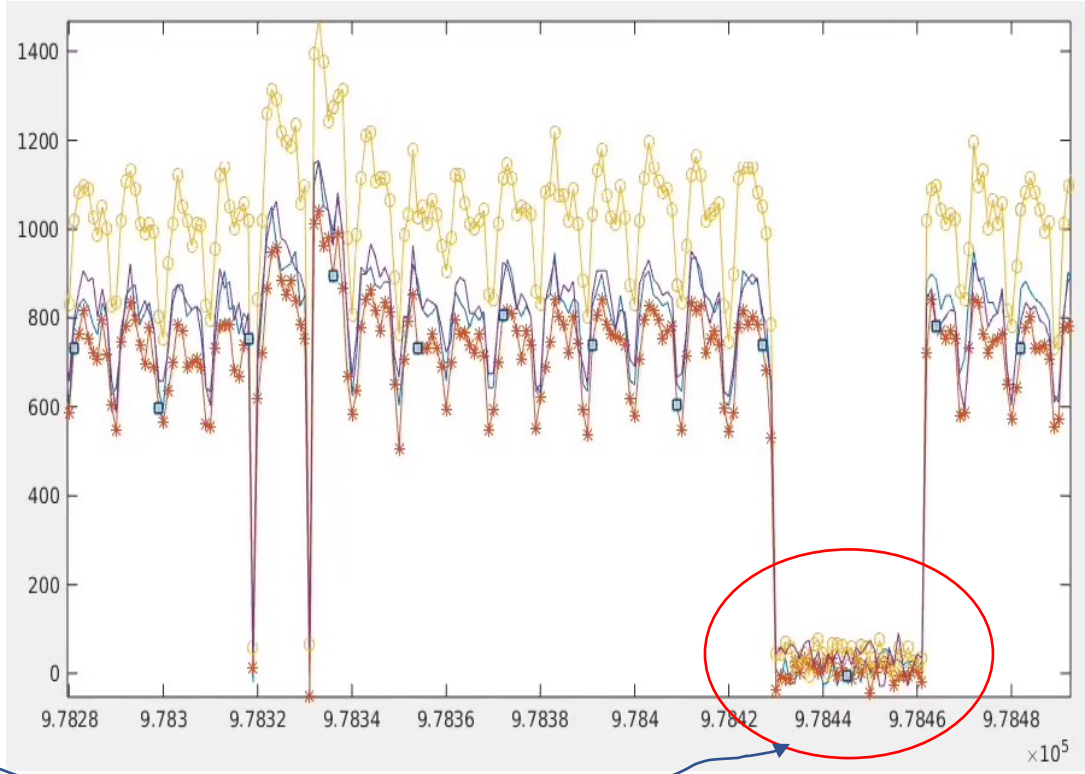
1320*10k turns*2*2 = 52Mbytes



Bunch coupling measurement



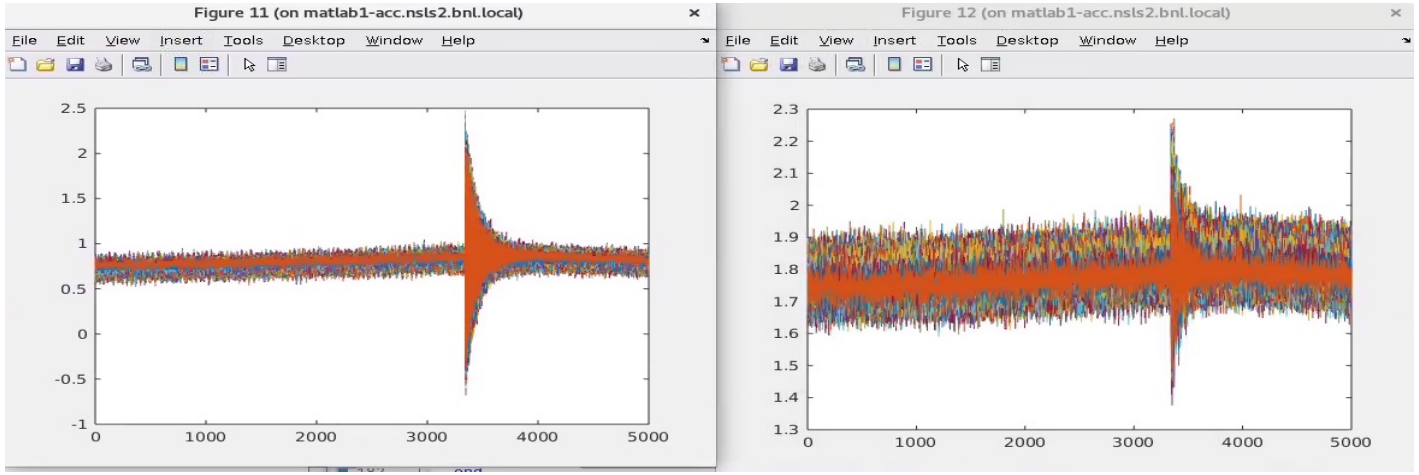
5Gsps ADC Raw A/B/C/D



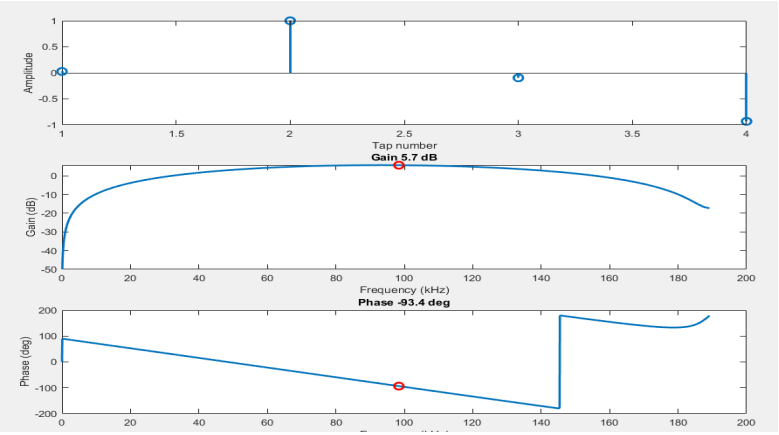
BxB 500 MHz A/B/C/D

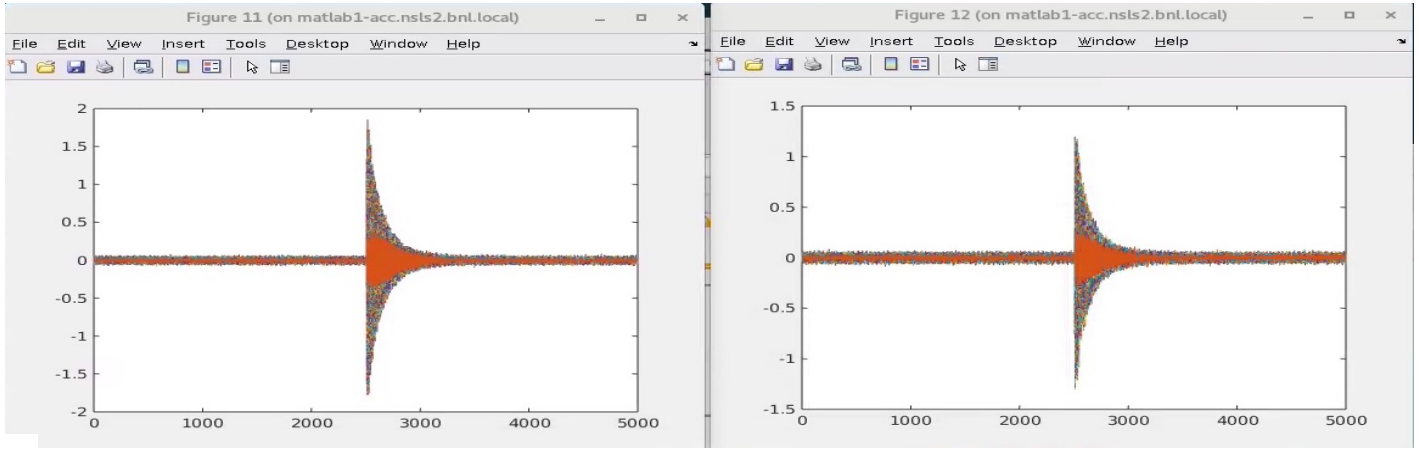
Top off injection transient (FIR HP filter output), negative peak signal for PM x/y position capturing

PM Position



PM FIR 4 tap

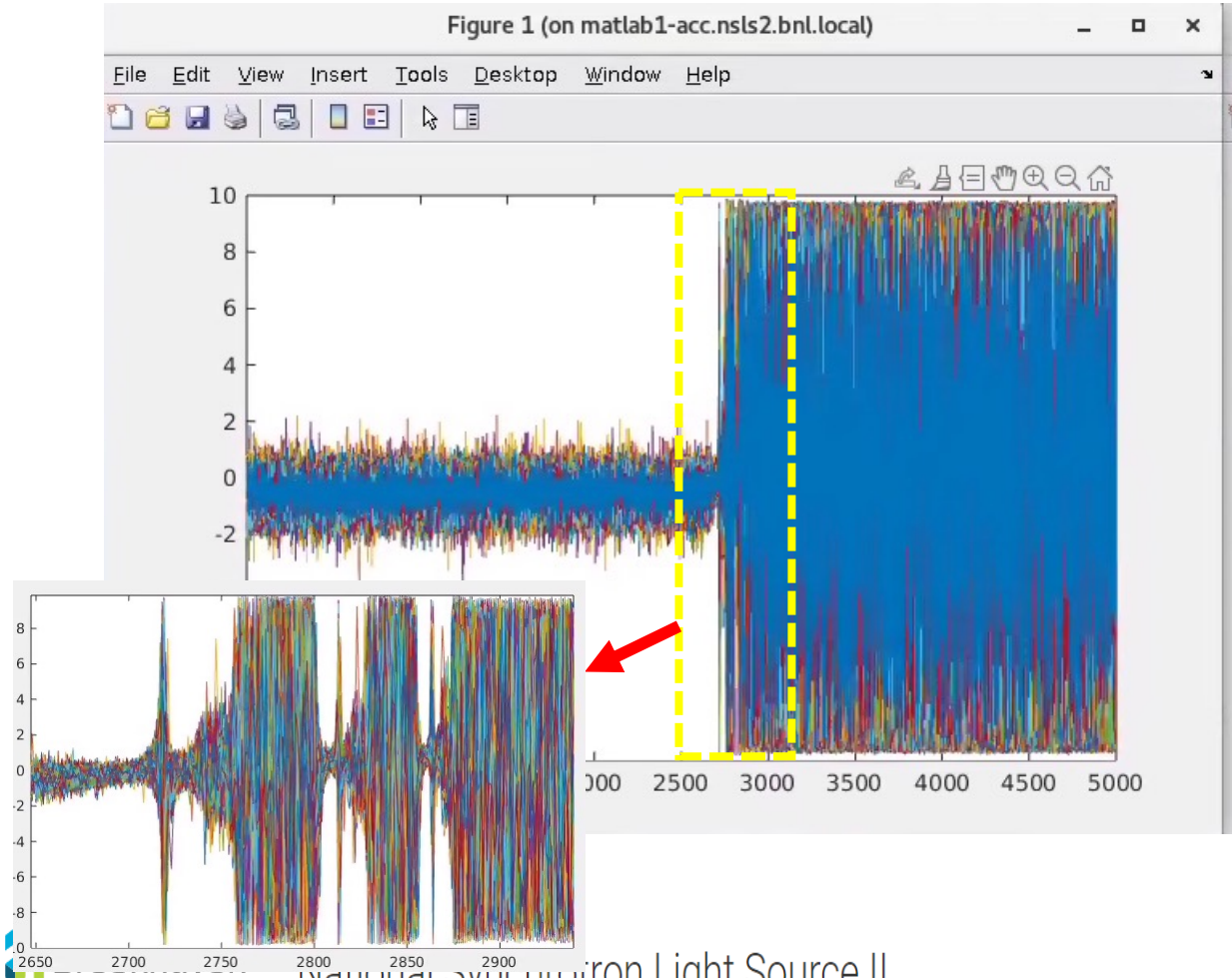




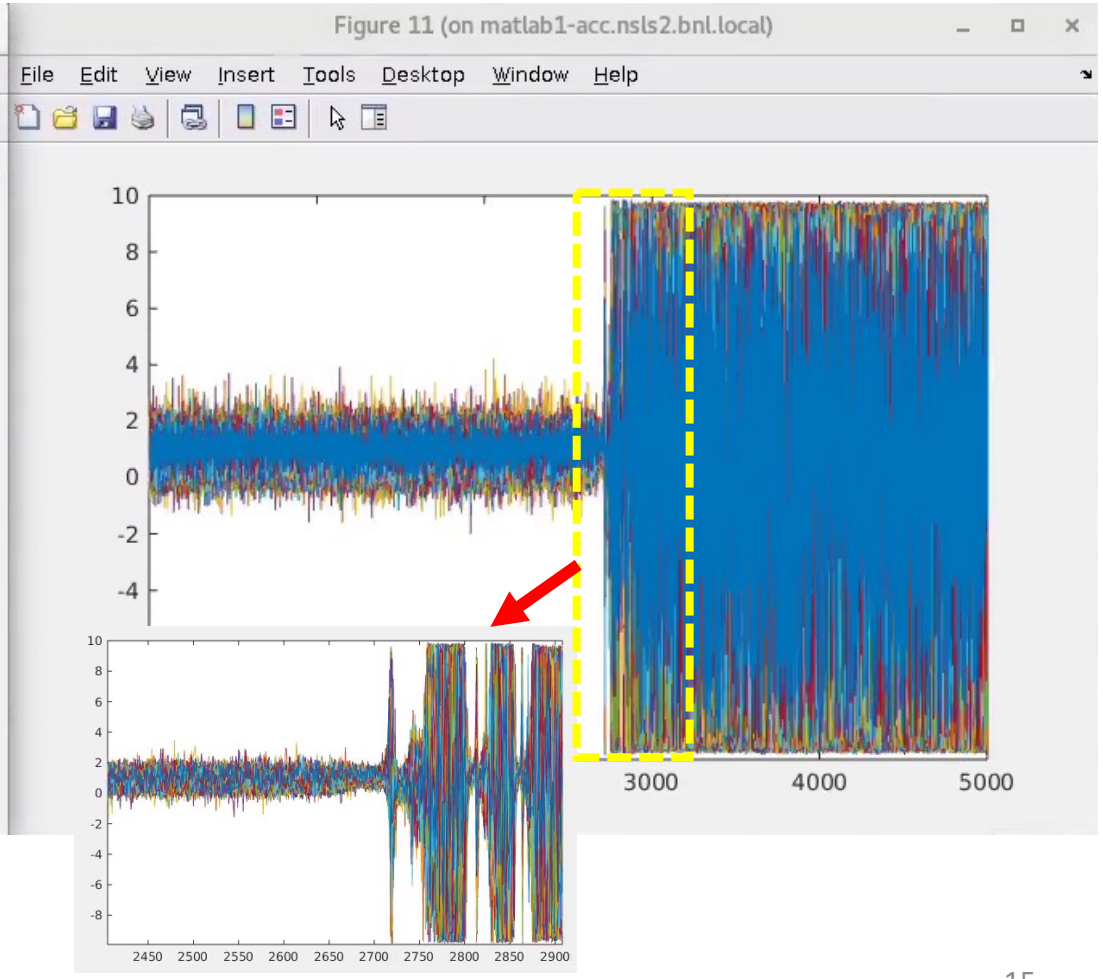
PM Position FIR output x/y

PM data collection : RF fast dump from AI(ID28-7)

X bunches

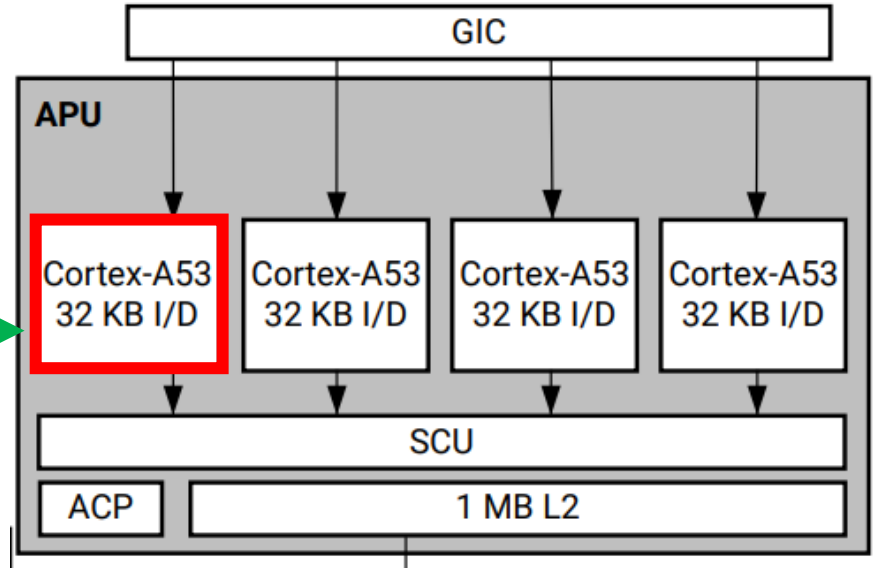


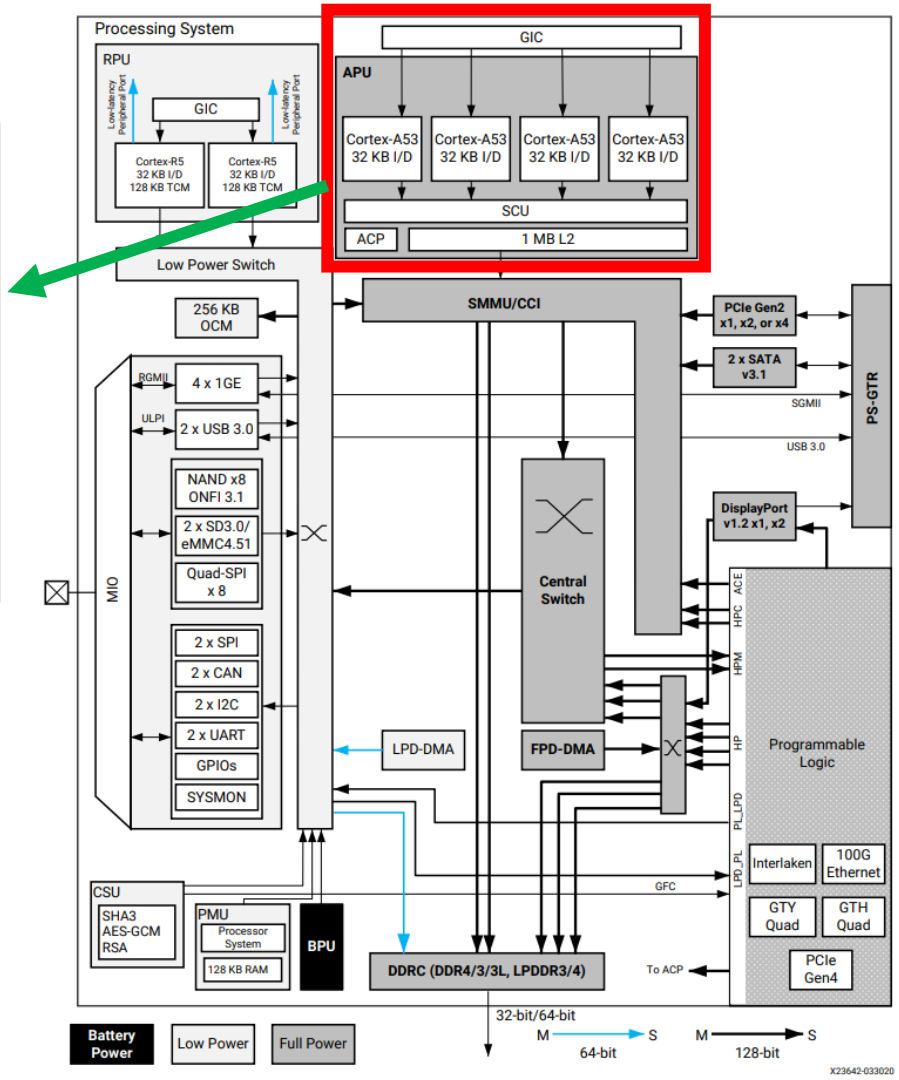
Y bunches



RFSoC APU (Same architect with MPSoC)

CPU for EPICS Interface

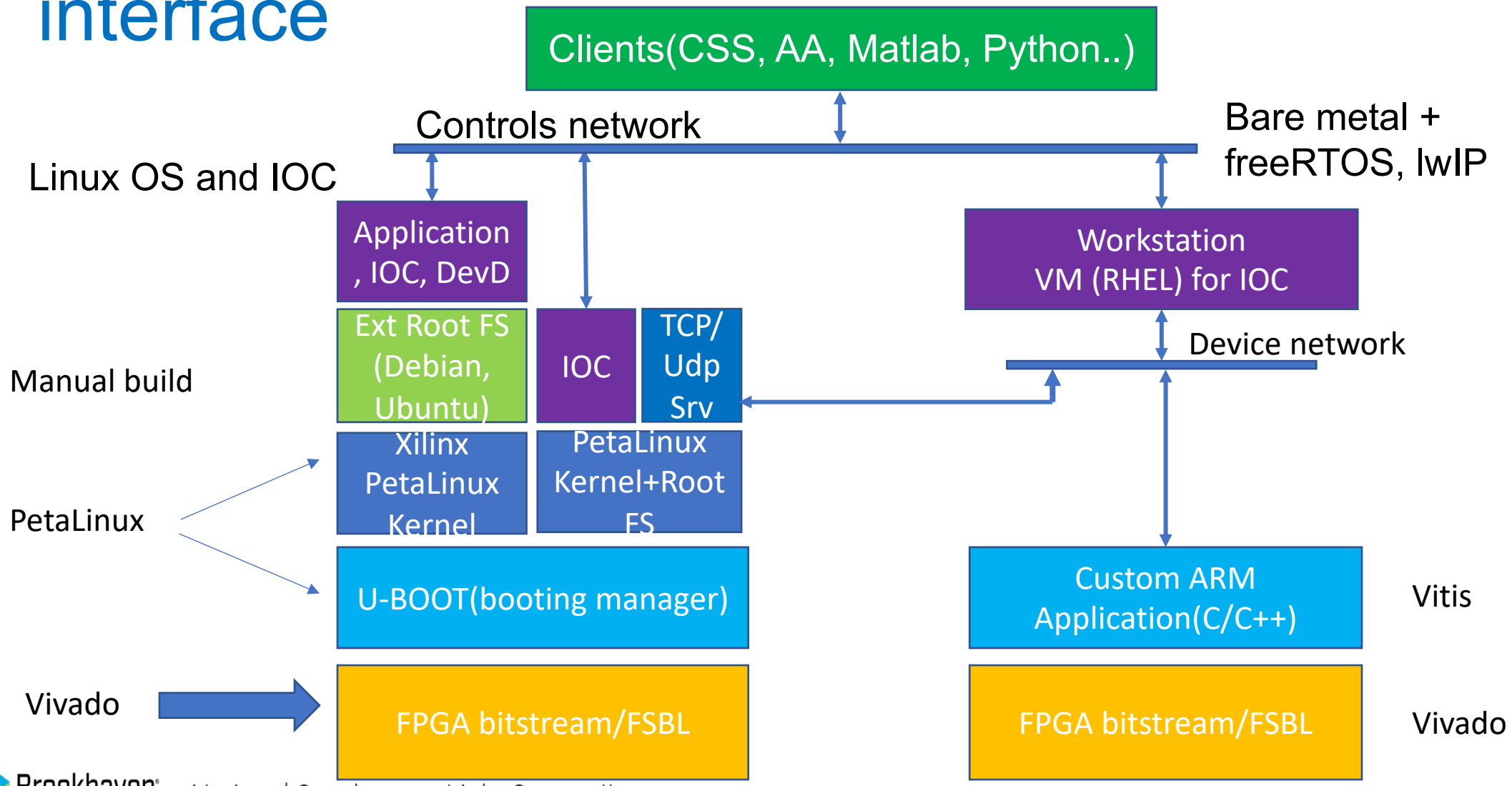




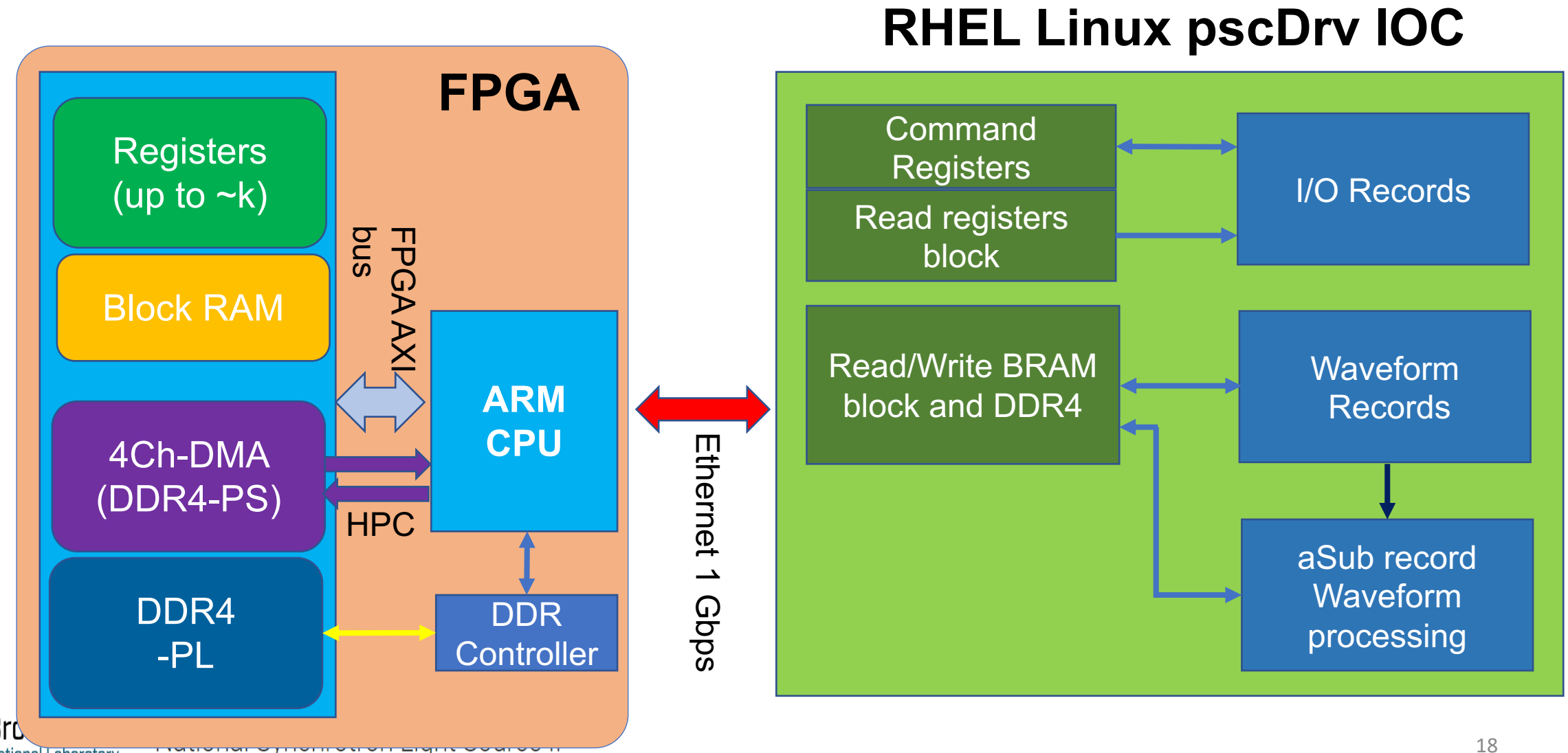
- ❑ PS : 4GB 64-bit, 2400MT/s
- ❑ PL : 4GB 64-bit, 2666MT/s

ZCU208 Evaluation Board User Guide (xilinx.com)

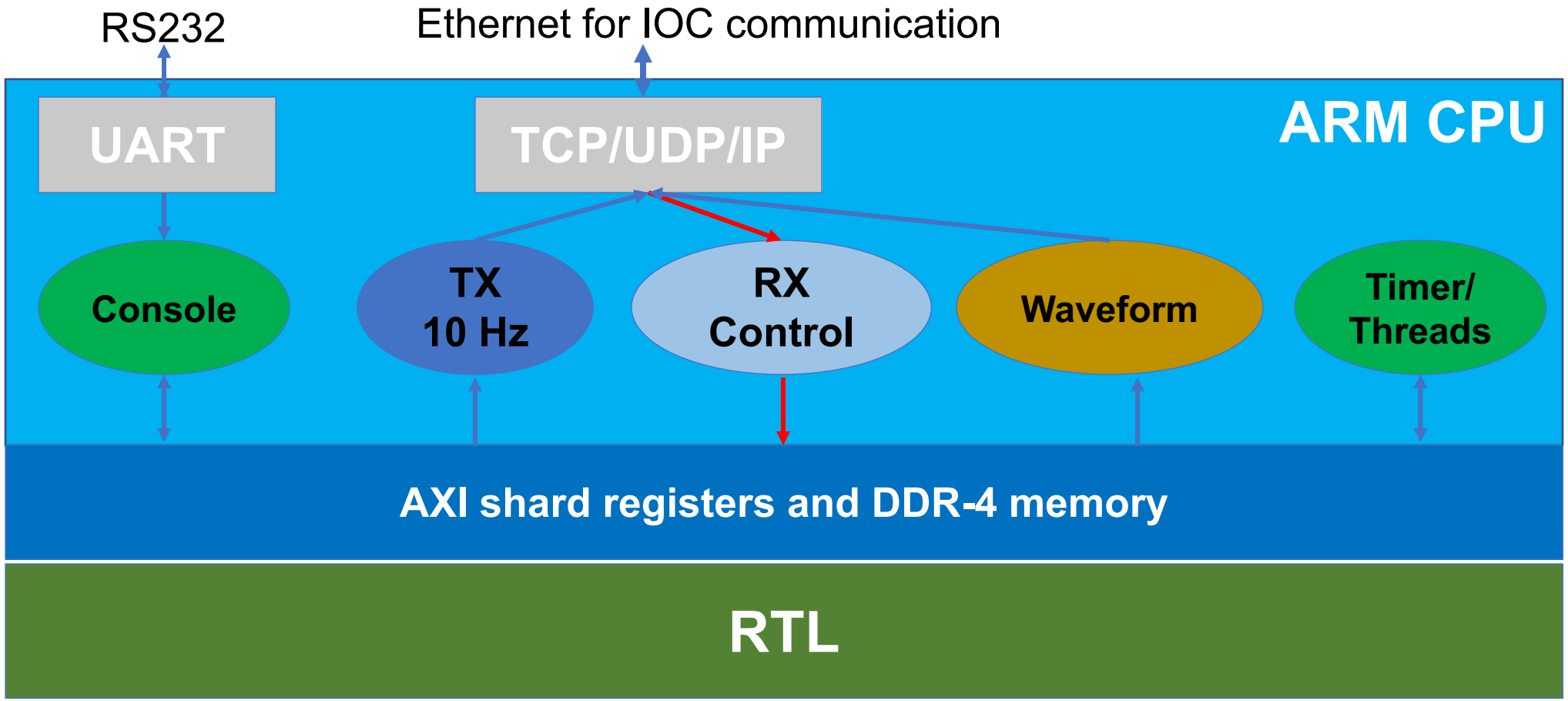
FPGA and ARM application for EPICS interface



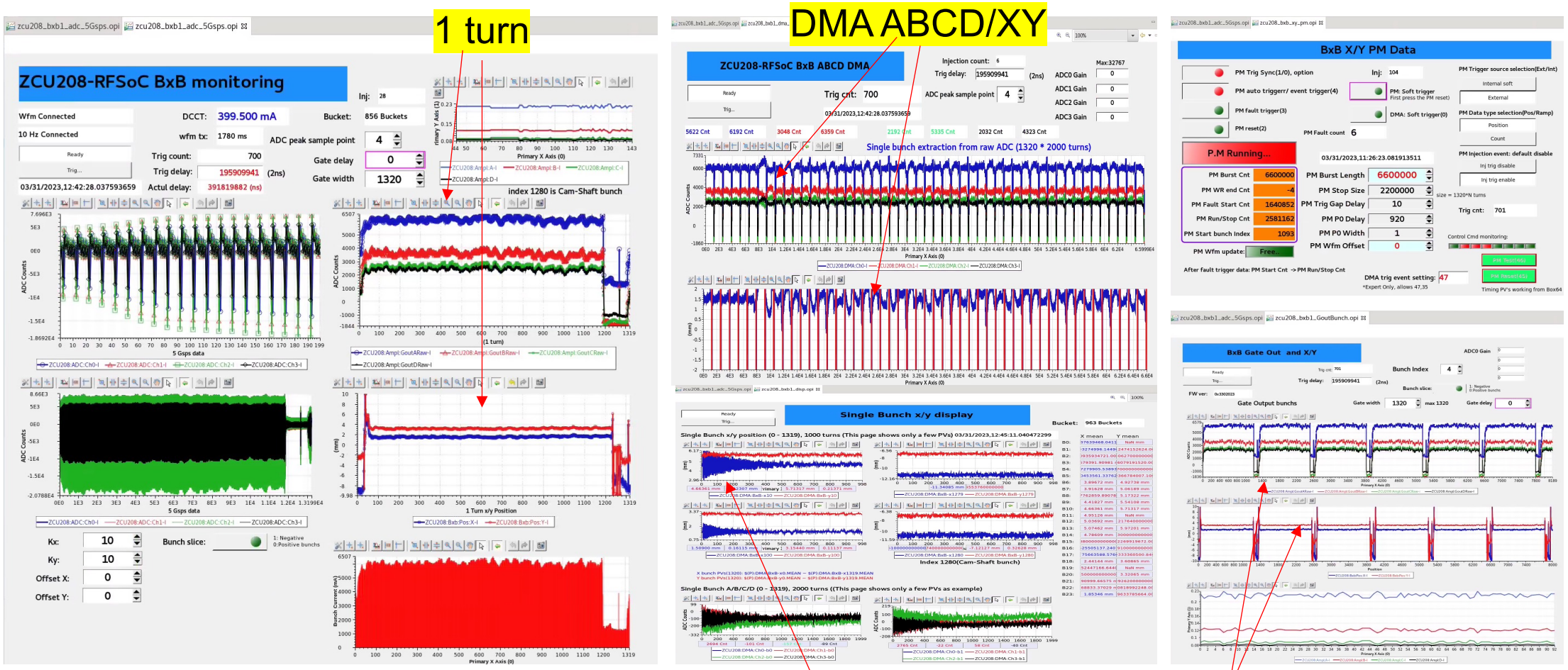
FPGA and EPICS IOC Interface



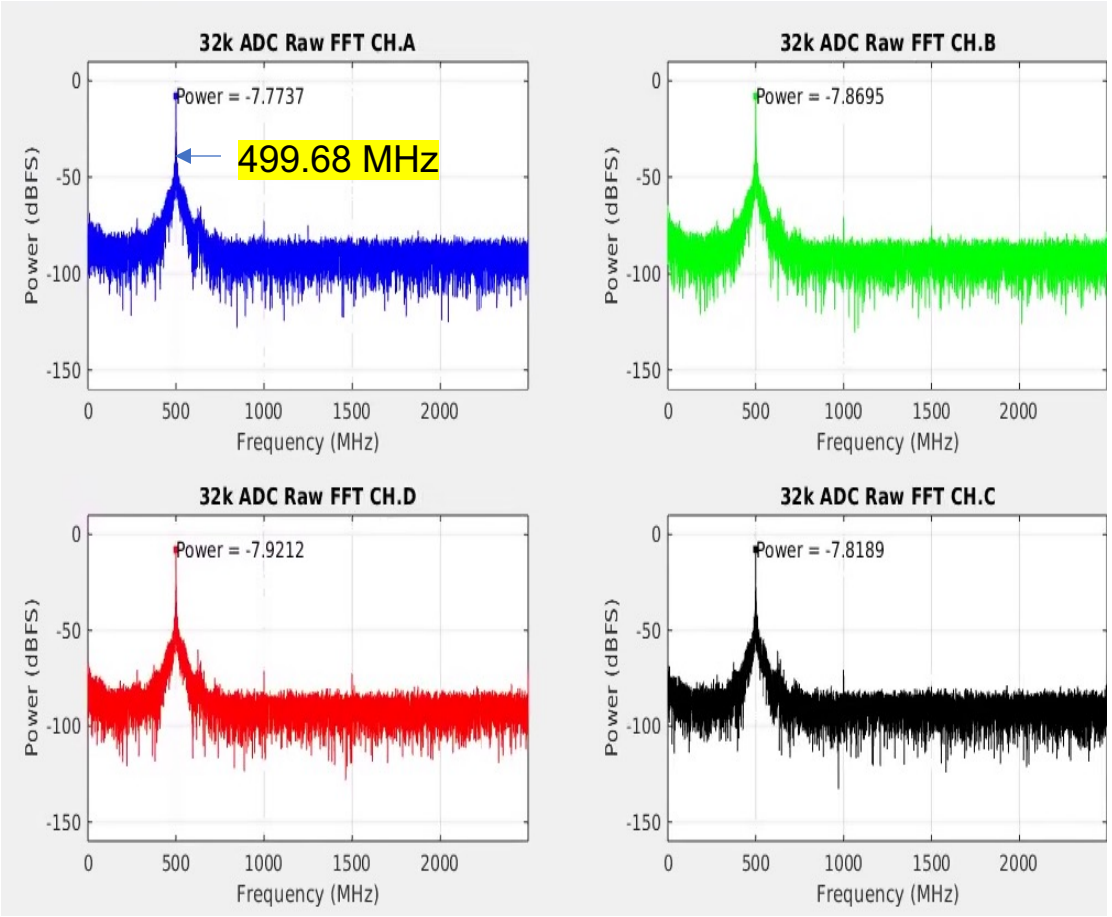
ARM TCP/UDP/IP server (freeRTOS+lwip)

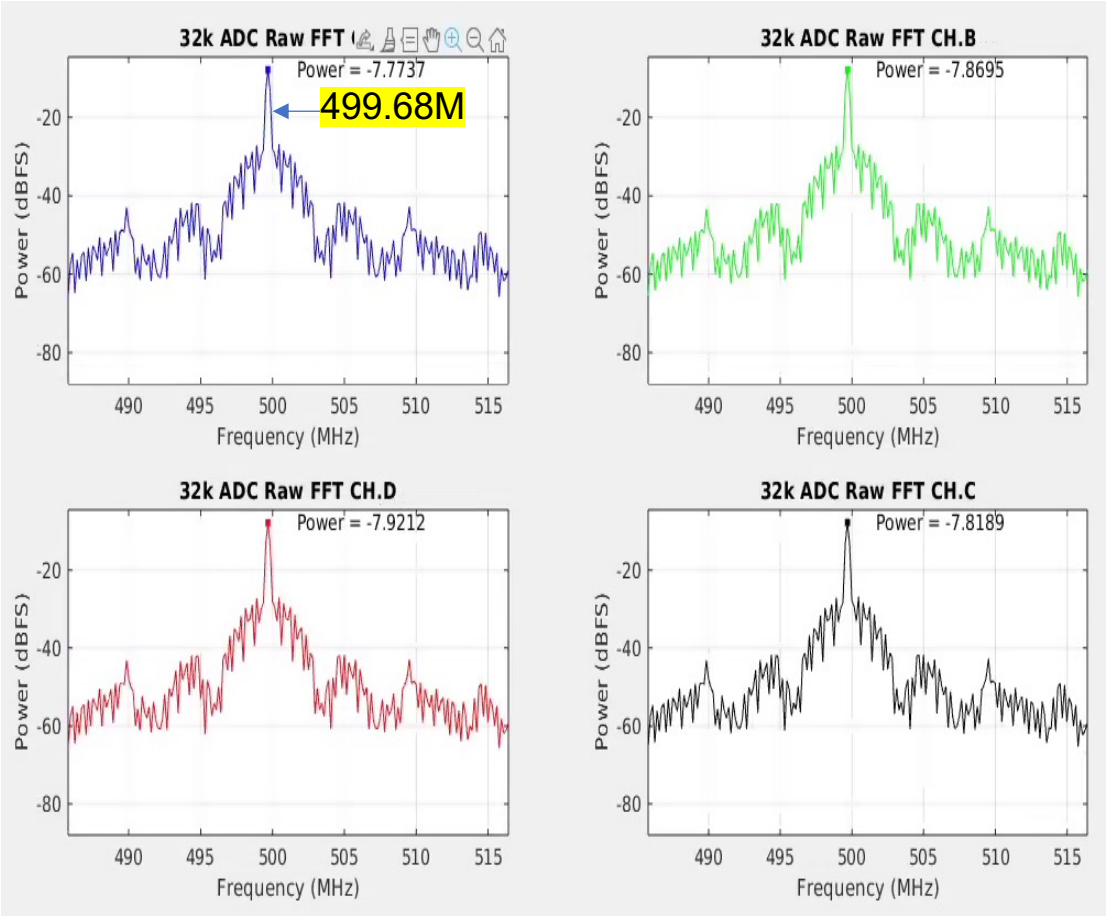


OPI CSS example



Matlab CA and 5Gsps 32 k point FFT





NSLS-II RFSoC based development project

- BxB BPM – 1st project and good progress, Diagnostics/controls
  - Firmware development and beam test complete, planned user beam study
- LLRF Controller – RF/controls =
  - Start evaluation
  - EPICS interface discussion
- RF BPM – Plan, Diagnostics/controls
  - Decimation, I/Q demodulation and basic function test
- BxB feedback system – Study, Diagnostics/controls
  - N-taps FIR, DAC I/Q NCO, turn delay, fine delay(3.3 ps step) function test
  - Emittance growth control study
- Other projects as needed
  - Longitudinal phase measurement(beam arrival time)
  - High speed digitizer
  - PT generator

Summary

- FPGA firmware is working for all requirements
  - System processing clock is 499.68 MHz and no timing issues
- Fully functional an EPICS IOC interface and OPIs
- Beam test result was good
  - Tested single bunch mode
  - Tested multi bunch mode
- Will release for operation 1st BxB system
- Start user service and collect requests from physics group
  - Selected Facility Improvement Project and will install dedicated two BxB BPM

Thank you for your attention!

Questions and comments are welcome.