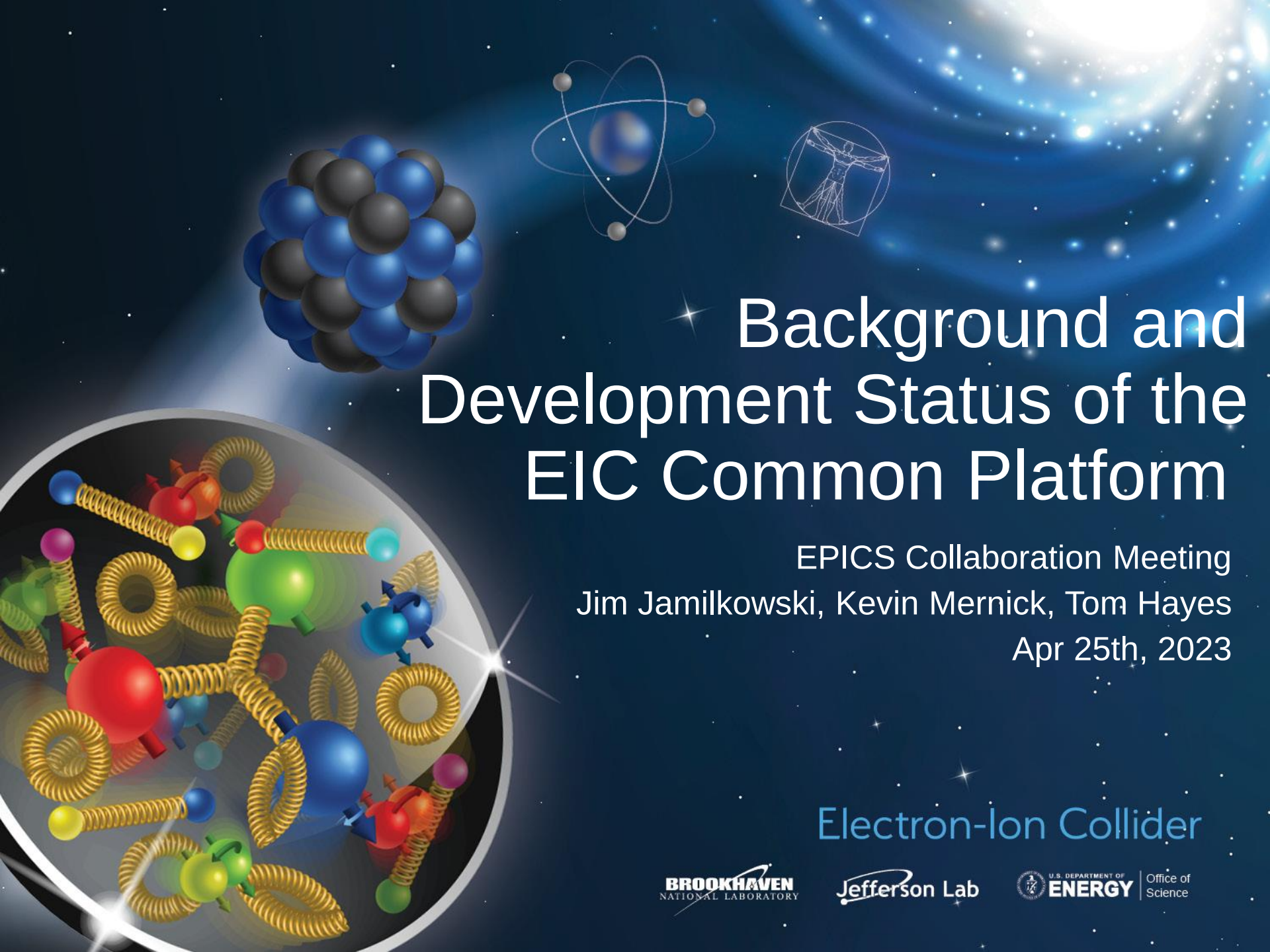

Background and Development Status of the EIC Common Platform

EPICS Collaboration Meeting

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Apr 25th, 2023

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY

Jefferson Lab

U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- EIC Common Platform Hardware Concept
  - EIC Common Platform
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  - Recent Projects Involving Zynq FPGA Designs
  - CP Diagram & Rendering
- Common Platform Carrier
  - Layout
  - Functionality
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- Front End Computer Remote Interface
  - FEC Interface Diagram
  - Development Environment
- Overall Status and Plans

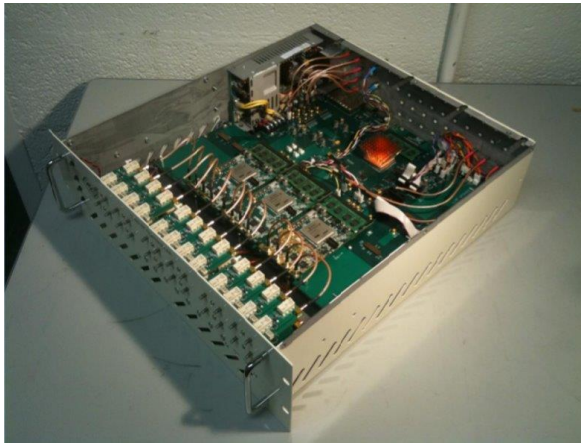
Common Platform Hardware Concept

EIC Common Platform

- Why develop a common platform for the Electron Ion Collider project?
  - Maximize efficiency in labor expenditures
  - Reduce development, production, installation, commissioning, maintenance time and costs
  - Increased system reliability and uptime
  - Reduce technical, cost, and scope risks
  - Reduce cost of spares inventory
  - Improve maintainability and upgradability

RHIC LLRF Chassis Predecessor

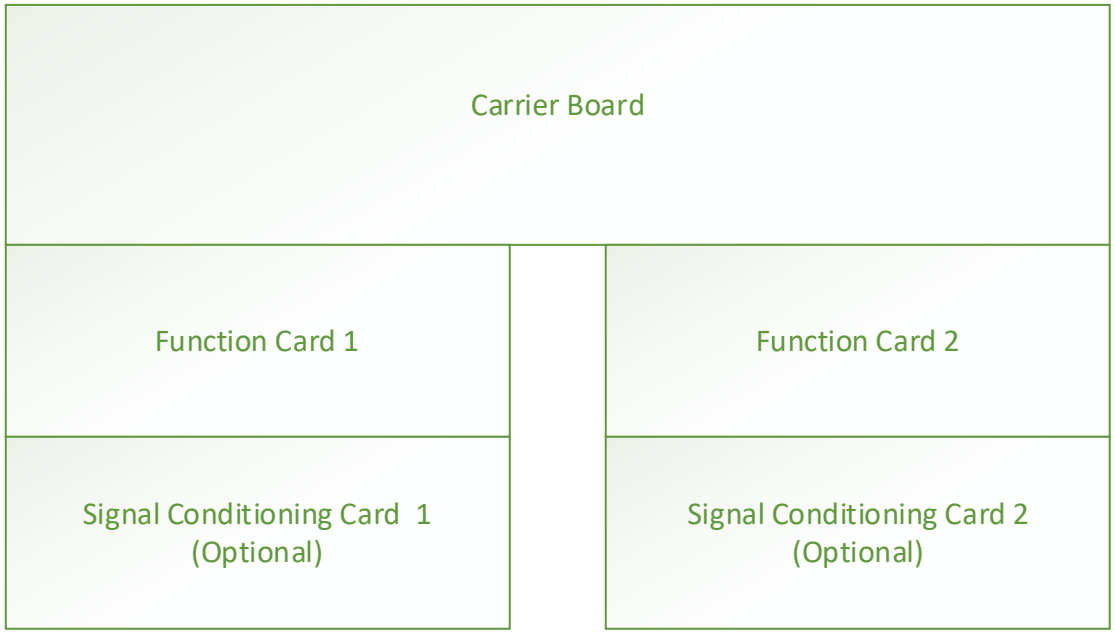
- 3U chassis
- Carrier provides connections to control system, including timing and machine protection
- Provided upgrade path from the original LLRF VME systems
- XILINX SoC platform, Virtex-5 FPGA w/ embedded PPC
- Carrier/Daughter card design, supporting up to 6 modules for specific roles (ex. DAC, ADC, motion, etc)
- in use since 2009... fully deployed at CAD for several years now
- Runs VxWorks RTOS v6.5 (circa mid-2000s)
- Software interface based on BNL/Collider-Accelerator Department proprietary "ADO" interface

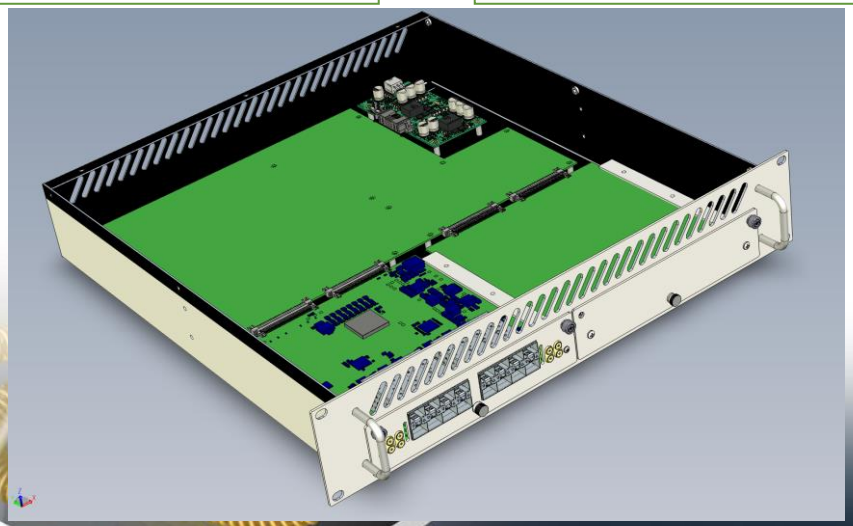


Recent Projects Involving Zynq FPGA Designs

- Since ~2015, there have been small scale deployments of "pizza box" crates employing Zynq development boards and COTS FMC daughter cards running Linux for instrument control
- A VME form factor was used for multiple Zynq-based systems called V301: BPM signal processing, machine protection for BPM signals, and a timing generator used at RHIC, CeC, and LEReC at BNL, and Cbeta at Cornell
- A Zynq-7000 eval board and custom FMC module were used to build a fast-timing generator for the LEReC laser system, with a bare-metal interface
- While these systems demonstrate significant design and operational flexibility inherent to modern FPGA capabilities, the goal of the EIC Common Platform is to provide board and interface standardization in order to reduce NRE and streamline design efforts

CP Diagram & Rendering

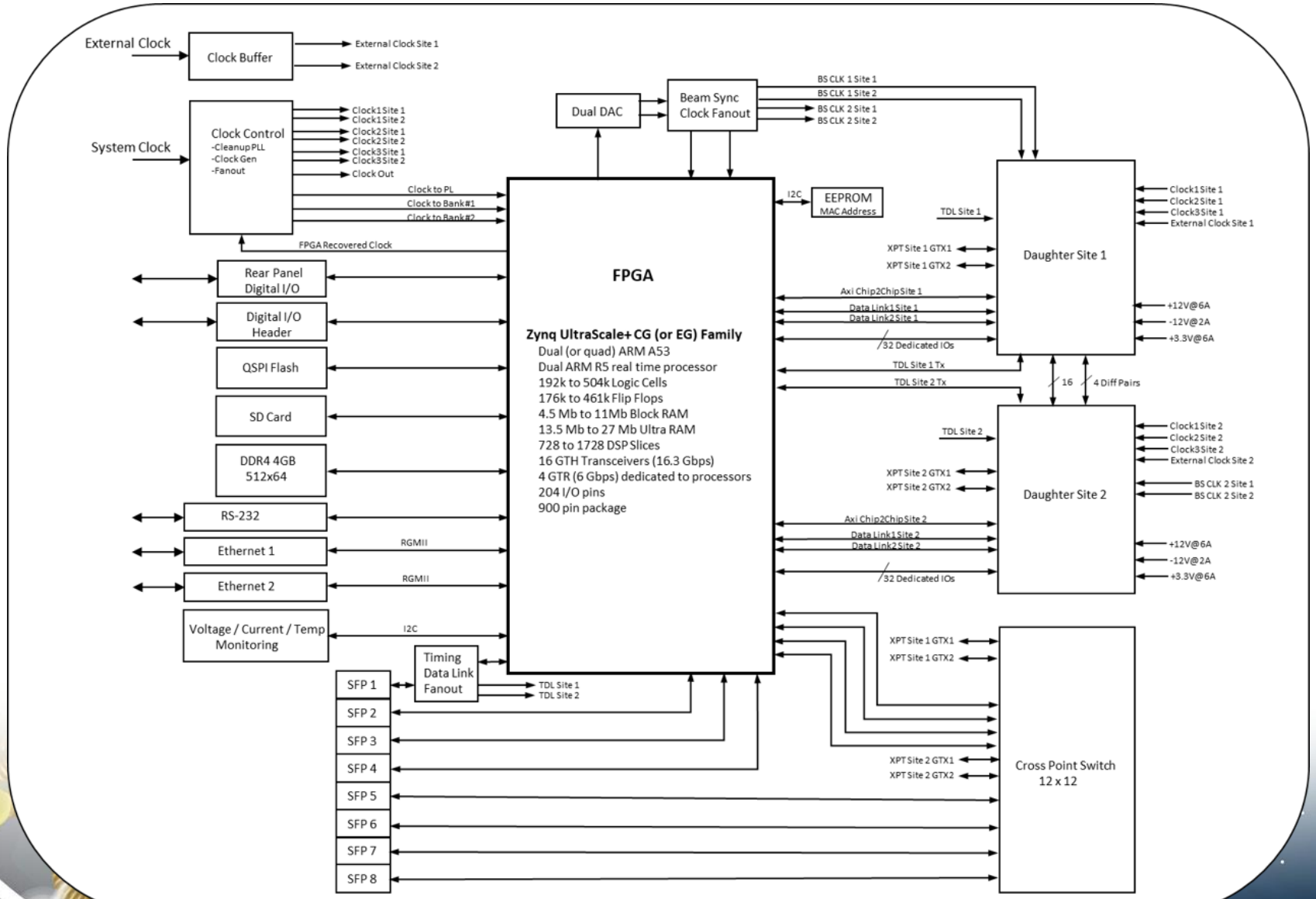




- 2U chassis
- FEC/IOC host interface running on separate commercial 1U blades
- Carrier provides all connections to control system / timing
- Carrier comes in one flavor to reduce NRE
- High speed edge mounted connector allows function / filter cards to be accessed thru front panel of chassis
- Provides upgrade path for existing VME systems

Common Platform Carrier Board

Common Platform Carrier Diagram



CP Carrier Functionality

- Dual gigabit ethernet
- Memory - 4 GB of DDR4
- 8 SFPs – 1 dedicated to Timing/Data Link
- External Clock, Clock Recovery Option, (Clean Up PLL)
- On-board Beam Synchronous Clock generation
  - Available on each carrier using Direct Digital Synthesizers (DDS)
- SD Card & QSPI Flash boot/configuration memories
- UART Interfaces (1 RS-232 Interface, 1 via USB)
- Voltage/Current/Temperature Monitoring
- Two Daughter Sites
  - 3 Dedicated Multi-Gigabit Serial Links to Carrier FPGA, running at 8 Gbps
  - Flexible connection to SFPs, carrier FPGA, or adjacent Daughter site via cross-point switch
  - 32 generic I/O connections to carrier FPGA, 16 generic I/O connections to adjacent Daughter site
  - Real Time and Beam Synchronous Clocks
  - Site to Site Connections (covered in previous bullets)

FPGA Evaluation

Part Number	XC5VFX70T-1FF1136C	XC7Z030-1FFG676C	XCZU4CG-1FBVB900E	XCZU5CG-1FBVB900E	XCZU7CG-1FBVB900E	XCZU7CG-1FFVC1156E	XCAU25P-1FFVA784E	XCAU10P-1FFVB484E
Family	Virtex 5	Zynq-7000	Zynq UltraScale+	Zynq UltraScale+	Zynq UltraScale+	Zynq UltraScale+	Artix UltraScale+	Artix UltraScale+
Logic Cells	71680	125000	192000	256000	504000	504000	308000	96000
Flip Flops	44800	157200	176000	234000	461000	461000	282000	88000
LUTs			88000	117000	230000	230000	141000	44000
Total Block Ram (Mb)	5.3	9.3	4.5	5.1	11	11	10.5	3.5
Ultra RAM (Mb)	-	-	13.5	18	27	27	-	-
DSP Slices	128	400	728	1248	1728	1728	1200	400
Transceivers (Max Data Rate)	16 (6.5 Gbps)	4 (12.5 Gbps)	16 (16.3 Gbps) + 4 for PS (6 Gbps)	16 (16.3 Gbps) + 4 for PS (6 Gbps)	16 (16.3 Gbps) + 4 for PS (6 Gbps)	20 (16.3 Gbps) + 4 for PS (6 Gbps)	12 (16.3 Gbps)	12 (16.3 Gbps)
Processor	PowerPC 440	Dual ARM Cortex A9	Dual ARM A53 / Dual ARM R5	Dual ARM A53 / Dual ARM R5	Dual ARM A53 / Dual ARM R5		None	None
PS I/O Pins	-	128	214	214	214	214	-	-
HD I/O Pins	640	100	48	48	48	48	96	48
HP I/O Pins	-	150	156	156	156	312	208	156
External Memory Support	DDR2	DDR2,DDR3	DDR4, DDR3	DDR4, DDR3	DDR4, DDR3	DDR4, DDR3	DDR4	DDR4
Notes	For Comparison	For Comparison	Footprint compatible. They are also compatible with the quad ARM A53 equivalent parts.					

- Zynq UltraScale+ ZU4/5/7 selected for carrier
  - Dual or Quad ARM A53 Processors plus dual ARM R5 realtime processors
  - Large range of Logic Cells / Flip Flops
- Artix UltraScale +
  - Cost effective for daughtercard logic
- Silicon lead times from Xilinx have improved significantly of late. We have been able to get prototype quantities in a reasonable amount of time.

CP Carrier Power & Cooling

- Modular power input board developed in support of all equipment that resides in each chassis
- Carrier board receives +/-12 V from power input board
- Remaining components receive power from carrier
  - Cooling fans
  - Daughter cards
  - Signal conditioning cards
- External equipment powered separately
- 48V DC input power via external AC/DC converter for prototype power input board
- Modular power input design allows different input voltages

Common Platform Daughter Card

Daughter / Function Cards

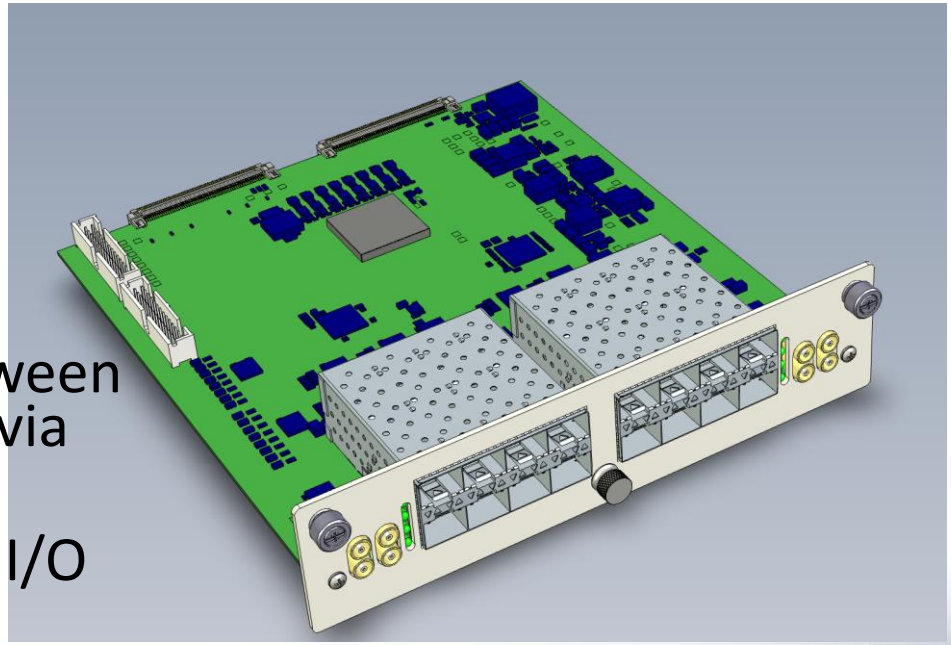
- 7.5 inch width, 8 inch depth
- Both generic and system specific designs
- Examples
  1. Digital I/O - Supporting both discrete I/O and delayed trigger applications
  2. Baseband ADC – 32 Channel, 5 MSPS
  3. Baseband DAC – 16 Channel, 1 MSPS
  4. SFP breakout – 16+ SFPs – ARTIX UltraScale+ based
  5. RF Digitizer, type A (8 ADCs @ 125 MSPS, 2 DACs @ 500 MSPS)
  6. RF Digitizer, type B (4 ADCs @ 125 MSPS, 4 DACs @ 500 MSPS)
  7. BPM Processor – 8 ch / module design under development
  8. Power Supply Controller
     - Potential upgrade path for RHIC WFG/MADC equipment (VME)
     - Considering integration of ALS-U PSC modules for certain systems via SFP interface module

Filter / Signal Conditioning Cards

- Optional add-on
- Provide easy and cheaper means of customization
- Signal Conditioning for generic function cards
- Analog (Baseband ADC & DAC)
  - Filtering
  - Signal Conditioning, Gain, DC Offset, etc.
- Digital I/O
  - Signal buffering
  - Support various I/O standards – TTL, Open drain/collector, dry contact, relay coil, LVDS, ECL, etc.
- Connector options
  - Coax
  - Ribbon connectors to mate with existing installations supported by VME equipment
- Considering stacked board-to-board configuration with daughter card
- Determining dividing line on what circuitry should be located on the signal conditioning card versus the daughter card
  - Ability to customize while minimizing costs tends to favor including certain features on the SigCon card

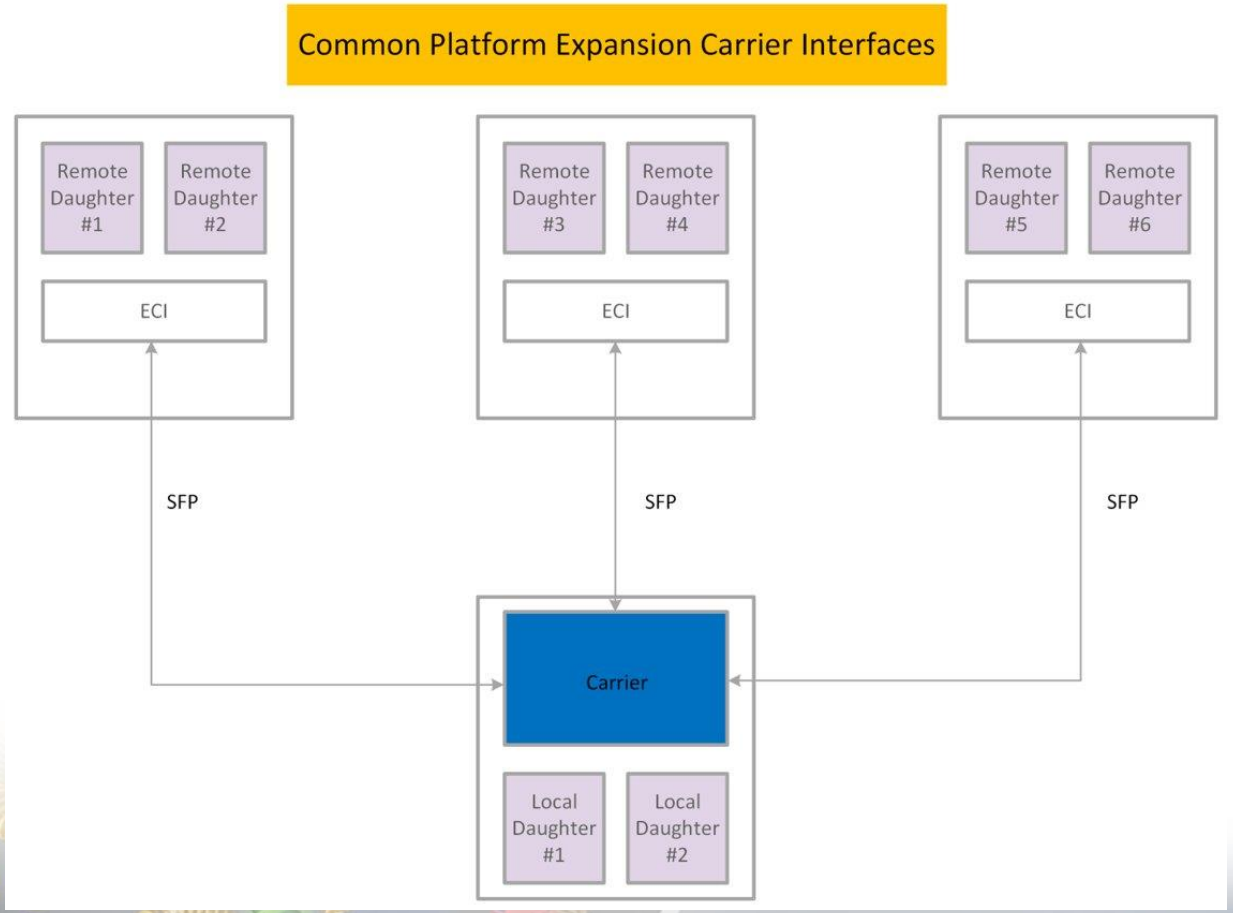
SFP Breakout Daughter Card Example

- Artix Ultrascale+ FPGA
  - 12 GTY transceivers
  - Slave serial or QSPI Flash bitstream configuration
  - FFVB676 package, AU(10,15,20,25)P compatible
- 512Mb QSPI Flash
- 2Kb EEPROM
- 16 SFP+ ports
  - 13 TX/RX, 3 TX only
- Configurable datapaths between Carrier, Daughter, and SFP+ via crosspoint switches
- 8 LEMO bidirectional digital I/O
- 4 Front panel LEDs



Expansion Carrier Interface

Expansion Carrier Interface Concept

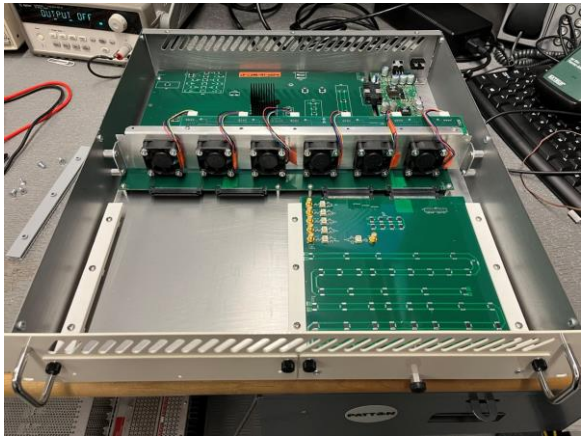


- Support 1 - 2 daughter cards per ECI board
- Support external clock generated by carrier board
- Eventually add support for clock-recovery
- Cost savings by skipping on-board FPGA
- Utilize SFP connections for comm to carrier
- Power feed similar to carrier board
- Allows for higher I/O density in less performance-driven cases

Common Platform Chassis

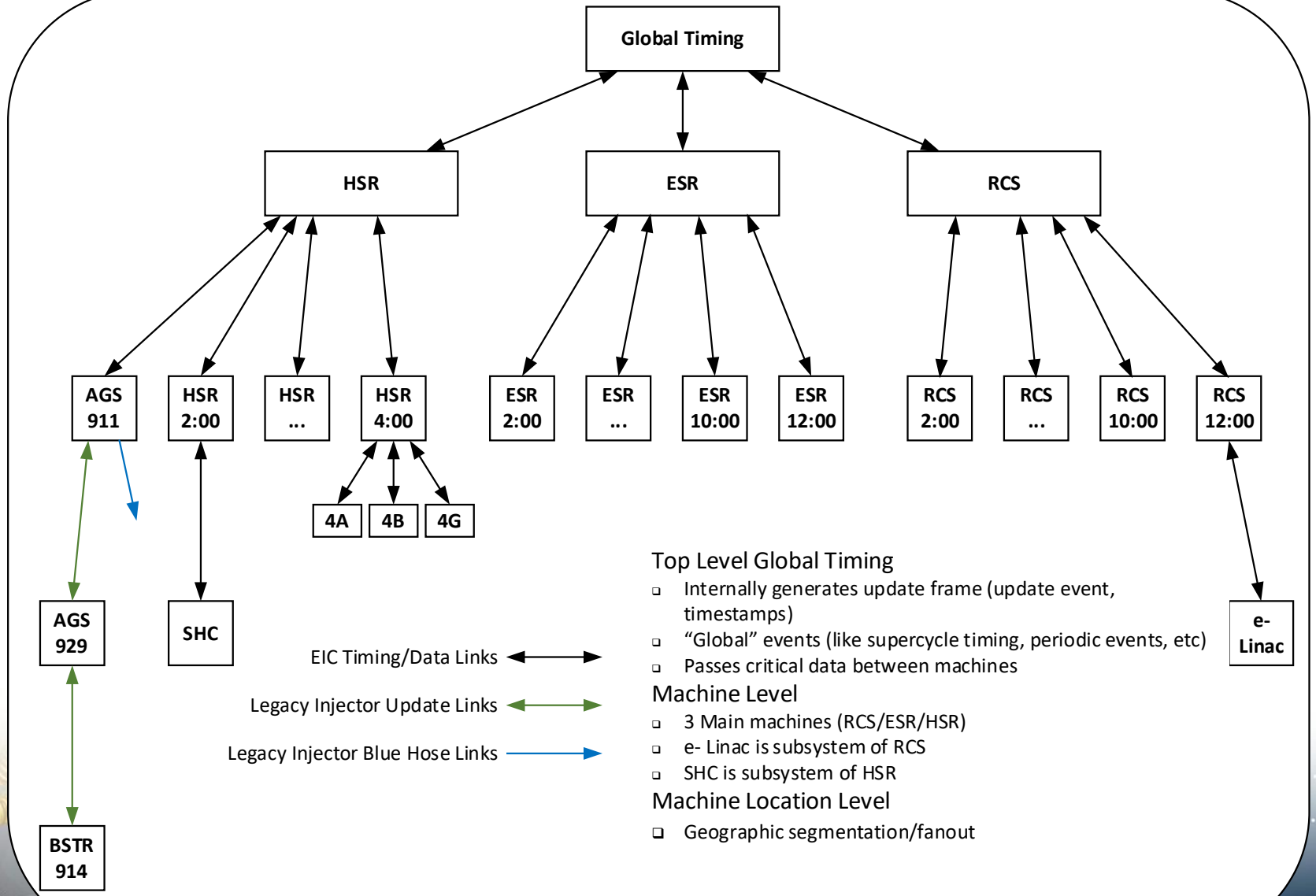
Mockup Chassis Status

- Currently lab testing a mockup chassis with simulated heat dissipation
  - Carrier board
  - Daughter cards
  - Standard PSU
- Measuring chassis air flow
- Working on comparisons against temperature and air flow models to help determine optimal configuration



Timing System Interconnects

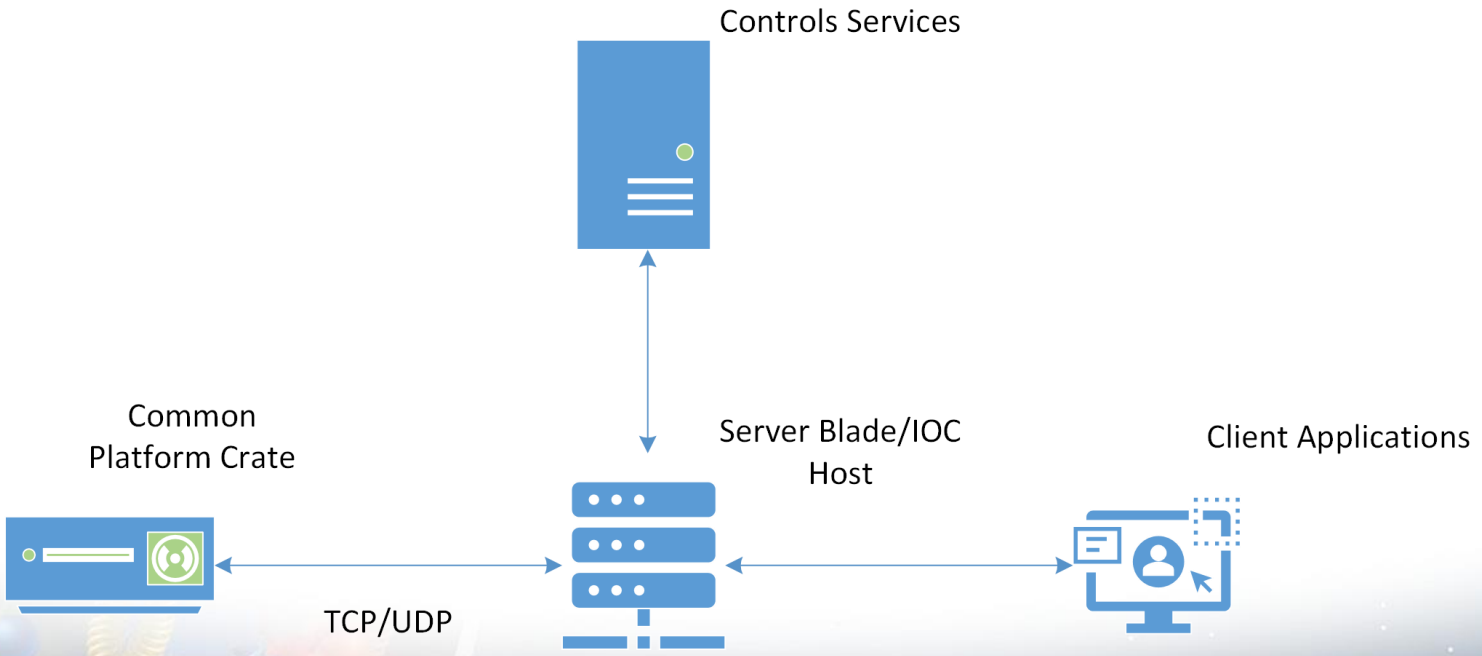
Timing System Conceptual Layout



Front End Computer Remote Interface

FEC Remote Interface Diagram

Common Platform Interface



FEC Remote Interface

- Evaluating use of FreeRTOS on the Front End Computer
  - Well supported, though there are newer options
  - Avoids licensing concerns
  - Need to confirm performance
- Use of Linux is also under consideration
- The initial plan is to host IOCs remotely, though we will also consider local hosting capabilities
  - Is remote hosting the more common option in the EPICS community?
  - CAD ADO system is generally handled via local hosting, which has led to performance bottlenecks in higher volume client data / client count situations, and solutions involving "reflective" processes running on more capable servers
- Starting out using development tools that were created at DESY for their LLRF system
- Our plan is to develop a generic remote interface protocol for integrating the FEC with the remote interface running on a separate host
  - Will support EPICS PVaccess protocol
  - Will support CAD ADOs protocol for off-project application at least
  - Aim is to develop a standard communication library that could be used with any CP application

Overall Status and Plans

- Currently finalizing PCB routing of initial prototypes
  - Carrier board
  - SFP breakout daughter
- Baseband ADC daughter card is under design
- Support is being provided via MOU from C-AD and NSLS-II at BNL
  - Our JLab partners are also responsible for EIC project scope, and will be contributing to the daughter card development efforts
- Timing Data Link details
  - Considering development of delay compensation for timing distribution to meet performance requirements of critical systems
  - Improved GTH receiver locking procedure over current LLRF implementation
- Machine Protection System
  - Design work is needed, but we intend to distribute a separate MPS fiber link as needed around the EIC Complex in a similar topology to the TDL
- Working on developing the communication protocol between Front End and remote interface IOC/ADO processes
- Need to consider AI/ML implications on CP design
  - Local storage and processing/tagging of data in special cases, when higher performance is required?

Thanks to...

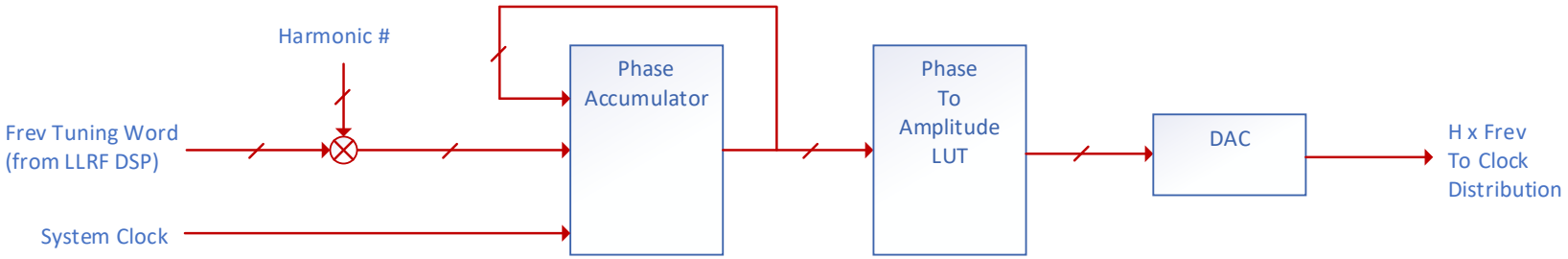
Tom Hayes, Kevin Mernick, Freddy Severino, Geetha Narayan, Paul Bachek, Rob Hulsart (BNL/CAD)

Joe Mead (BNL/NSLS-II)

Any Questions?

Backup Slides

Beam Sync Timing Generation



Existing VME Boards

Name	Functionality	Operational
V102	Delay Module	147
V108	Utility Module	484
V113	MADC controller	142
V114	A to D module	140
V115	Waveform generator	592
V120	RHIC permit module	48
V124	Beam sync trigger module	70
V194	Pulse fanout	59
V202	Delay module	158
V233	QFG	71
V294	General I/O module	29
VMIVME-1160A	Digital input	69
VMIVME-2170A	Digital output	111
VMIVME 3122	64 ch, 16bit analog input (100kHz max)	82
VMIVME 3123	16 ch, 16 bit analog input	14
VMIVME 4122	8 ch, 12 bit analog output	37
VMIVME 4140	16 or 32 ch, 12bit analog output	35
VTR2535	8ch, 12bit, 10MSPS A/D	4
VTR2537	8ch, 12bit, 1MSPS A/D	8
VX-2	Motion controller	38

RHIC Beamsync Info

- Separate Blue/Yellow generator boards and associated timing links, each using RF rev tick
- Distributed on fiber/copper cables ("blue hose"), separate from other primary connections (ex. RHIC event link)
- VME V124 modules decode one beamsync link and provide beam-synchronous timing with delay control capabilities
  - Originally designed for 360 bucket operations, with harmonic adjustment added in later
  - 8 output channels per board
  - Differential ECL signal output
  - Jitter is ~ 8 ps
- The hope is that the Common Platform equivalent trigger outputs will have smaller jitter with the newer generation of FPGAs