areaDetector Challenges and Perspectives for Sirius High-Throughput Detectors

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LNLS sirius
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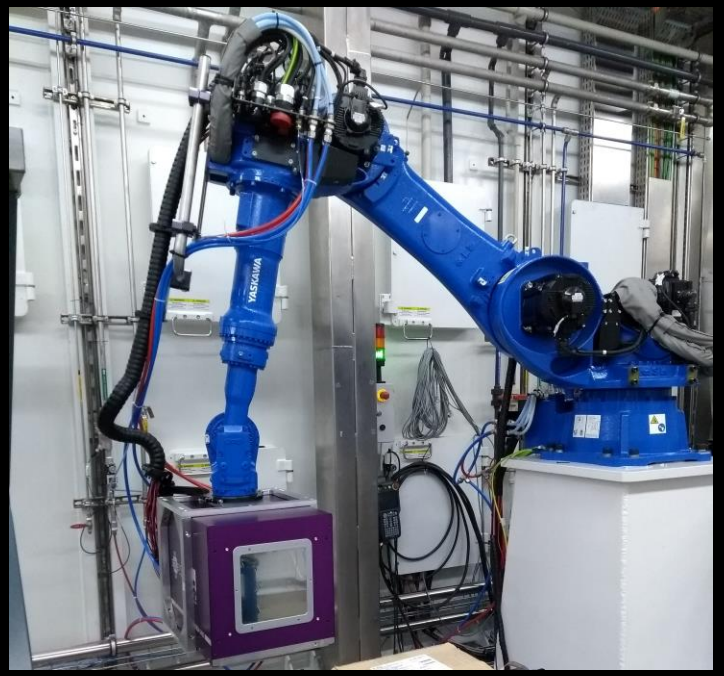
Brazilian Center for Research in Energy and Materials

What we have/What we want

- In-house detector development currently deployed at 5 beamlines
- Control software architecture integrated with EPICS
- Detector data acquisition architecture partially/completely integrated with EPICS

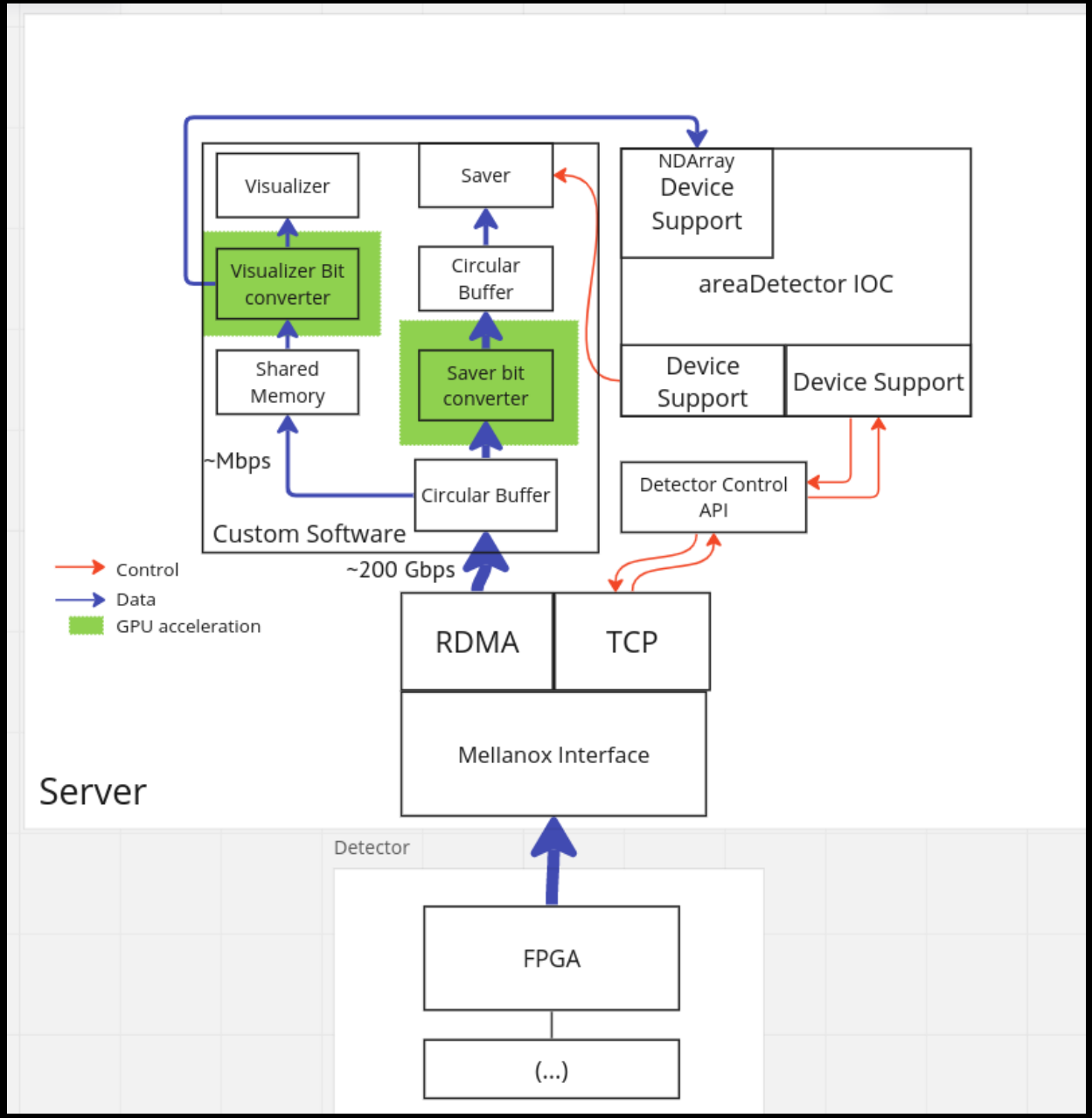


			Timepix3 (2013)	Timepix4 (2019)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s
TOT energy resolution			< 2KeV	**< 1Kev**
TOA binning resolution			1.56ns	**195ps**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**
Target global minimum threshold			<500 e^- Detector	<500 e^-

- Current implementations deal with 210 Gbps
- Future detectors can require up to ~1.8 Tbps

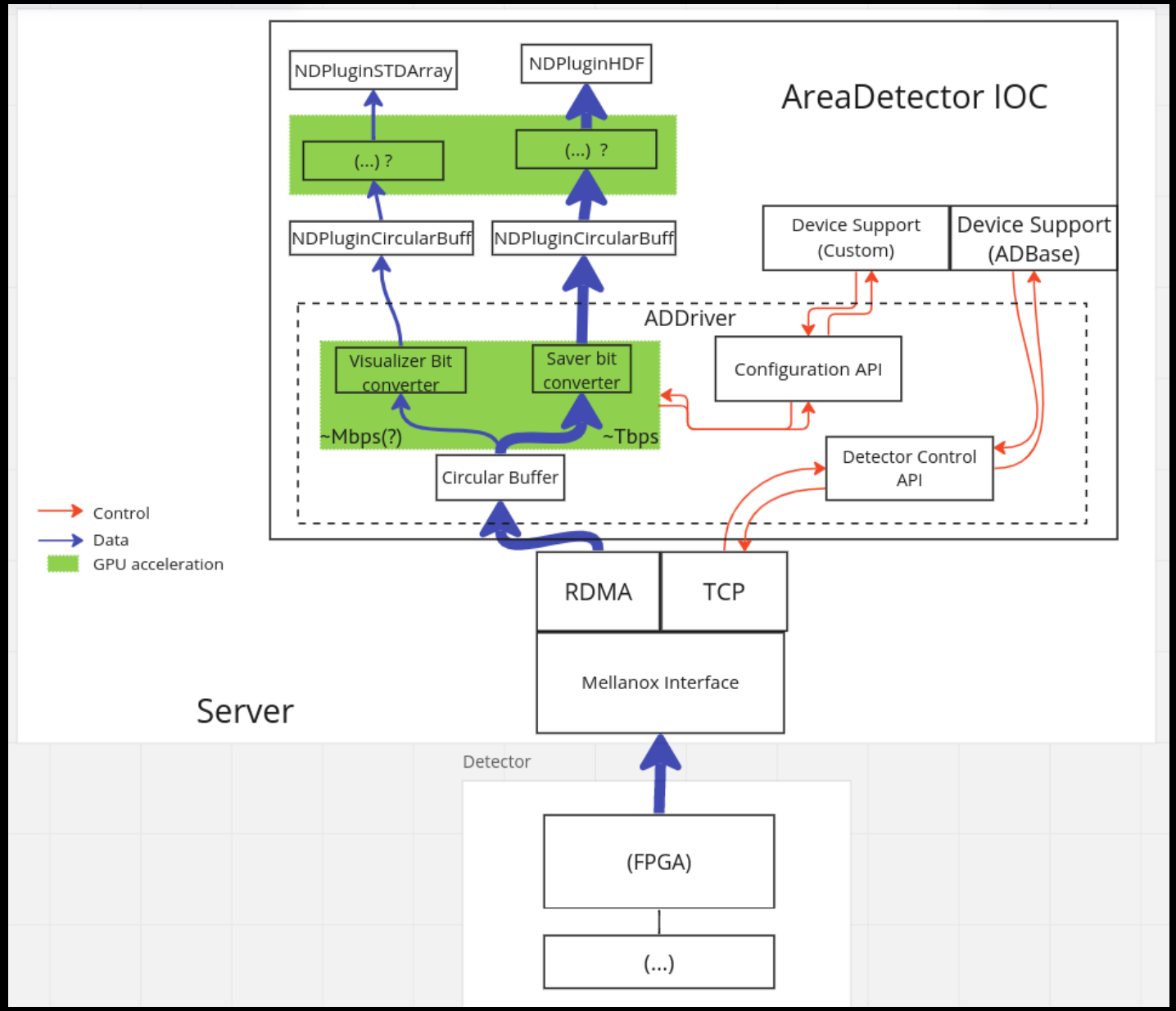
What we have

- Software architecture decoupled from areaDetector
- Data pipeline is defined at compile time
- No customizable metadata
- Implementation not modularized (monolithic)
- Can choose between with/without hardware acceleration (GPUs)



What we want

- Use areaDetector resources as much as possible
- Reconfigurable data pipeline
- Customizable metadata, ROIs, etc.
- Modularized implementation
- Integrated hardware acceleration



Final questions:

1. Does the proposed architecture make proper use of areaDetector or are we abusing it? Is it meant for high-throughput?

2. Hardware acceleration options: should we develop new plugins/drivers or extend existing ones?

3. Are there plugins/drivers that already use hardware acceleration?

4. Are there ongoing efforts to develop such hardware acceleration capabilities? If yes, how could we team up on this?

Thanks!

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