DUNE FD2 PDS HV Impact Mitigation

Last Update: 03 April 2023
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Revision Change Log

Date of Revision	Revision PoC	Revision Notes
03-Apr-2023	Ryan A. Rivera	Incorporated minor feedback from PDS Consortium
24-Mar-2023	Ryan A. Rivera	Included more details on BNL balun study
15-Mar-2023	Ryan A. Rivera	Initial draft for FD2 PDS Final Design Review

Introduction

This document describes the DUNE Far Detector 2 (FD2) Photon Detector System (PDS) plans and methods for mitigation of the threat for component damage due to electrical discharge from the operation of the high-voltage (HV) subsystem. The understanding is that discharges of the FD2 HV subsystem will happen, the discharges will impact the FD2 PDS, and the impact can be minimized. This document will be updated throughout the FD2 PDS production phase if interfaces and constraints are modified.

The FD2 PDS consists of cold photo-collectors known as X-ARAPUCA (XA) on the cryostat membrane and cathode, and the supporting infrastructure for operation, readout, and control.

There are four primary subsystems comprising the FD2 PDS:

1. Warm Electronics
2. Membrane-mounted photon detector
3. Cathode-mounted photon detector
4. Response Monitoring System (RMS) fibers and diffusers

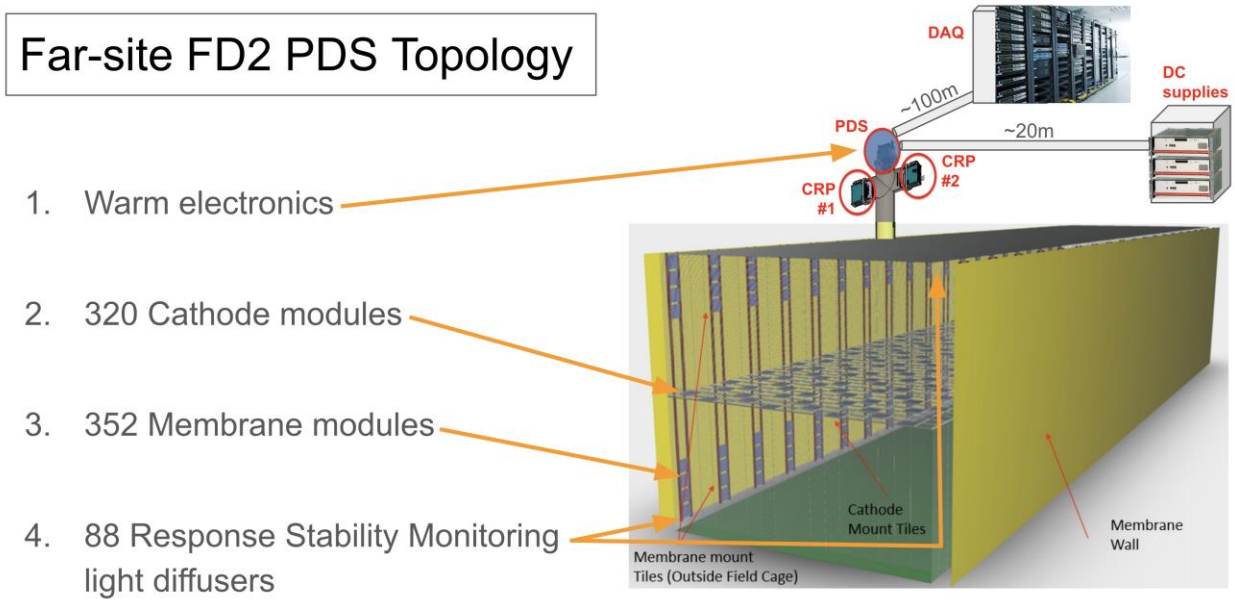

Figure 1. DUNE FD2 PDS topology at SURF.

The FD2 HV subsystem consists of a HV feedthrough and extender which supply -300kV to the cathode and then to the field cage profiles through parallel resistor arrays. The field cage resistor arrays linearly step the voltage down at each field cage profile from -300kV at the cathode, in increments of 2kV, to cryostat ground potential at the top and bottom anode.

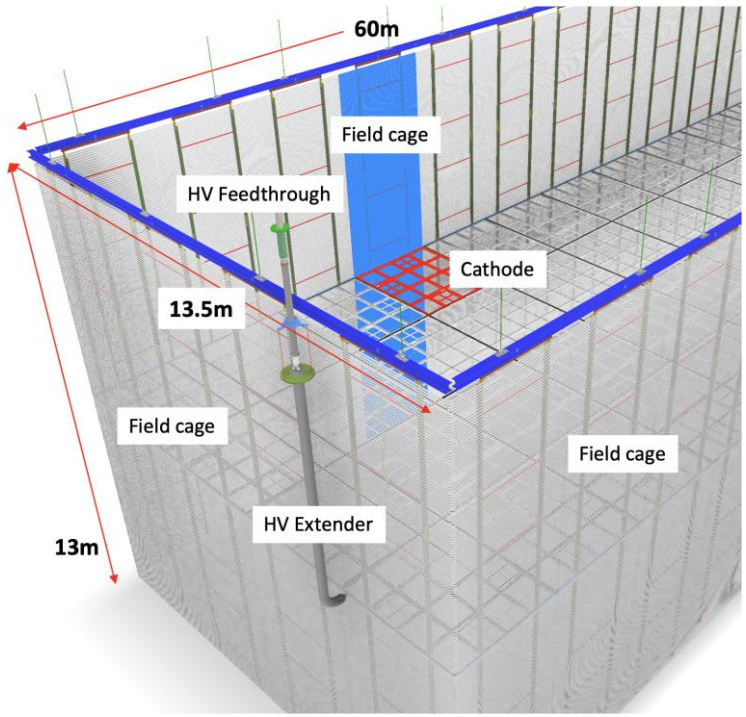

Figure 2. DUNE FD2 HV topology at SURF.

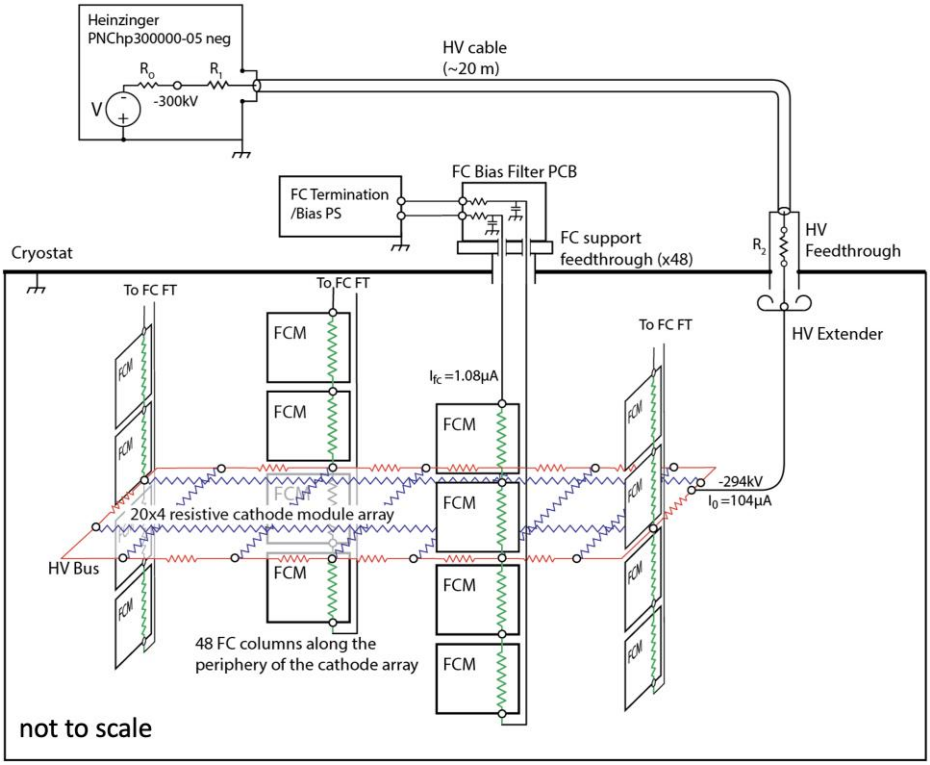

Figure 3. DUNE FD2 HV schematic diagram.

Risk of HV Impact

Any high potential difference system can breakdown, creating a sudden low resistance current path, and discharge. Reducing the potential differences, and controlling the discharge paths, are the primary mitigation approaches to minimize the impact of discharges. The DUNE FD2 HV system is designed to operate the cathode at -300kV potential difference relative to the top and bottom anode, and relative to the cryostat membrane. Discharges can occur anywhere in the system where enough charge builds up, and a low enough resistance discharge path exists (i.e. conductive or resistive paths), or is formed (e.g. bubbles or impurities in the LAr). The Membrane-mounted XA primary discharge risk is from charging up non-conductive surfaces, counteracting the electric field generated by the local field cage profiles. The Cathode-mounted XA primary discharge risk is from catastrophic HV system discharge events dropping the cathode voltage from -300kV to cryostat ground over a timescale of 10ns. The FD2 PDS RMS system is at low risk for discharge impact as it is run in conductive conduit along the cryostat membrane.

Physical separation of potential differences is the best way to reduce electric field magnitudes and minimize the impact of a discharge. The distance from cathode to bottom and top anode is greater than 6m. Critically, however, the distance from the cathode to the cryostat membrane wall, and the distance from the HV feedthrough and extender to the cryostat membrane wall, is less than 1m. Thus, the highest risk of HV system discharge is from the cathode and HV feedthrough/extender to the cryostat membrane.

It is anticipated that the HV system will, inevitably, discharge during the lifetime of the DUNE experiment, and so it is a requirement for all subsystems to survive a HV discharge event. In the case of the FD2 PDS, there are three subsystems that must survive a HV discharge event: Membrane-mounted XA, Cathode-mounted XA, and the RMS.

Modeling of HV Discharge Event

The approach taken to mitigate, and ultimately survive, the eventuality of a HV discharge event was, first, to use simulations to understand the severity of the voltage, current, and charge impact on the FD2 PDS elements. Two independent simulation studies were launched, one at Brookhaven National Laboratory (BNL: Sergio Rescia, Veljko Radeka, Bo Yu, Hucheng Chen, et. al.) and one at Fermi National Accelerator Laboratory (FNAL: Paul Rubinov, Sergey Los, et. al.); the two studies started from the same assumptions, and then diverged with the approach taken and analysis tools used (i.e. BNL used Spice, and FNAL used Ansys). It is acknowledged that the modeling problem is challenging due to the large scale (60m x 13m), the large quantity of elements of the system, and the complex topology of the X-ARAPUCA relevant details (i.e. distributed SiPMs, bias voltage, supply voltage, and signals). The conclusions from both simulations agreed to an order of magnitude. Thresholds were then developed for survival based on the more pessimistic of the two, and then grounding and shielding solutions were devised to meet the thresholds.

Parameters and Timeline

The parameters and timeline of a worst-case HV system discharge are defined as follows:

- Steady state: The HV distribution system operates the 60m x 13.5m cathode at -300kV, relative to the two anodes and cryostat membrane; the anodes are electrically tied to the cathode 6.5m away by a gradient field cage, and the system stores 270 Joules of energy.
- Timescale 0-10ns: A single point on the field cage or HV bus/extender/feedthrough discharges from -300kV to zero, creating a large local potential difference impacting the local Cathode-mounted XA.
- Timescale 10ns-100ns: Capacitive coupling induces a large spike of charge and then current, which then rushes off the cathode, impacting the entire cathode and all Cathode-mounted XA.
- Timescale 10ns-100ms: Transients propagate and settle diffusively throughout the entire HV system.

Capacitance Matrix

From the same steady state initial conditions, both the BNL and FNAL teams arrived, independently, at the same capacitive coupling matrix among field cage, cathode, and anode elements.

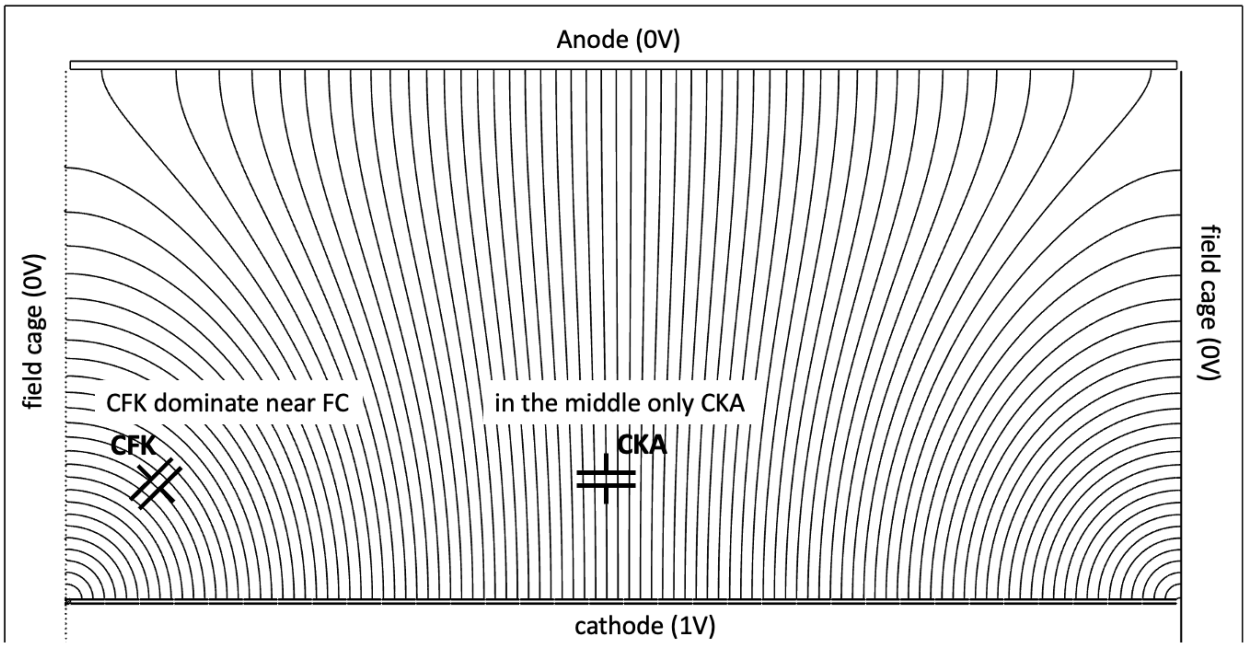

Figure 4. Illustration of capacitive coupling from BNL (S. Rescia, et. al.) simulation.

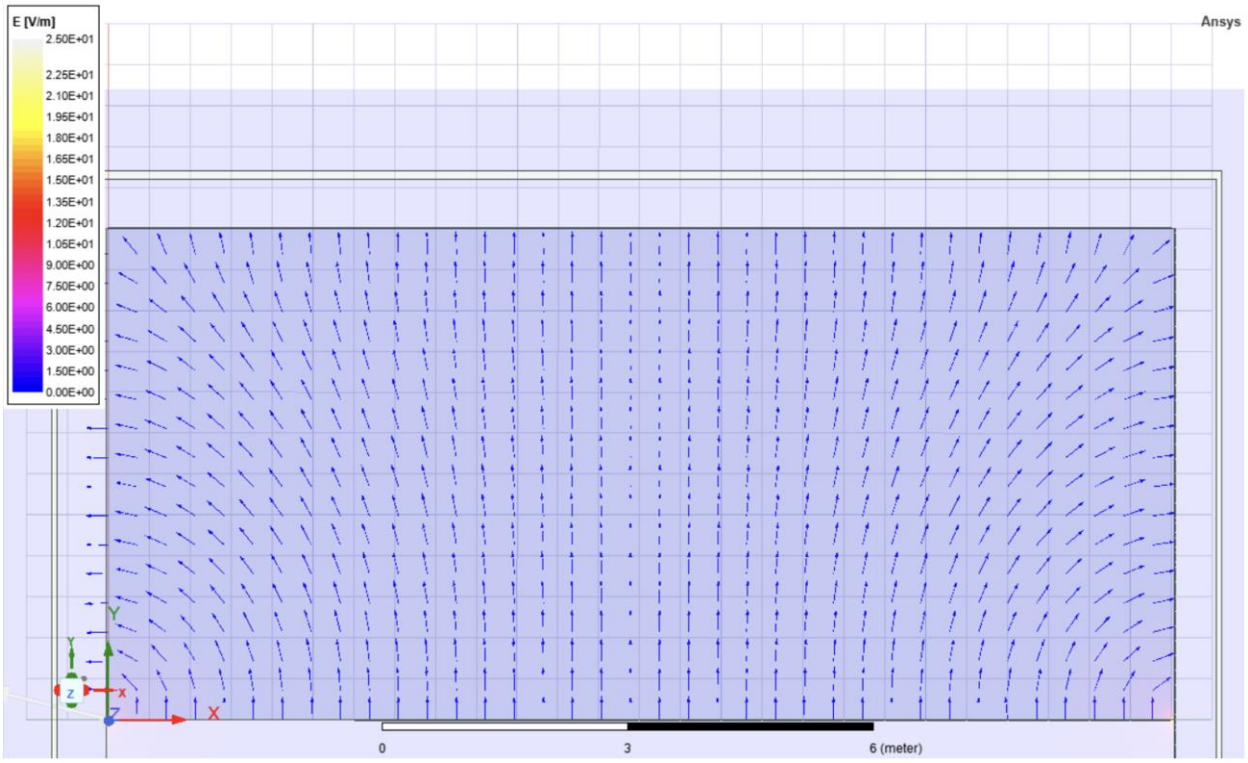

Figure 5. Plot of capacitive coupling matrix from FNAL (P. Rubinov, et. al.) simulation.

Induced Potential Difference

From the parameters of a discharge provided by the HV team, both the BNL and FNAL teams arrived, independently, at the same result for the induced potential difference on the cathode from the -300kV discharge event. The results showed that the largest impact is on XAs near the point-of-discharge, and the greatest magnitude potential difference from one XA to another XA reaches 100kV. The derivation of induced potential at any location on the cathode is a capacitive divider, from which charge and current can follow, with a fit to the function.

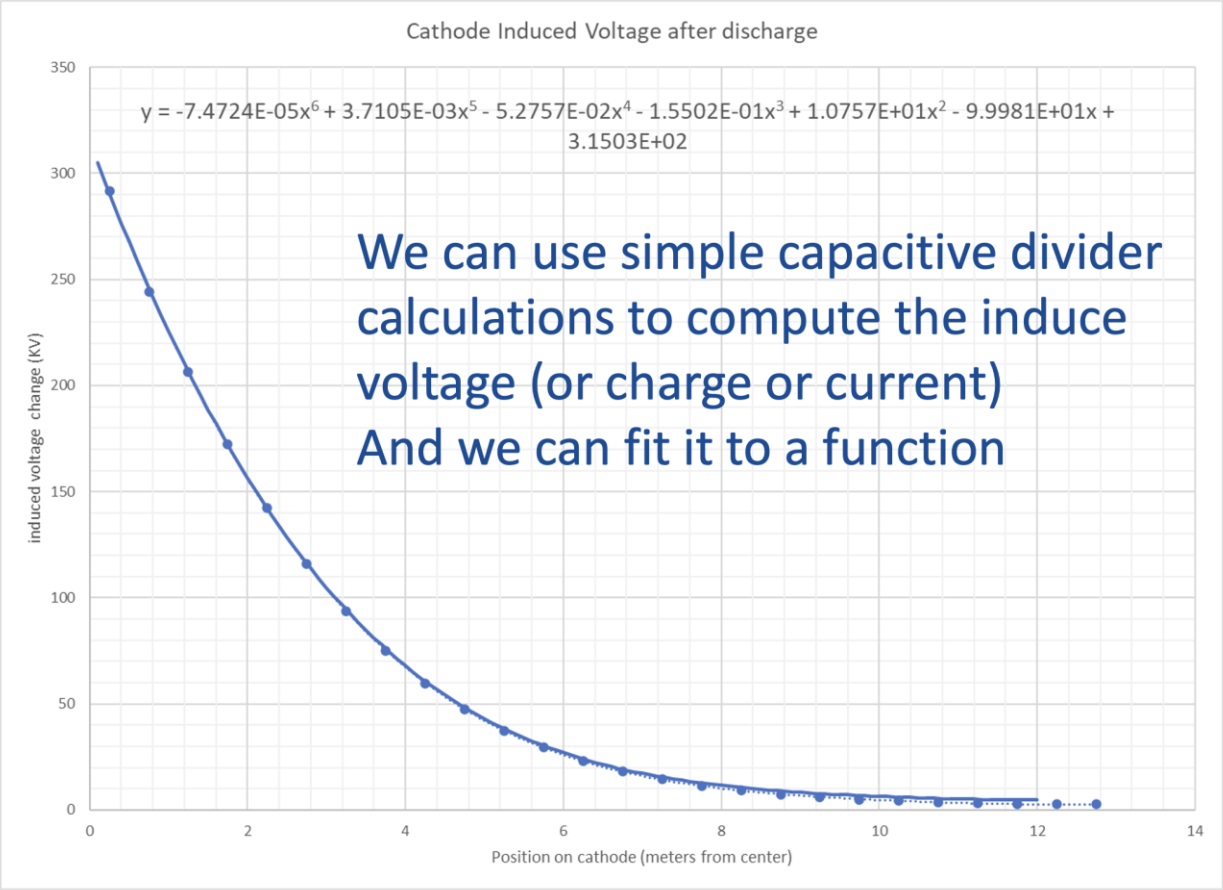

Figure 6. Fit of induced potential calculation on cathode after a HV discharge event from FNAL (P. Rubinov, et. al.).

Using the capacitive coupling matrix, 2-dimensional and 3-dimensional timelapse modeling studies of a HV discharge event could be generated to help visualize, and qualitatively comprehend, the magnitude of the induced voltage.

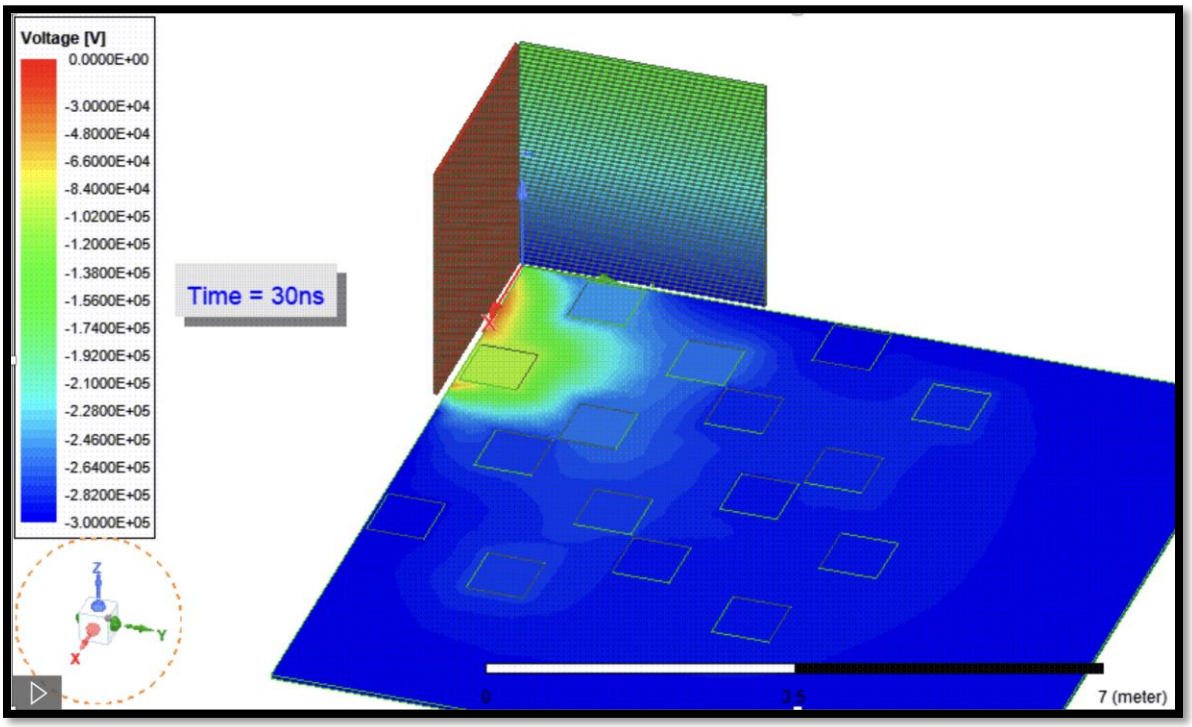

Figure 7. High voltage breakdown 3-dimensional time study, from FNAL (P. Rubinov, et. al.) for a discharge from the field cage column relative to cryostat ground potential.

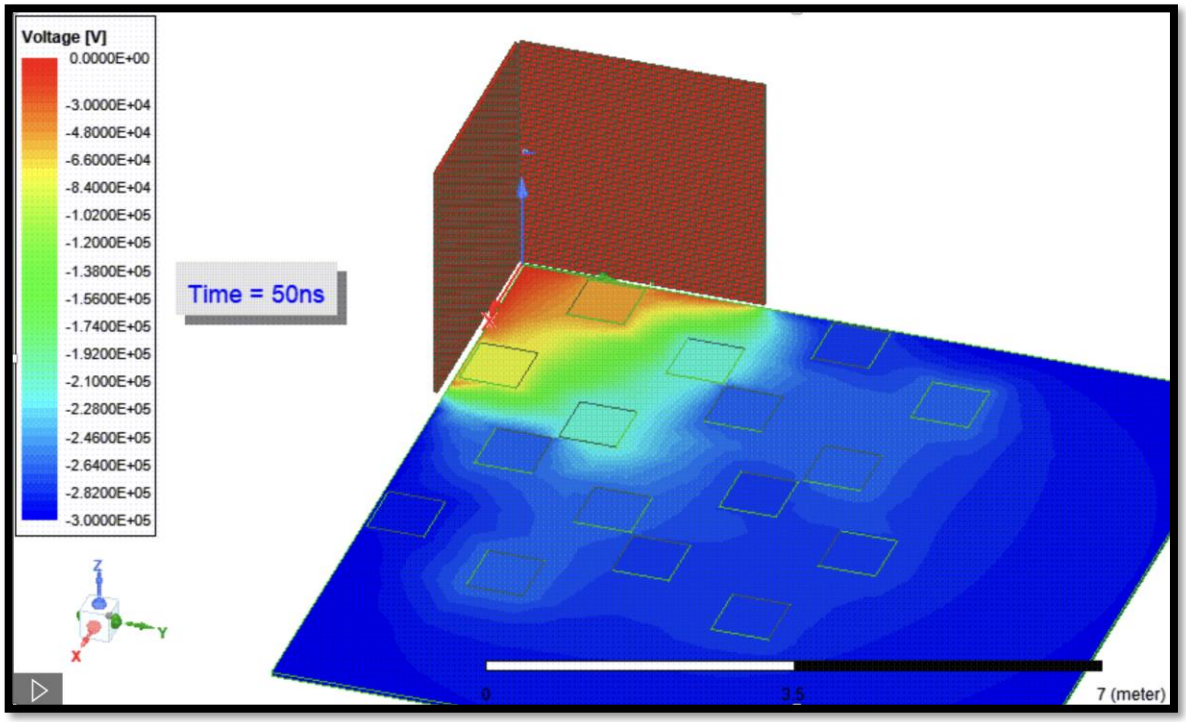

Figure 8. High voltage breakdown 3-dimensional time study, from FNAL (P. Rubinov, et. al.) for a discharge from the field cage corner relative to cryostat ground potential.

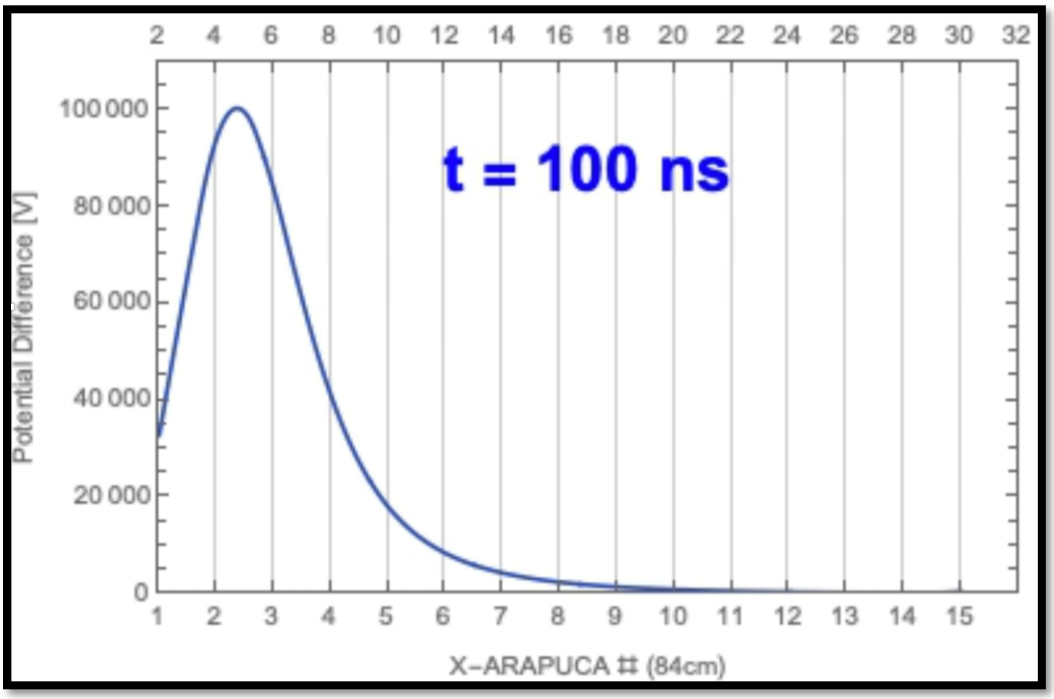

Figure 9. High voltage breakdown 2-dimensional time study from BNL (S. Rescia, et. al.), for a discharge from a single point on the field cage, showing the potential difference across a Cathode-mounted XA, where XA #1 is closest to the point-of-discharge and XA #16 is furthest at the opposite field cage column.

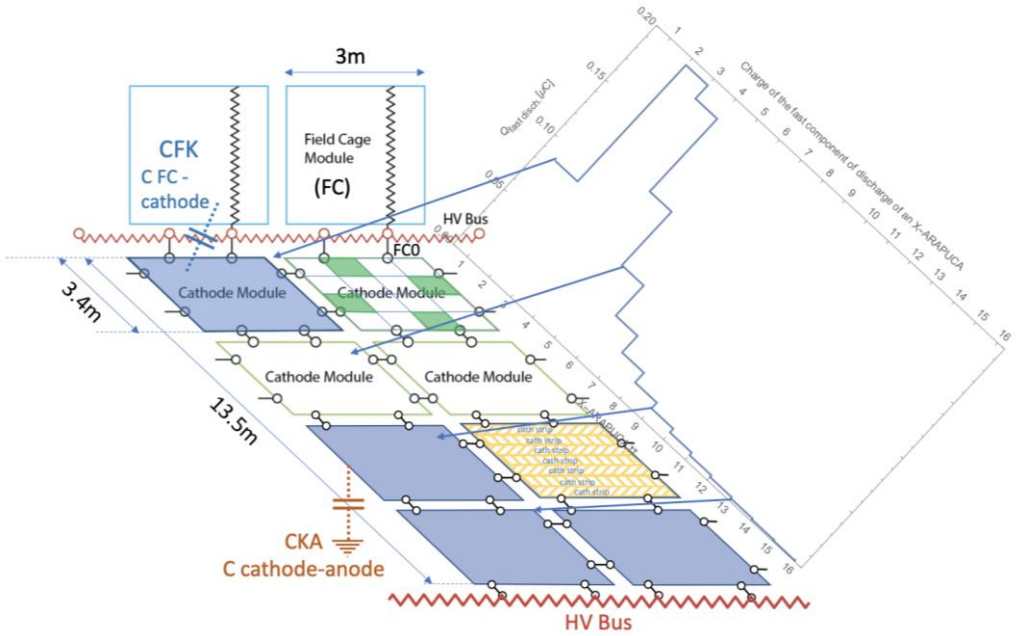

Figure 10. Study showing the mapping of the capacitively induced charge distributed over the XA on the cathode from BNL (S. Rescia, et. al). The peak charge induced at an XA is 0.2 µC.

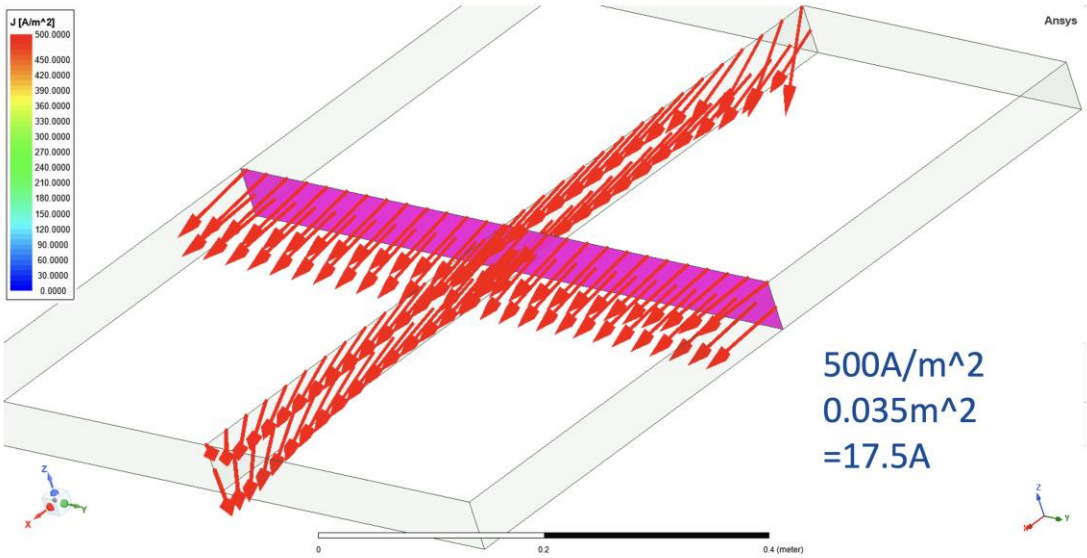

Figure 11. Visualization, from FNAL (P. Rubinov, et. al.) of the induced current over the X-ARAPUCA, through the cathode mesh, during a discharge event.

Induced Charge

The simple worst-case calculation of charge induced is to consider 1m from the field cage, approximately representing one XA, where the capacitance coupled to the cathode is 50pF/m. The gradient at that 1m point is 100kV/m, in the worst-case – thus, the XAs near the field cage experience 50kV potential difference, worst-case. This implies a worst-case induced charge at an XA of (50kV * 25pF) which is 1.25µC. 1.25µC maps to an induced current spike (10ns) of 125A over the area of an XA. The induced charge is then dissipated diffusively throughout the cathode over 100ms.

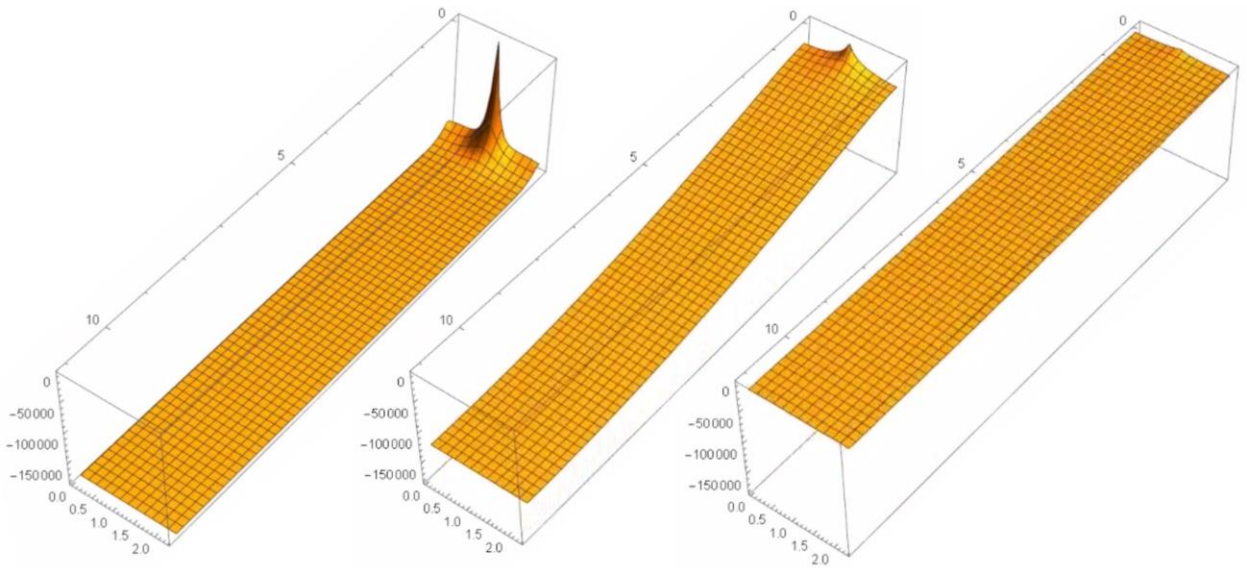

Figure 12. Time-lapse visualization from BNL (S. Rescia, et. al.) of diffuse dissipation of disharge event throughout the cathode.

Modeling of XA Non-conductive Surfaces

In addition to the HV cathode discharge impact studies, the effects of charging up non-conductive surfaces of the Membrane-mounted XA, in the steady state of HV system operation, was modeled. BNL (B. Yu, et. al.) conducted a 3-dimensional finite element analysis (FEA), which represented a quadrant of an XA as 325mm x 50mm at 70cm from the field cage at -150kV. Revealed in this study was, if no mitigation were applied, the XA surface is anticipated to charge up to -62kV to counteract the local electric field generated by the field cage and the cryostat membrane potential difference. In response to this understanding, several permutations of mitigation approaches (i.e. applying conductive mesh over the PD surface) were modeled.

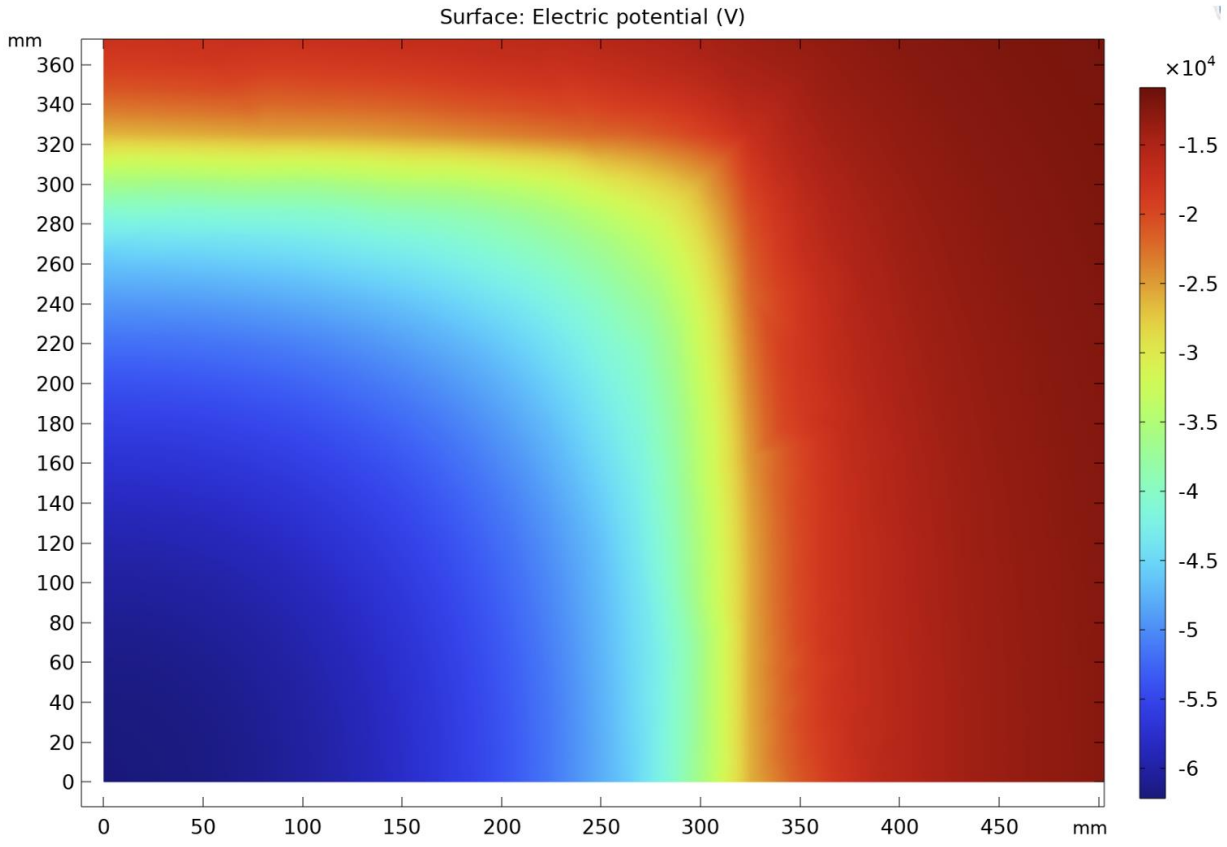

Figure 13. FEA of the PD surface with no conductive elements showing a max potential of -62kV.

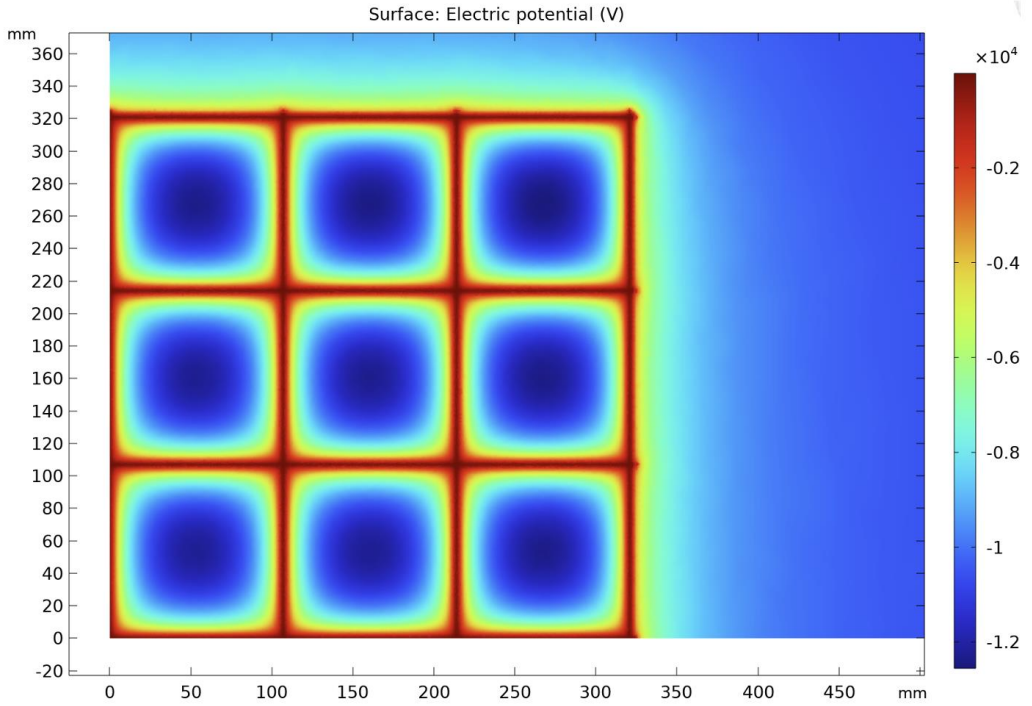

Figure 14. FEA of the PD surface with 2mm conductive wire in 10cm x 10cm grid showing a max potential of -12.5kV, with electric field on the wire surface of 31kV/cm.

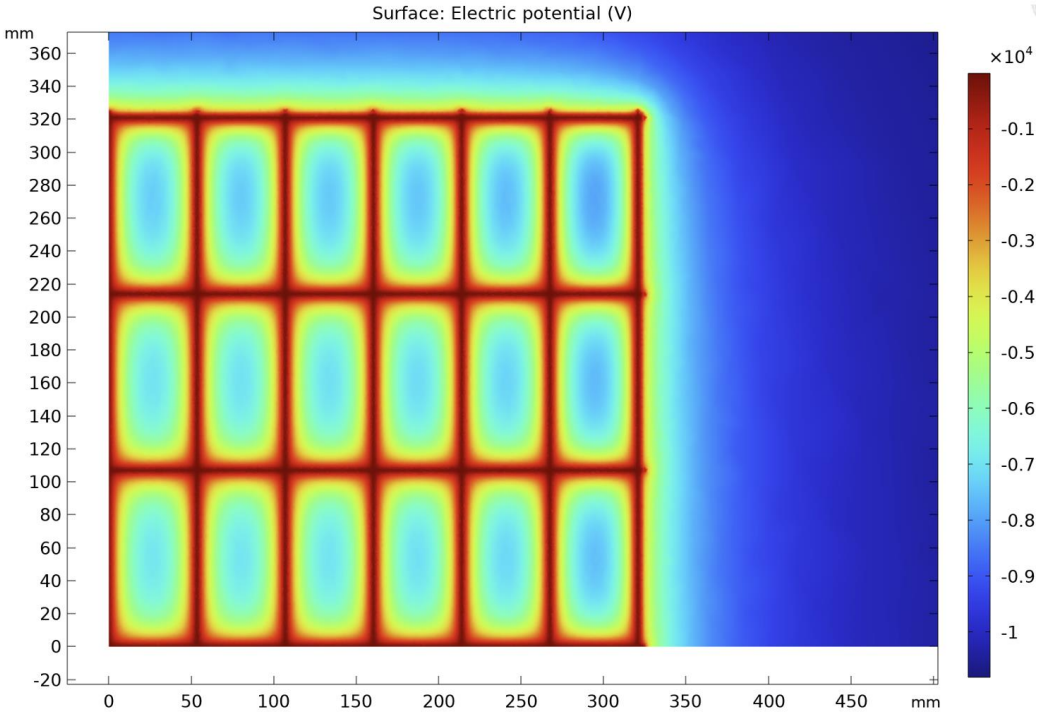

Figure 15. FEA of the PD surface with 2mm conductive wire in 5cm x 10cm grid showing a max potential of -7.9kV, with electric field on the wire surface of 27kV/cm.

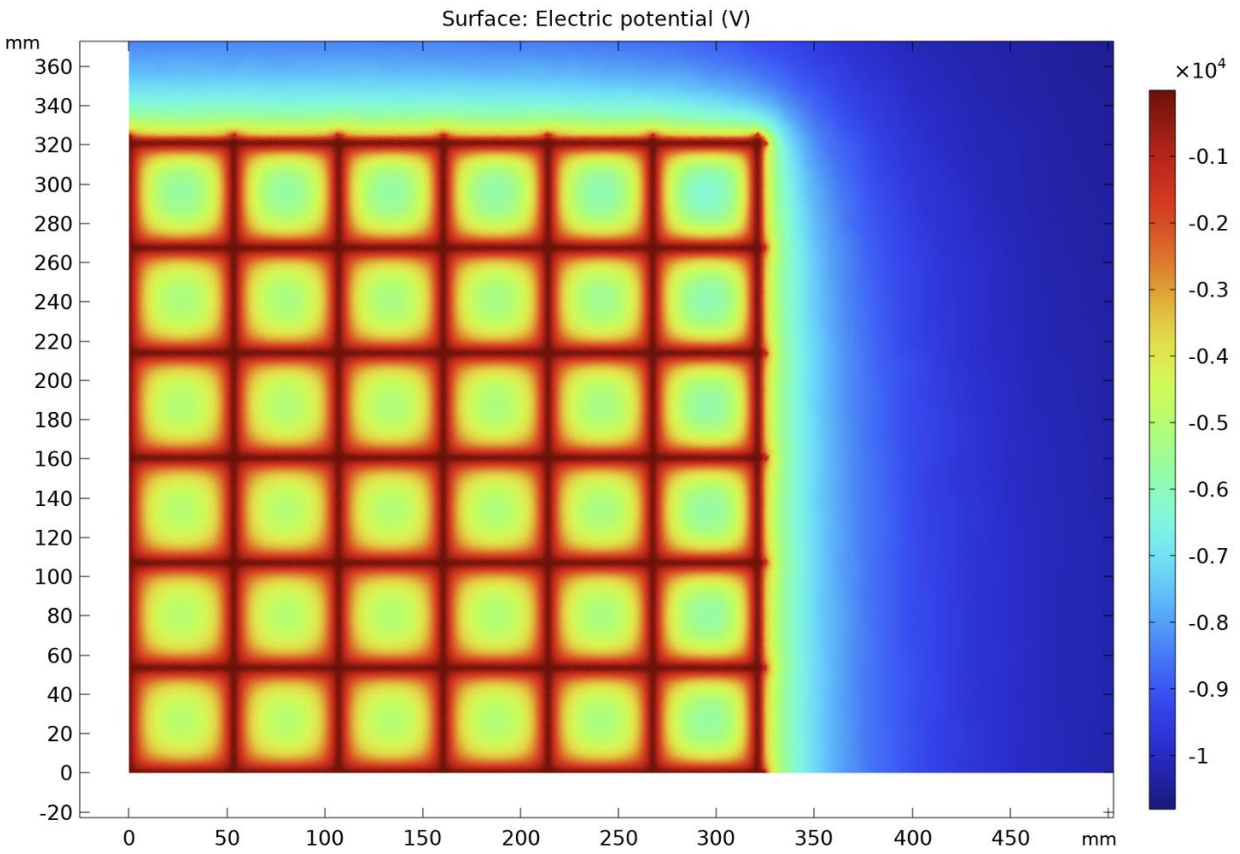

Figure 16. FEA of the PD surface with 2mm conductive wire in 5cm x 5cm grid showing a max potential of -6.3kV, with electric field on the wire surface of 24kV/cm.

At the conclusion of this study, led by BNL (B. Yu, et. al.), acceptable operating thresholds for Membrane-mounted XA were set at -7kV for max potential on the surface of the XA, and 25kV/cm electric field max on a 2mm diameter wire surface. These thresholds were set based on the cathode wire mesh studies, from the HV team, which concluded 10kV/cm electric field was acceptable on a wire mesh of 0.3mm and 3.81cm pitch.

The FD2 PDS RMS system is anticipated to avoid charge up issues by deploying a conductive conduit and routing only along surfaces referenced to cryostat ground potential.

FD2 PDS HV Impact Mitigation

In response to the understanding of the impact of the HV system, developed from the series of studies from BNL and FNAL, mitigation strategies were developed for the FD2 PDS Membrane-mounted XA and Cathode-mounted XA.

SiPM and Readout Electronics Discharge Mitigation

The first mitigation strategy is common to both the Membrane-mount and Cathode-mount XA. Conductive shielding protecting the readout electronics and SiPM signal path were designed. The concept is to provide a conductive path for discharge events away from the sensitive electronics. The readout electronics protection was designed as a fully enclosed conductive box. The SiPM signal cables are two conductors with a shield. The SiPM carrier circuit board required the most attention because the SiPMs cannot be fully enclosed without losing photo detection efficiency.

To optimize the SiPM shielding approach, a study was conducted by BNL (B. Yu, et. al.). A 2-dimensional model was created of a Cathode-mounted XA, as a worst case, with two SiPM circuit boards represented 70cm apart. The left "SiPM_L" circuit board was modeled near the field cage, and the right "SiPM_R" circuit board was modeled near a representation of the resistive cathode mesh.

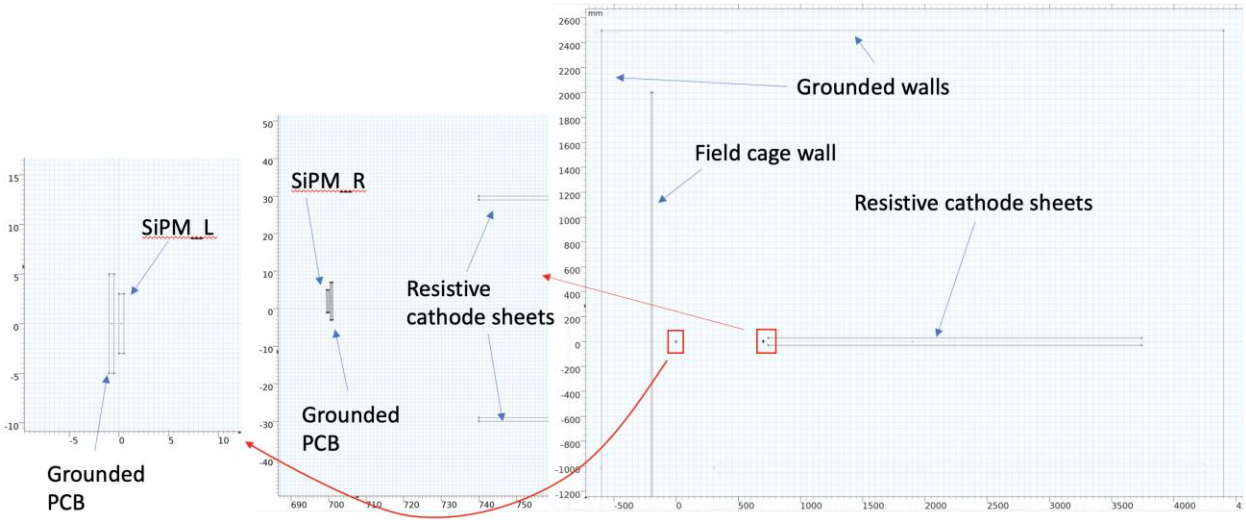

Figure 17. SiPM shielding optimization study done by BNL (B. Yu, et. al.) of a 2-dimensional representation of SiPM circuit boards.

If no SiPM shielding were applied, the BNL study showed that the SiPM circuit board would experience a charge injection of 1.2uC to the left circuit board, assuming a 300kV swing at the field cage, and 0.5uC of charge to the right, assuming a 100kV swing on the cathode.

Maxwell capacitance (F/m)				
	FC	SiPM_L	SiPM_R	Cathode
FC	2.13E-10	-4.03E-12	-8.86E-13	-1.75E-11
SiPM_L	-4.03E-12	2.08E-10	-5.30E-14	-5.92E-13
SiPM_R	-8.86E-13	-5.30E-14	2.09E-10	-4.87E-12
Cathode	-1.75E-11	-5.92E-13	-4.87E-12	9.04E-11

Figure 18. The capacitance matrix for the SiPM circuit board charge injection, due to discharge with no shielding, which results in 1.2µC and 0.5µC injected at the SiPM circuit boards.

Adding the conductive cathode wire mesh, above and below the SiPMs, was the next step in the modeling process, and a dramatic improvement was shown in the simulation - reducing the injected charge to 64nC and 81nC for the left and right SiPM circuit boards respectively.

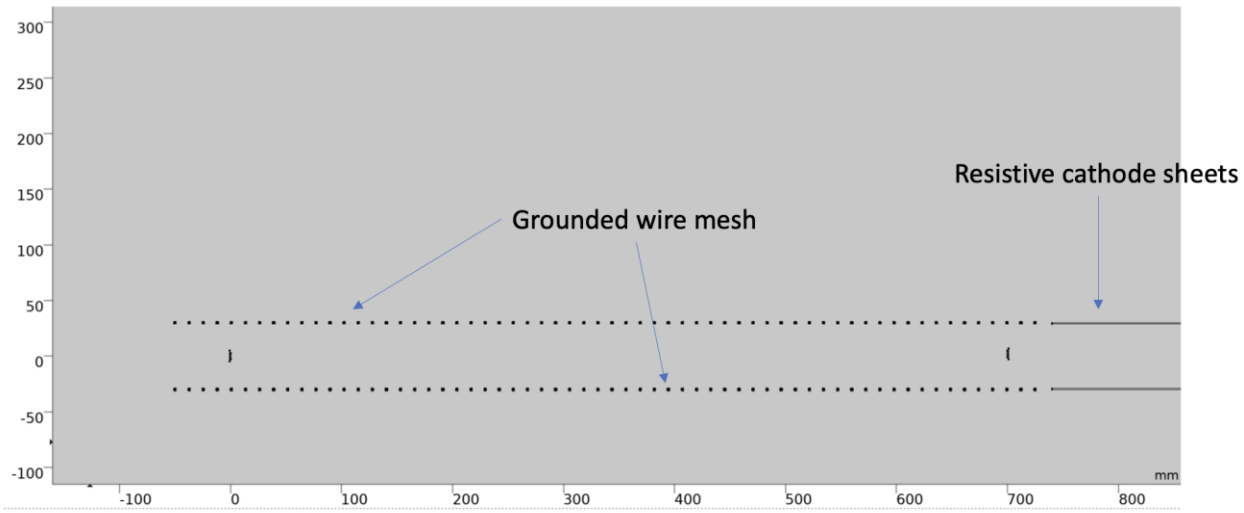

Figure 19. SiPM shielding optimization study considering the impact of the cathode conductive wire mesh of 0.6mm wire diameter and 12.7mm pitch.

Maxwell capacitance (F/m)				
	FC	SiPM_L	SiPM_R	Cathode
FC	2.34E-10	-2.13E-13	-1.93E-14	-1.05E-11
SiPM_L	-2.13E-13	2.10E-10	-2.01E-17	-5.47E-15
SiPM_R	-1.93E-14	-2.01E-17	2.10E-10	-8.07E-13
Cathode	-1.05E-11	-5.47E-15	-8.07E-13	1.19E-10

Figure 20. The capacitance matrix for the SiPM circuit board charge injection, due to discharge with only cathode conductive mesh shielding, which results in 64nC and 81nC injected at the SiPM circuit boards.

Then, adding a 1cm x 1cm conductive C-channel of shielding around the SiPM circuit board was modeled, which showed another dramatic reduction in the simulation - reducing the injected charge to 1.8nC and 1.5nC for the left and right SiPM circuit boards respectively.

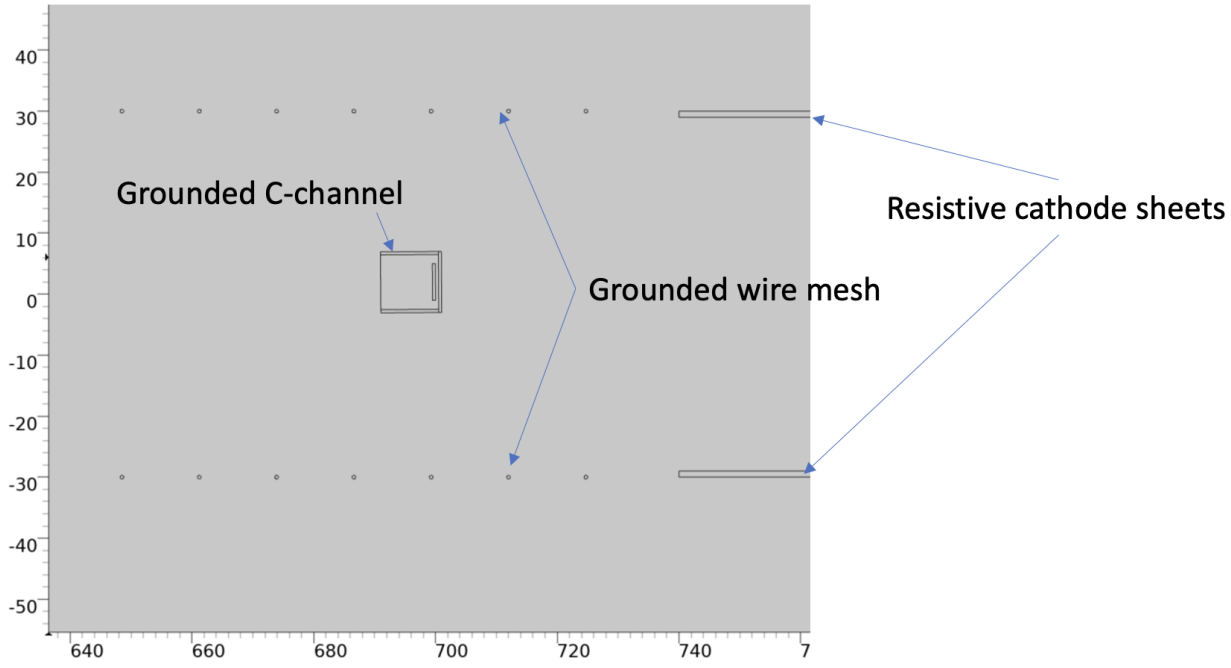

Figure 21. SiPM shielding optimization study considering the impact of a 1cm overhanging conductive C-channel, with the cathode conductive wire mesh.

Maxwell capacitance (F/m)				
	FC	SiPM_L	SiPM_R	Cathode
FC	2.34E-10	-6.00E-15	-8.02E-16	-1.05E-11
SiPM_L	-6.00E-15	2.24E-10	-3.47E-20	-2.20E-16
SiPM_R	-8.02E-16	-3.47E-20	2.24E-10	-1.49E-14
Cathode	-1.05E-11	-2.20E-16	-1.49E-14	1.19E-10

Figure 22. The capacitance matrix for the SiPM circuit board charge injection due to discharge, with a 1cm overhanging conductive C-channel and the cathode conductive mesh shielding, which results in 1.8nC and 1.5nC injected at the SiPM circuit boards.

Finally, one step further was considered, adding a 2cm x 1cm conductive C-channel of shielding around the SiPM circuit board, which the BNL simulation showed reduced the injected charge to 50pC and 30pC for the left and right SiPM circuit boards respectively.

Other shielding concepts considered were a 70% transparent C-channel and no C-channel with double-density conductive cathode mesh; both were shown by the BNL simulation to be worse than the 1cm x 1cm C-channel.

SiPM Shielding Implementation

The conclusions from the SiPM shielding study were that simple conductive shielding can significantly reduce the injected charge into the FD2 PDS sensitive electronics, and the design plan was set forth to target at least a 1cm C-channel shielding overhang surrounding the SiPMs in the XA frame design.

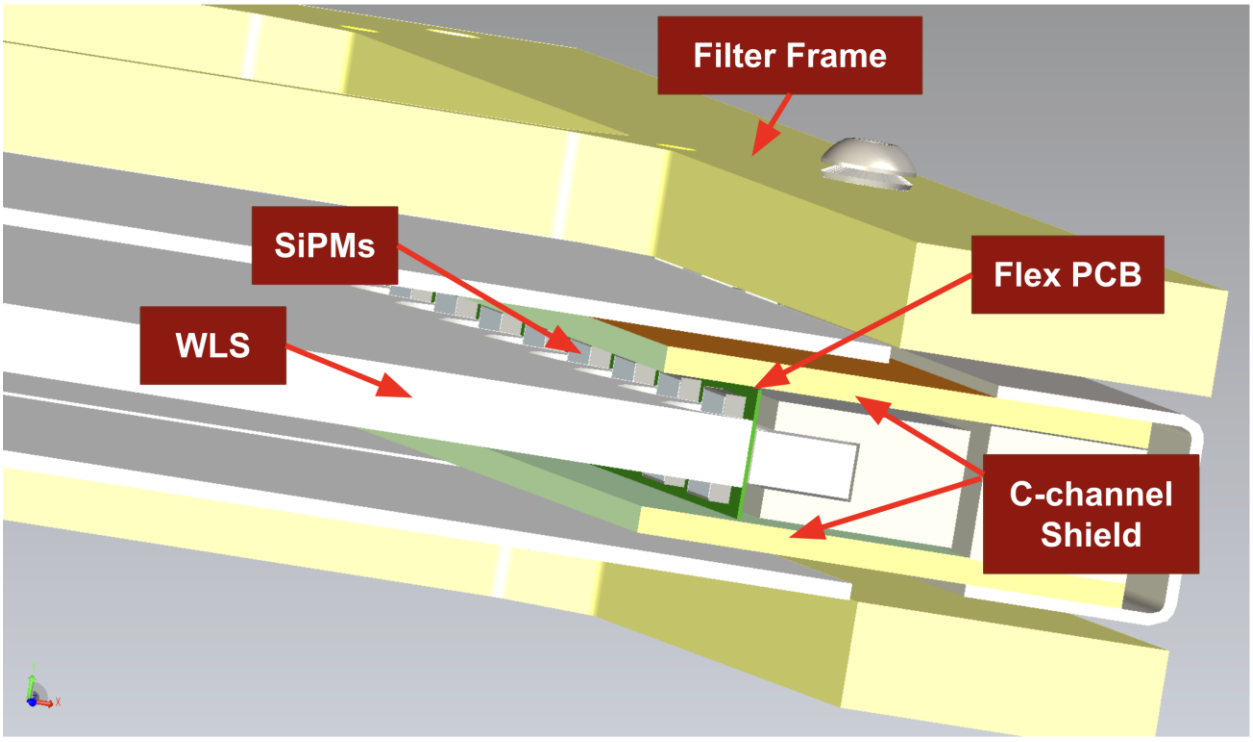

Figure 23. CAD model of XA frame design with C-channel SiPM conductive shielding.

Membrane-mount XA Charge Buildup Mitigation

The Membrane-mount XA mesh minimizing charge buildup on the non-conductive surfaces of the XA was optimized through an additional study from BNL (B. Yu, et. al.). In modeling the effect of varying the wire distance from the insulator, a 2-dimensional model was employed with a single wire grid cell of 10cm width, with the top surface of the cell biased at -150kV. The other three sides of the cell are mirror symmetry boundaries, with no normal electric field components. The results of the study showed an optimum wire mesh heigh of 2cm above the XA surface.

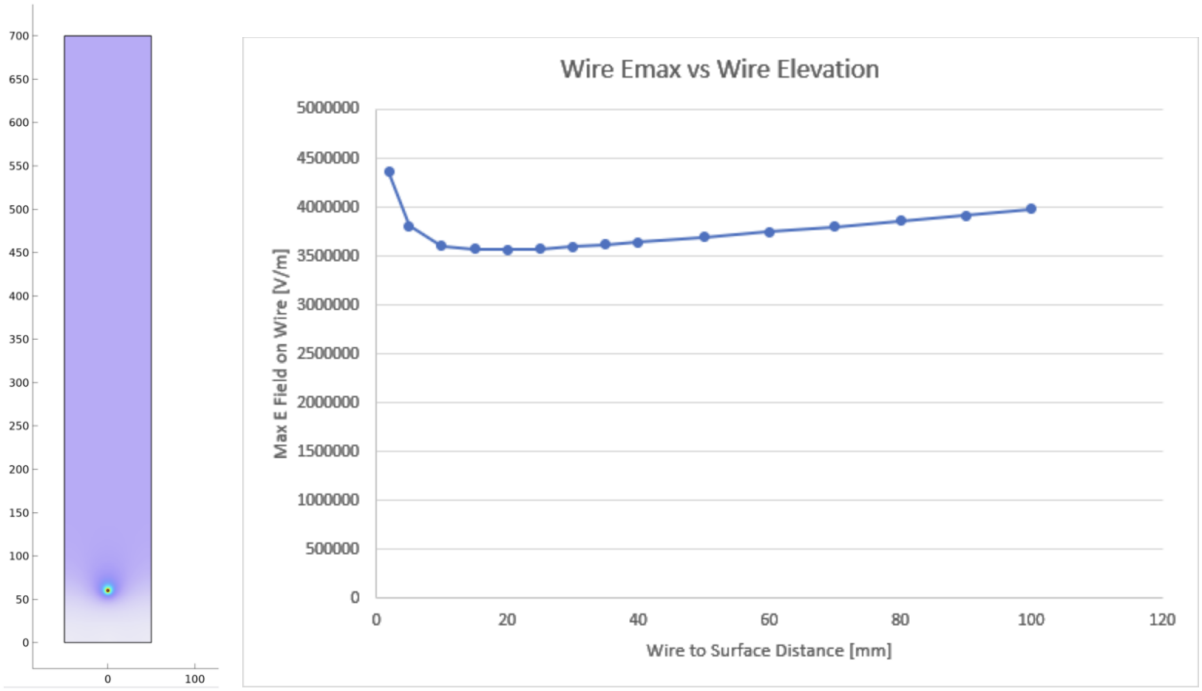

Figure 24. Analysis of the optimum wire mesh height above the XA surface, showing an optimum heigh of 2cm.

Membrane XA Shielding Implementation

The Membrane-mount XA wire mesh shielding final design was then decided to target a 2mm wire diameter, at 2cm from the non-conductive XA surfaces, in a 5cm x 5cm grid to satisfy the threshold requirements of -7kV for max potential on the surface of the XA and 25kV/cm max electric field.

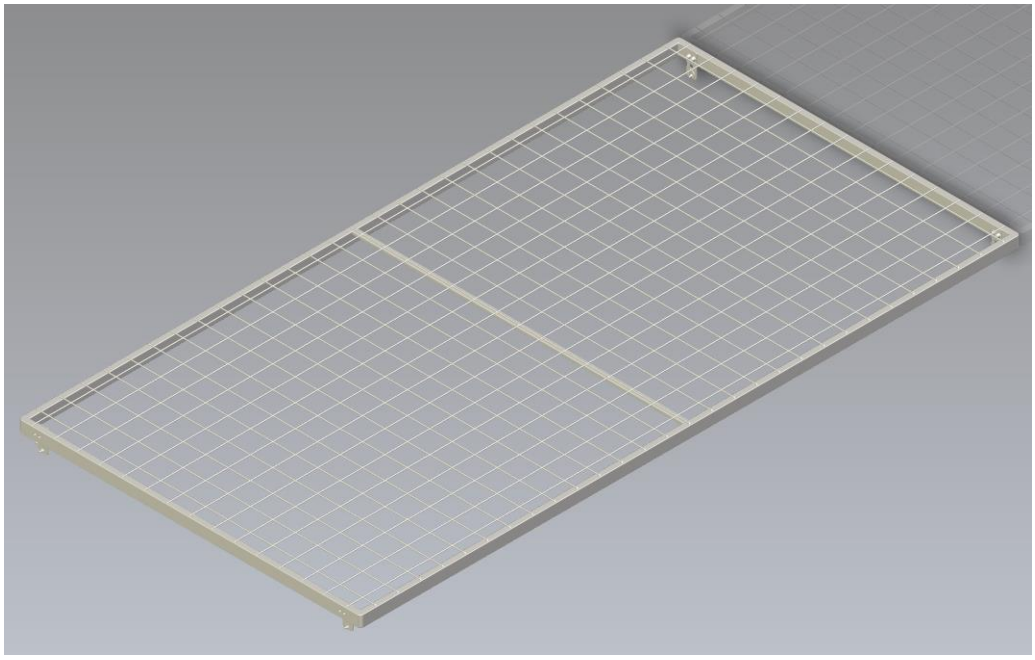

Figure 25. Membrane-mounted XA HV-shield 5cm pitch mesh CAD model.

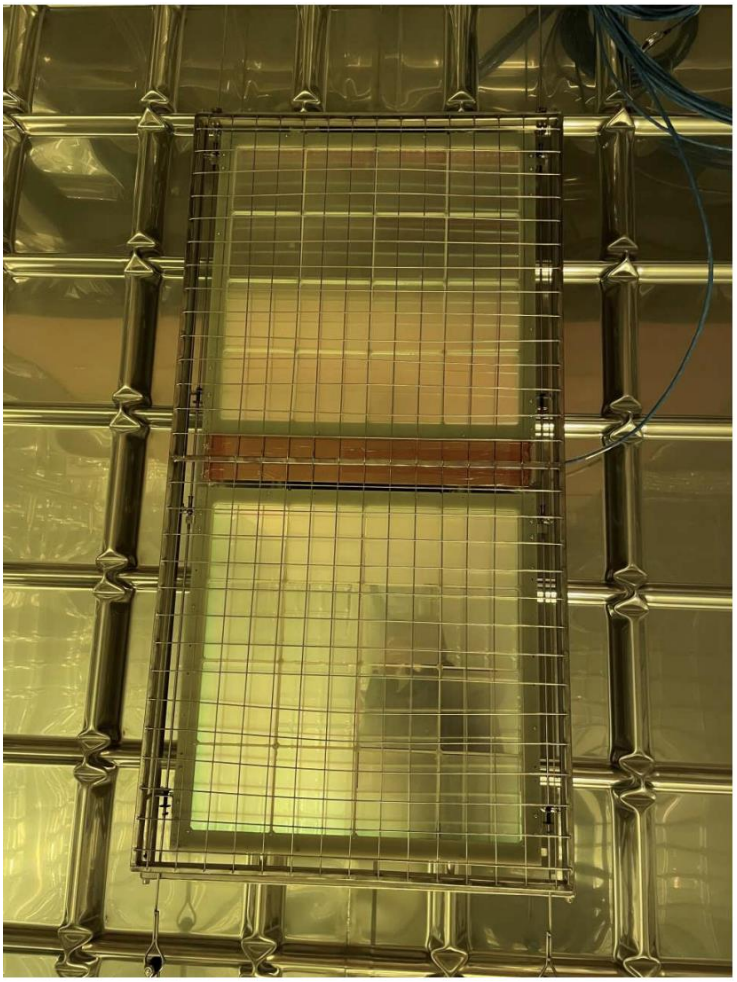

Figure 26. Membrane-mounted XA with HV-shield mesh protection installed at ProtoDUNE2-VD.

Cathode-mount XA Discharge Mitigation

The primary conclusions, with regard to the FD PDS Cathode-mount XA, from the two independent studies at BNL and FNAL are as follows:

- During a discharge, there is some risk (worse at the cathode edges) to an independently powered XA, but it is reasonable to expect that a conservatively shielded XA design would survive at any location on the cathode.
- During a discharge, there is more risk (still worse at the cathode edges) to XAs that share/distribute power and signal, but it is reasonable to expect that a conservatively shielded XA design, with conductive conduits and balun box break would survive in the central cathode modules.

- To converge on a conservatively shielded XA design, at test benches cathode discharges should be emulated with progressive charge injection approaches; the readout electronics should be monitored during the charge injection to identify weaknesses in the shielding, and to identify which components are most sensitive.
- To demonstrate survival and complete the qualification of the final shielded XA design, at the end of the Module-0 run, discharges of the ProtoDUNE2-VD HV system should be induced.

Cathode XA Discharge Mitigation Implementation

As a direct result of the above conclusions (presented to the FD2-VD Technical Board on April 27, 2022), the FD2 PDS Cathode-mounted XA baseline topology was modified from a topology requiring shared power and bias distribution among XA, to a topology of independently powered and biased XA. Also, XAs originally located in the cells of the cathode immediately adjacent to the field cage were moved inward by one cell, away from the field cage. This FD2 PDS topology modification was decided to be the most conservative topology possible, within the constraints of available resources for the FD2 PDS subproject.

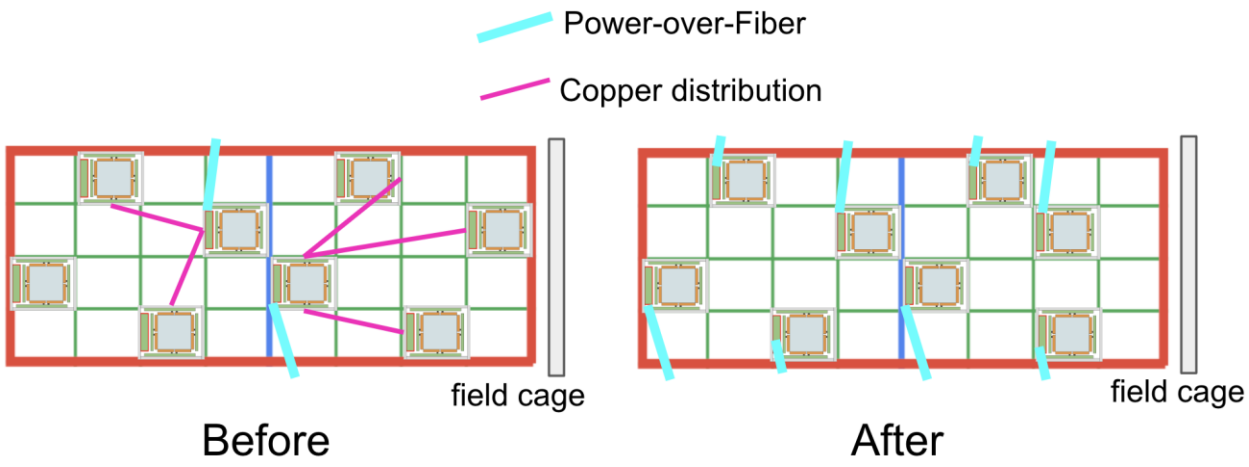

Figure 27. Cathode-mounted XA topology before and after responding to the HV discharge study conclusions of moving XA inward from the edge of the cathode and independent power and local bias generation.

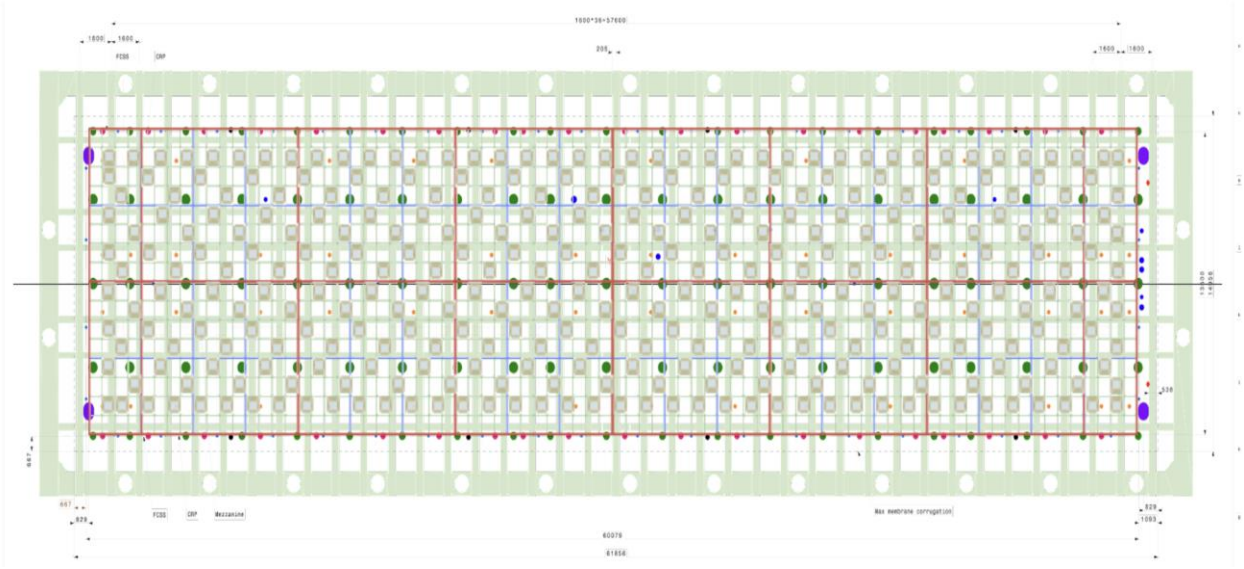

Figure 28. Full FD2 Cathode-mounted XA topology.

It is critical to note that local bias generation (i.e. a DC-DC step-up convertor) is required to support the independently powered XA topology (the alternative of stacking optical power converters in series was determined to be cost prohibitive). The complete bias generation solution, compatible with the constraints of the Cathode-mounted XA, was developed as part of the FD2 PDS prototyping phase which led up to Module-0 deployment. Three independent bias generation design and qualification efforts were launched: one commercial (led by University of Iowa: Mike Miller, et. al.) and two custom (one led by INFN-Milano: Niccolò Gallice, et. al.; one led by Lawrence Berkeley National Laboratory: Marcos Turqueti, et. al.). All three local bias generation design and qualification efforts culminated in successful demonstrations at the CERN Cold Box. The ultimate down-selection was made with consideration for performance, cost, and cryogenic lifetime qualifications – the design from Lawrence Berkeley National Laboratory was selected. Future bias generation optimization and characterization activities are still planned, leading up to the FD2 PDS Production Readiness Reviews.

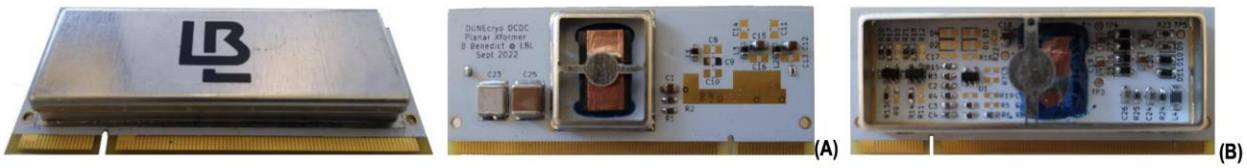

Figure 29. Redundant bias generation solution from LBL utilizing amplifier qualified in LAr for GERDA experiment.

In parallel with the bias generation efforts, a balun box bias voltage distribution design was launched, anticipating that copper bias voltage distribution (e.g., among four XA in each central cathode module) might be more cost effective than local bias generation for each XA. However, the balun box distribution effort did not converge in advance of the Module-0 installation timeline at ProtoDUNE2-VD. The prototype balun box test setup represented the cathode HV discharge with a 500 Hz pulse generator at 1.5 kV peak-to-peak.

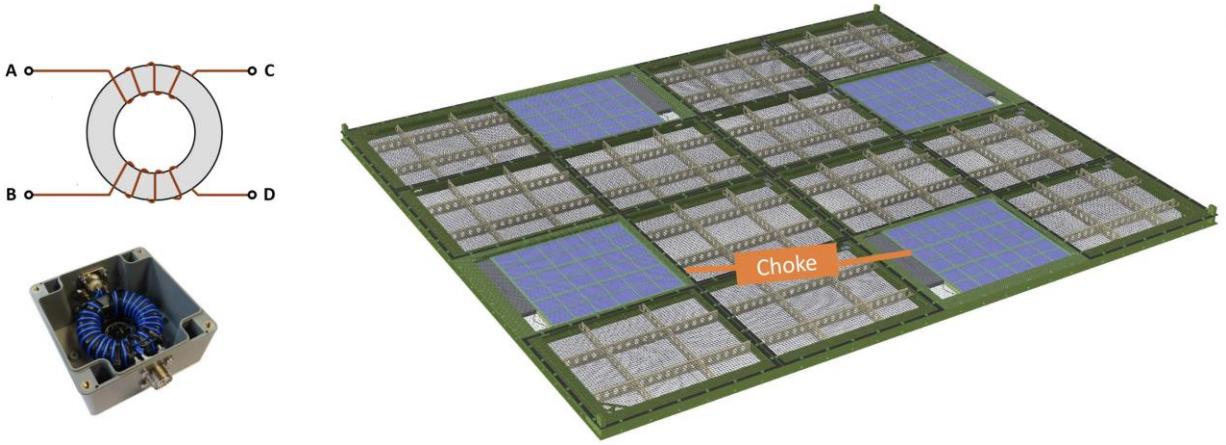

Figure 30. Balun bias voltage distribution concept.

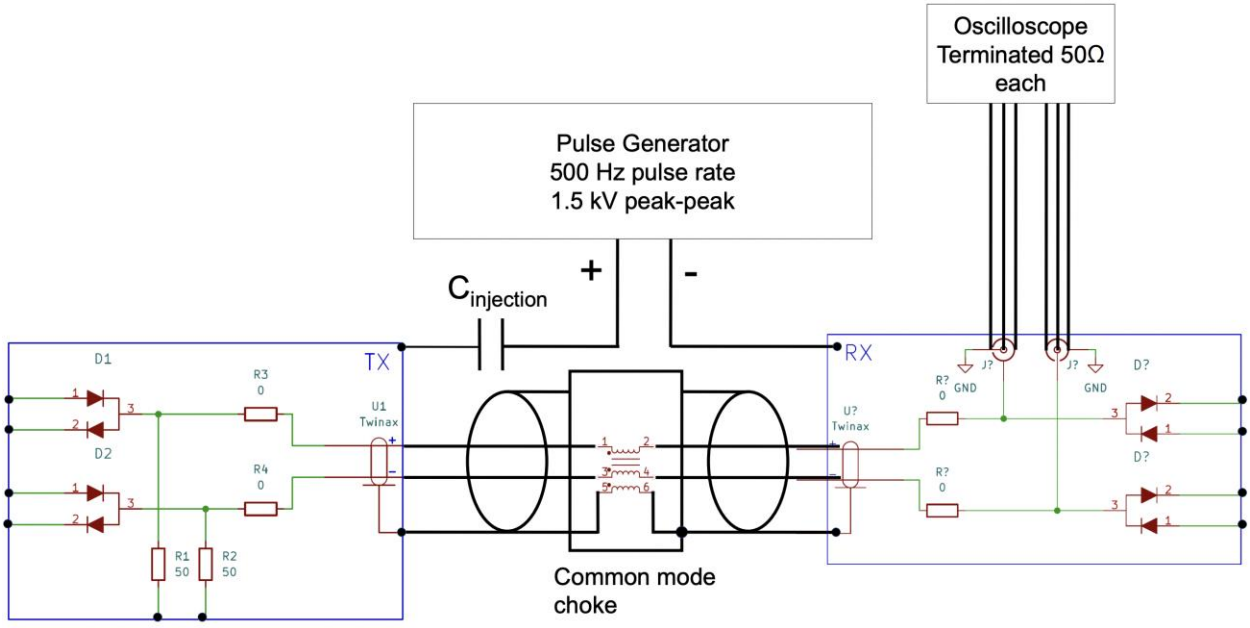

Figure 31. Balun bias voltage distribution test setup schematic.

As the local bias generation has been demonstrated to meet the FD2 PDS requirements for the SiPM bias and is compatible with FD2 PDS cost and schedule constraints, continuing the balun box design effort is low priority; FD2 PDS resources are anticipated to focus, in advance of the FD2 PDS Production Readiness Reviews, on optimizing the local bias generation solution that was deployed for Module-0.