Design Validation I:
Highlight results from VD PDS Prototyping Phase

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Prototyping Campaigns - CERN Coldbox

- Since December 2021 (first test of concept)
- 10 coldbox runs (parasitic, CRP and PDS-only)
- Importance: only available space for integrated xArapuca and cold electronics testing in depth in LAr

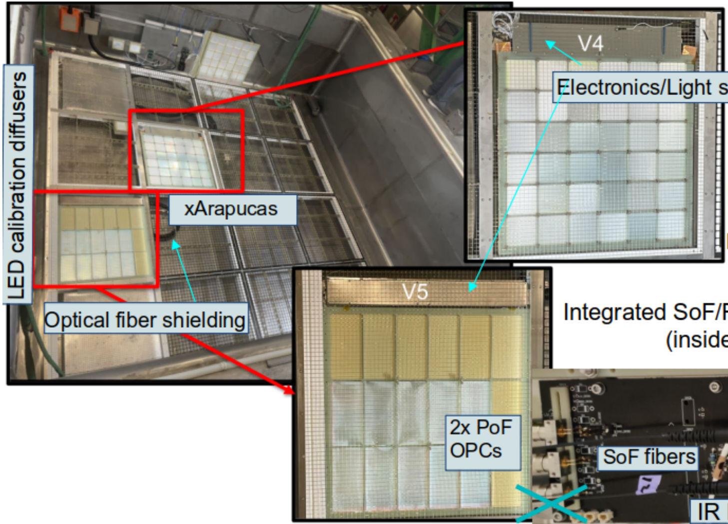
Purpose of the coldbox:

- Testing of the PDS system in realistic conditions
  $\rightarrow$ best/only way to validate the behavior of certain components
- Integration to CRP system
  $\rightarrow$ coordinated data taking

In this talk:

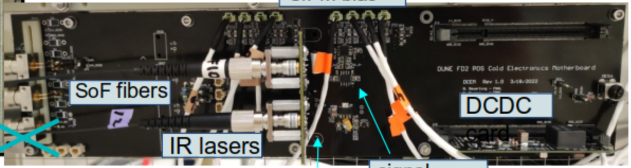
- Brief setup description
- Highlight of performance results obtained in 2023

Coldbox Installation - Cathode

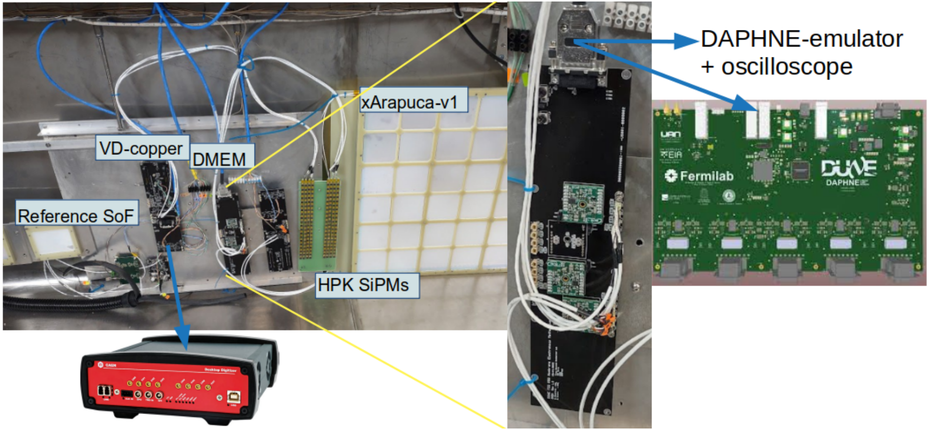


CAEN DT5730SB
14 b, 500 MS/s

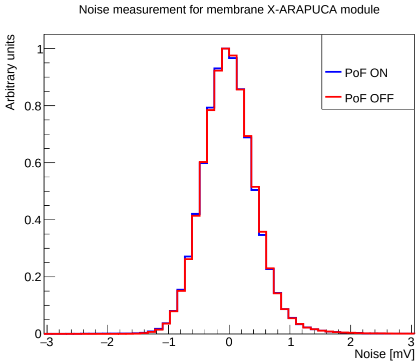
Integrated SoF/PoF electronics
(inside box)

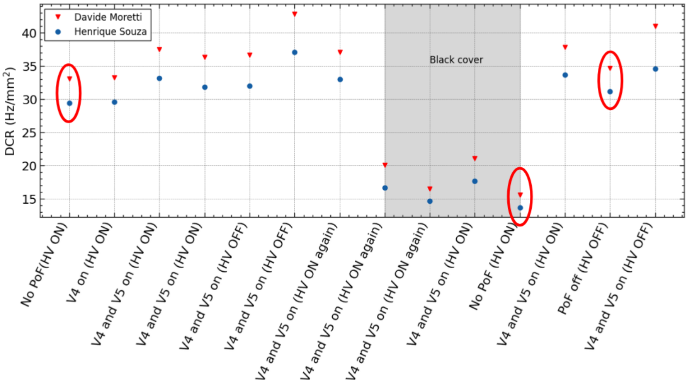


Coldbox Installation - Membrane



PoF and light leakage





- Black PVDF jacket on all fibers
- Black PTFE tubing (shield and protect fibers)
- Metallic cases for the electronics and FC-FC connectors

Result: no measurable light leakage from cathode system,
but we measure external light coming through CB edge

Latest cold electronics implementations

SoF

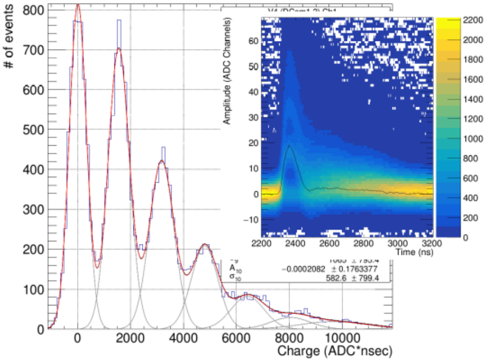
- New iteration of integrated motherboard and laser adapter: DCEM 1.2 SoF/PoF electronics
- Laser driver modification allowed to extend the dynamic range
- New defocused lasers allowed to overcome flooding issues
- Fine tuning to improve SNR: gain, pairing with DCDC, laser offset
- Proved that we can power with only 2 GaAs OPCs
- DAPHNE readout was attempted

Membrane

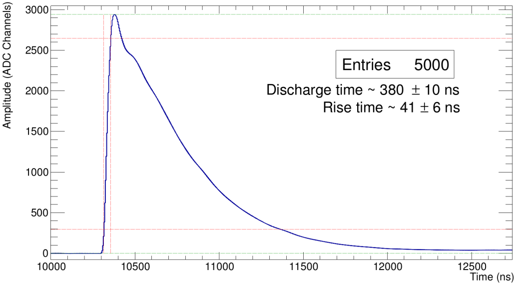
- HD amplifier with DMEM motherboard:
  $\rightarrow$ adapted to the VD-PDS and first data collected
- VD-style copper readout implemented on a SoF board
  $\rightarrow$ new boards have now been fabricated

SoF results - SPE sensitivity

V4 - DCEM 1.2 - March 2023



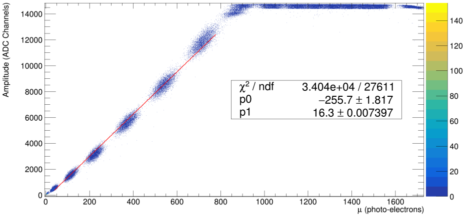
Average LED signal (for one LED voltage)



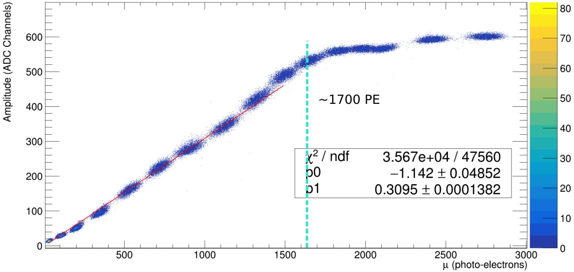
- Have implemented slightly different electronics configurations to understand the impact on SNR
- SPE signals extracted for both xArapucas, results consistent amongst modules and with expectations
- Rise time obtained is between 40 and 50 ns (measured between 10 and 90% of the amplitude)
- SNR= $\frac{\mu_1}{\sigma_0} \sim 5$ (with SPE 20 ADC)

SoF results - dynamic range and calibration

V4 - DCEM 1.2 - March 2023



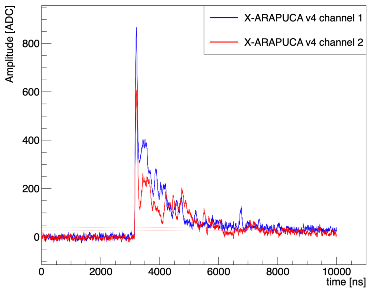
SPE amplitude ∼18 ADCs → warm side saturation at ∼780 PE

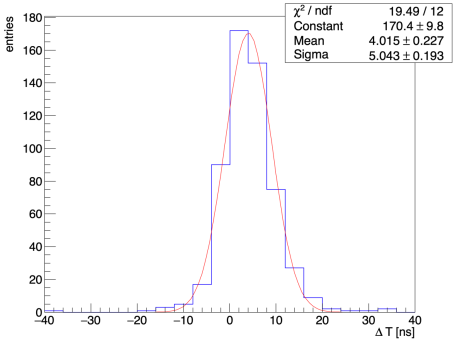


Using intercalibration, dynamic range of the cold electronics ∼ 1700PE

- Setup limitations: LED light non-linearities and commercial receiver saturation
- LED behavior was checked by comparing with signals from cosmics
- A light attenuator was added on the warm side to explore the full dynamic range of the cold electronics
- On-going simulation-based studies to determine a physics-driven requirement for the dynamic range.

SoF Time resolution



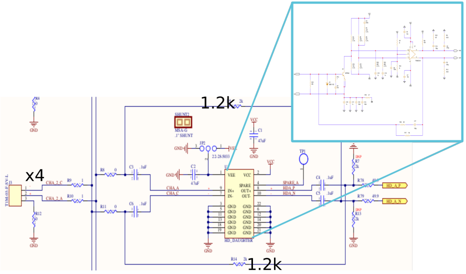


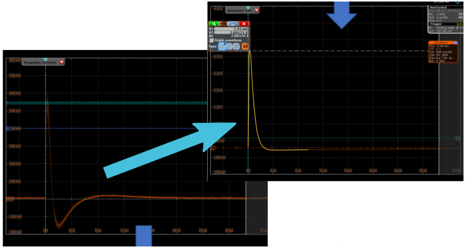
- Time resolution considers two channels of the same xArapuca (assumed to have same resolution)
- No fit/interpolation used to estimate the signal times

- $\sigma_T \sim \sigma(t_{ch1} - t_{ch2})/\sqrt{2}$
- Time resolution is consistent with digital sampling rate $\sim$ 4 ns

Membrane results - HD amplifier implementation

- Same HD cold amplifier as FD1, new context: SiPM hybrid ganging, DMEM motherboard, new PCB production
- After first tests in December 2022, modifications allowed a successful data-taking in March 2023
- Warm 2nd stage (DAPHNE input stage emulator): transformer by-passed to reduce undershoot, two amplifiers used for differential to single-ended conversion
- larger decoupling capacitors

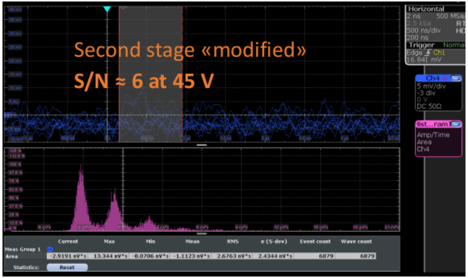




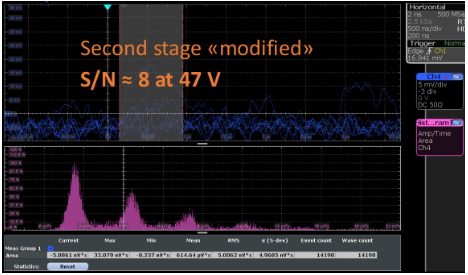
$\rightarrow$ undershoot $<$ 3%

Membrane results - HD amplifier

- Measurement with HPK SiPMs in VD-PDS flexes (not xArapuca)
- Two bias points, +3ov and +5ov

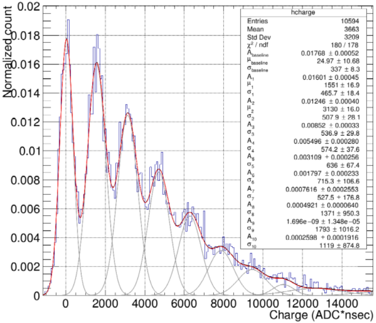


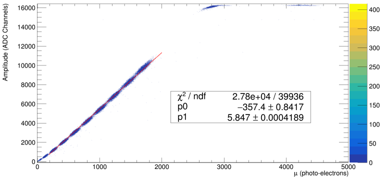
- High background rate, ∼100 kHz
  → possibly cosmics and external light

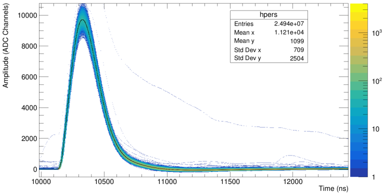


Membrane results - VD amplifier

Development motivated to have similar membrane and cathode signals.
Two configurations (adapted from SoF boards) tested in February 2023.

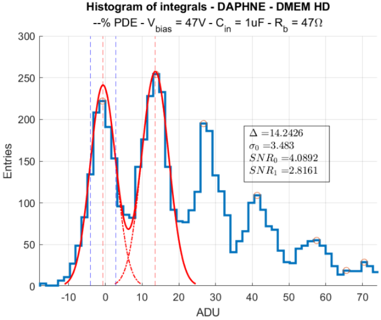


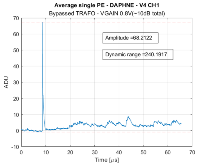


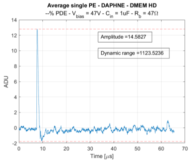


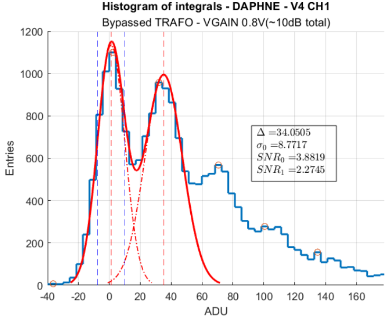
- SPE amplitude $\sim$ 6 ADCs, SNR $\sim$ 3-4
- Linear (with LED effects) up to 1750 - 2100 p.e.
- Rise time $\sim$ 120 ns

DAPHNE test - SoF and HD amplifier

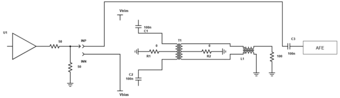




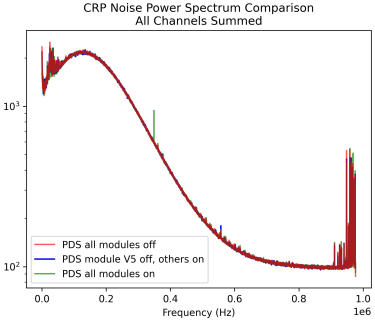


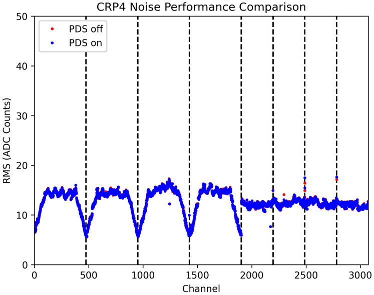


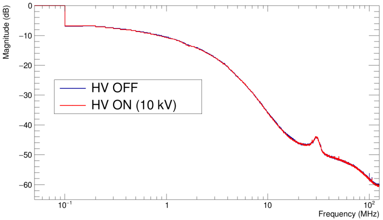
- HD: modified DAPHNE input stage achieves 8% undershoot
- SoF: DAPHNE with bypassed transformer, total 10dB gain
- Still space for improvements: ground loops in coldbox environment, AFE chip configuration, undershoot impact due to high signal rate



Integration



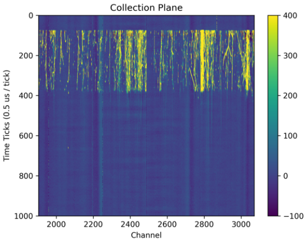


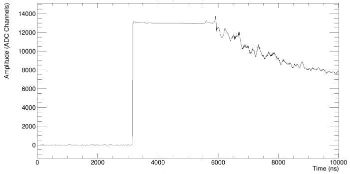


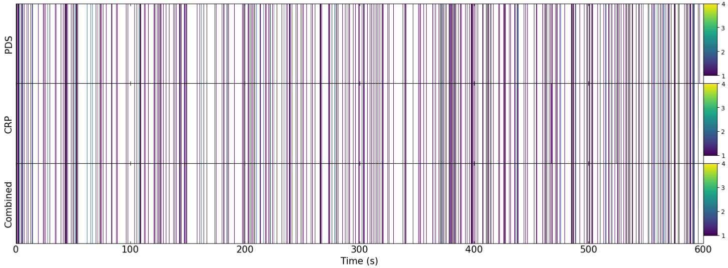
- Only a small 300 kHz peak detected by the CRP electronics, coming from V5 ”hybrid” electronics (now replaced)
- This contribution could not be detected in the electronics noise
- No effect from HV ON/OFF in the PDS

Data taking with CRP

- Simultaneous data taking with CRP (CRT triggered)
- High rate of matched triggers: 5836 by CRP vs 5912 by PDS - small difference due to CRP's 4ms acquisition time.







Conclusions

- Last few months of prototype testing campaigns led up to a mature configuration and satisfactory data output
- All PDS components have been running over multiple cycles inside the coldbox
- Performance goals have been mostly achieved
- We have learnt how to operate our system reliably
  $\rightarrow$ resistance to multiple thermal cycles
  $\rightarrow$ but data taking periods are short, a longer run is planned as final validation.

Thank you! (and many thanks to the PDS team!)

Back Up

Timeline and main benchmarks

February 2021 start of investigations

- analog circuit component selection
- decision to use lasers (over LED) with connectors
- definition of basic circuit characteristics

June 2021 First working analog transmitter

- laboratory tests with SiPMs in LN2 → SPE transmission

September - December 2021 Coldbox A_1

→ **successful SoF operation, with HV ON. Powered using Si PoF modules.**

March 2021: Ariadne parasitic run (A_2)

→ **additional statistics, long operation and first test with (preliminary) DAPHNE**

May 2022 Coldbox A_3 → first test of GaAs

July 2022 Coldbox B

→ **2 xARAPUCAS on cathode and integrated board**

August 2022 Coldbox B+ and B++ → dedicated PDS runs

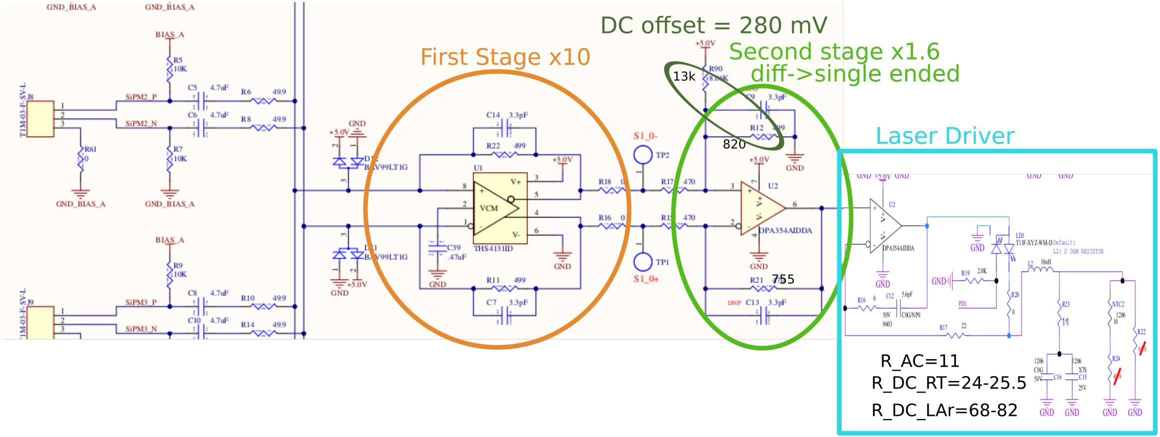
October-December 2022 CRP3, CRP2b runs → Optimized system

February-March 2023 CRP4 and CRP5 → Membrane / increased statistics

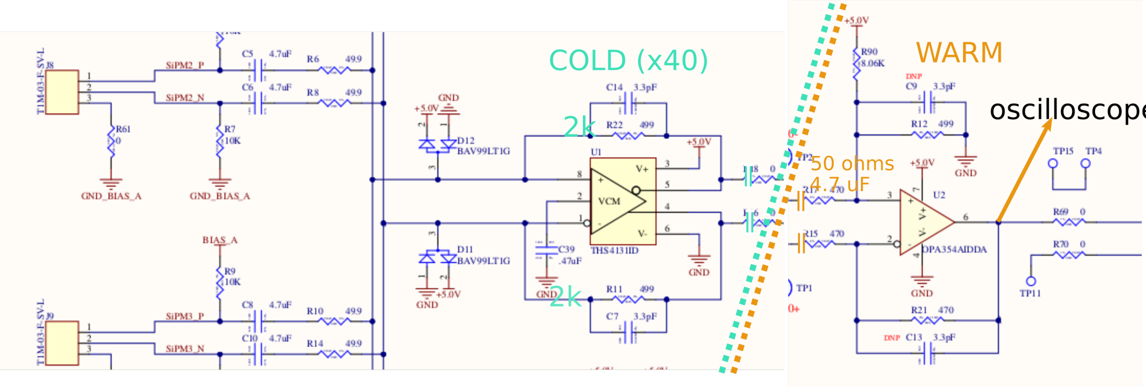
2021 - R&D towards functional prototypes

2022 - Optimization, performance, mechanics and installation - Extensive use of SoF.

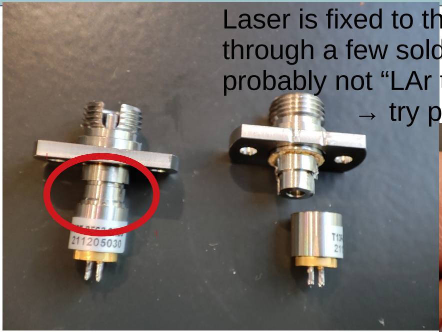
SoF Analog Transmitter Circuit - DCEM 1.2



SoF Analog Transmitter Circuit - DCEM 1.2

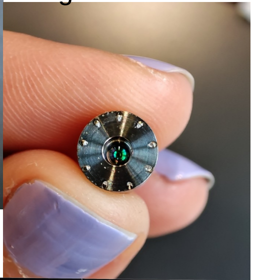


Lasermate FC connector



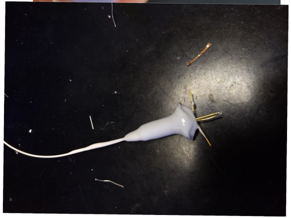
Laser is fixed to the FC connector through a few solder points: probably not “LAr tight”

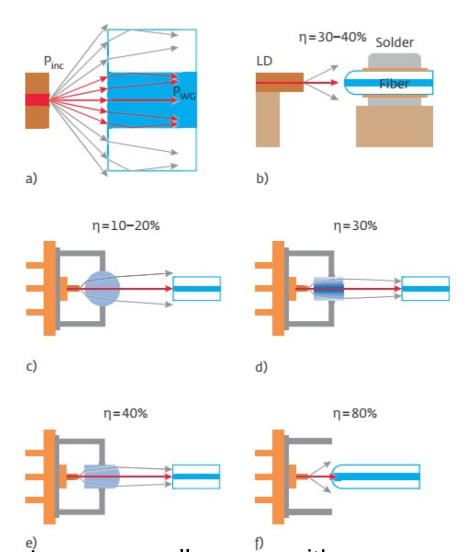
→ try potting this area?



* There seems to be a lens inside → usually the laser beam has a focus point ~few mm from lens

* By fully potting a pigtailed laser we did not see the power output drop
* potting is not trivial

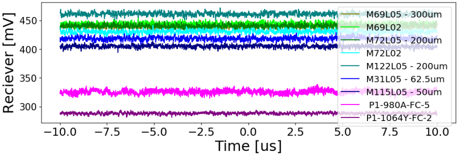


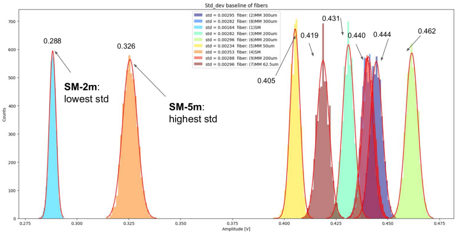


Lasers usually come with some kind of lens → not clear how LAr affects the focus

Fibers

Comparison of 2 single mode and 7 multi mode fibers of different core size and various characteristics and lengths.



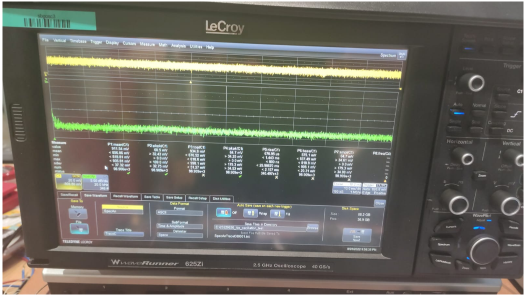


- Single mode should be more stable but depends on which fiber. Pigtail is stable
- Multimode has a much larger transmission efficiency
- Multimode could present modal noise
- jacket material could affect the fiber when in cold
- Testing of graded index fiber (as opposed to step index)
- sharp bends should be avoided $\rightarrow$ laser adapter card is vertical

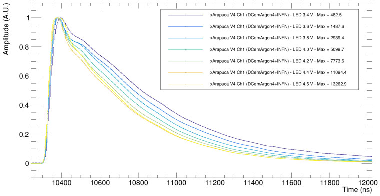
Low-Drop Out Voltage Regulator

First choice of LDO regulator is LP3964

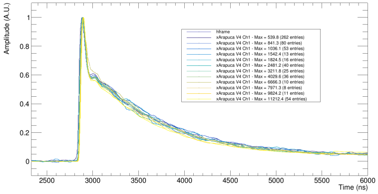
- requires an output capacitor with a relatively high ESR
- recommended tantalum capacitors are not suitable for long-term durability
- tested solution 1: add a resistor in series
- tested solution 2: switch to a more modern LDO AMD7151 that doesn't have this ESR requirement



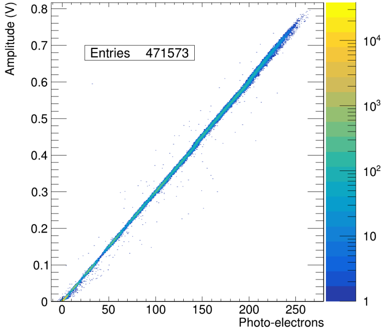
Linearity with Cosmics



LED signals



muon signals

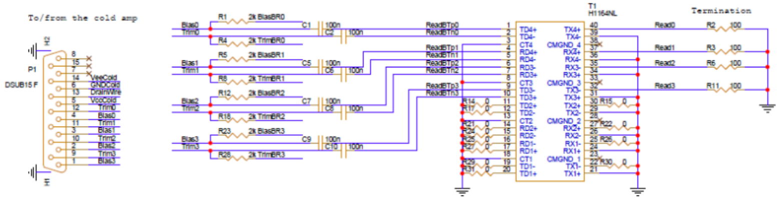


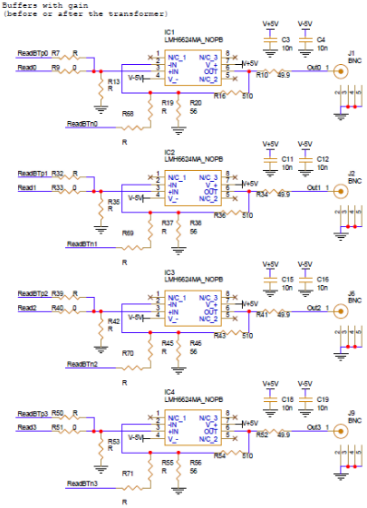
Amplitude vs charge for cosmics

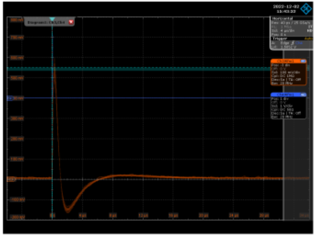
- Signals from LED do not keep a fully linear amplitude-charge relationship
- The signal width changes, since the LED light gets spread in time
- On the contrary, muon signals keep their shape
- This is well reflected by the linear relation between amplitude and charge

Warm second stage “standard”

- Undershoot ≈25% mainly due to input transformer used for differential to single-ended conversion
- Same as unmodified DAPHNE V2A
- There are ways to reduce undershoot with the transformer, studied by Esteban, not applied here

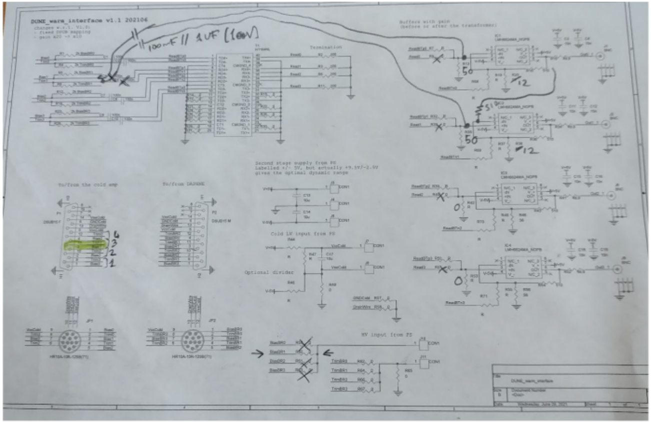


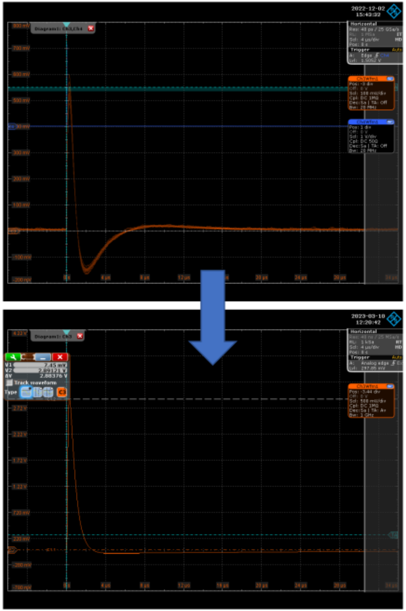




Warm second stage “modified”

- Modified to bypass input transformer
- AC coupling capacitors increased x10
- Differential to single ended conversion done with 2 opamps
- Undershoot <3%





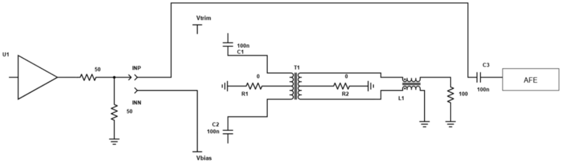
DAPHNE modifications

HD readout

- Need to keep transformer for differential input
- Changed transformer H1164NLT to its electrical analog HX5004ENL
- Modification of Vbias-trim and center tap resistor

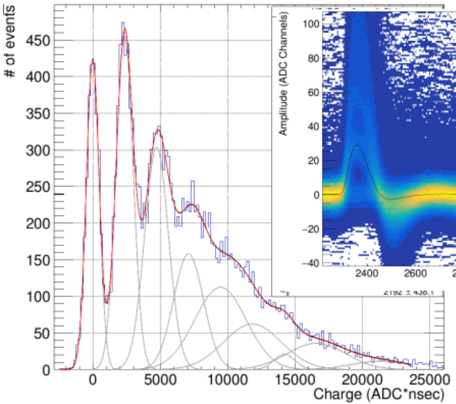
SoF readout

- bypassed transistor (not needed since signal is already single-ended)
- increase of AC coupling capacitors



SNR other channels

V5 - DCEMArgon4 - March 2023



V4 - DCEMArgon4 - February 2023