LSU LArASIC QC Testing at Room Temperature

Donny Phan, Anh Do, Ewerton Belchior, Hanyu Wei

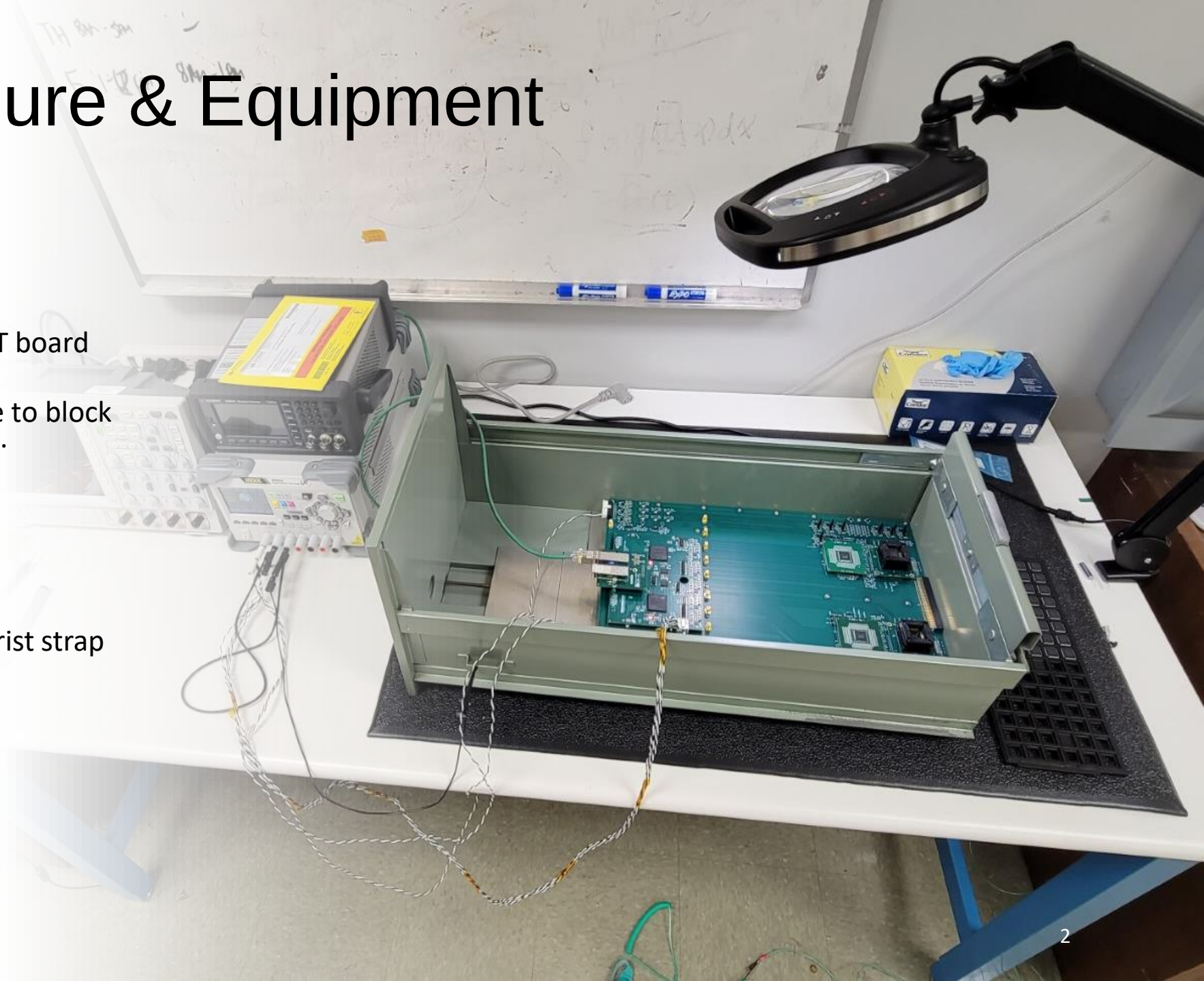
Louisiana State University

Feb 28, 2023

Testing Procedure & Equipment

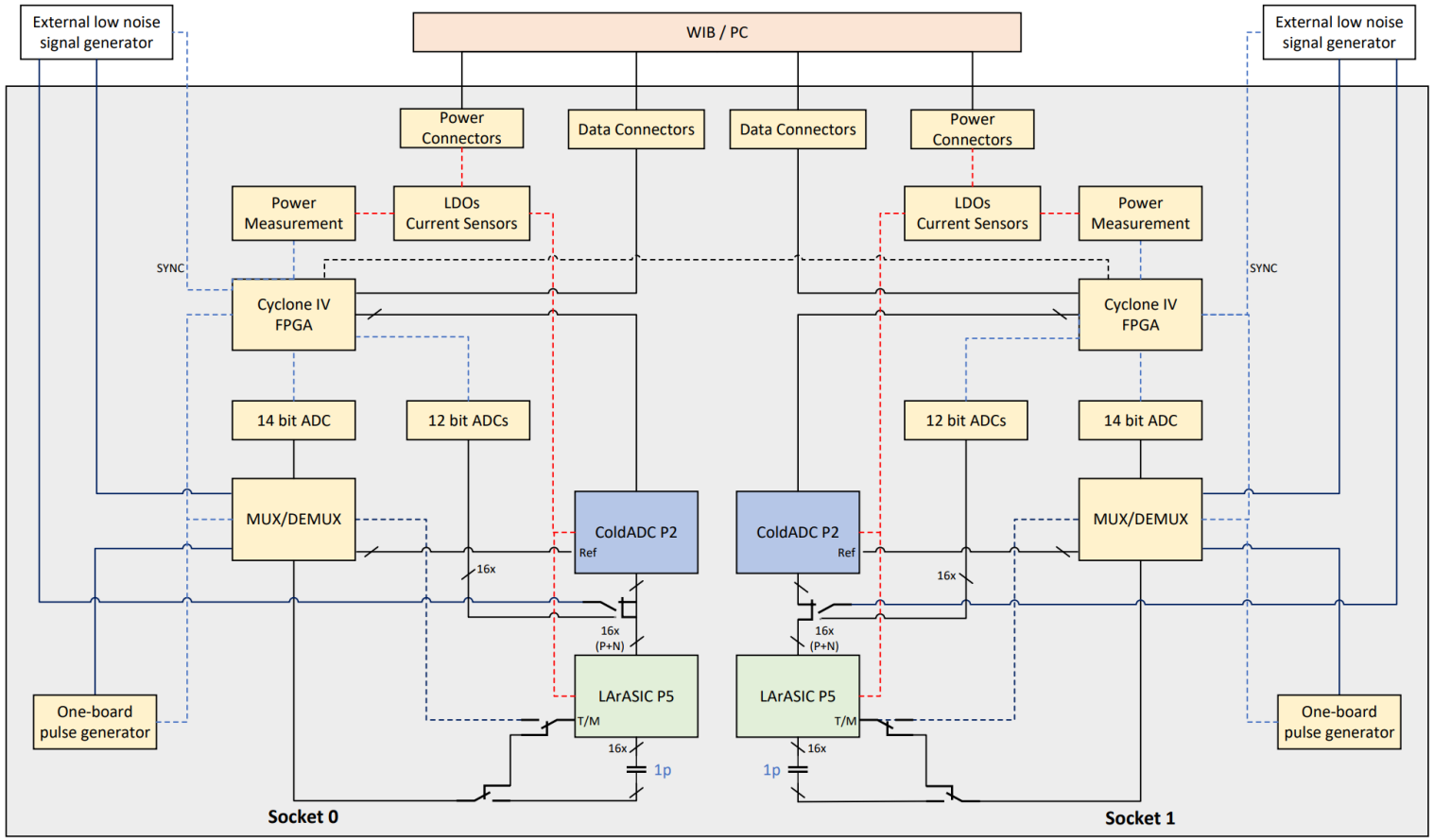
Equipment Used for Room Temperature Tests:

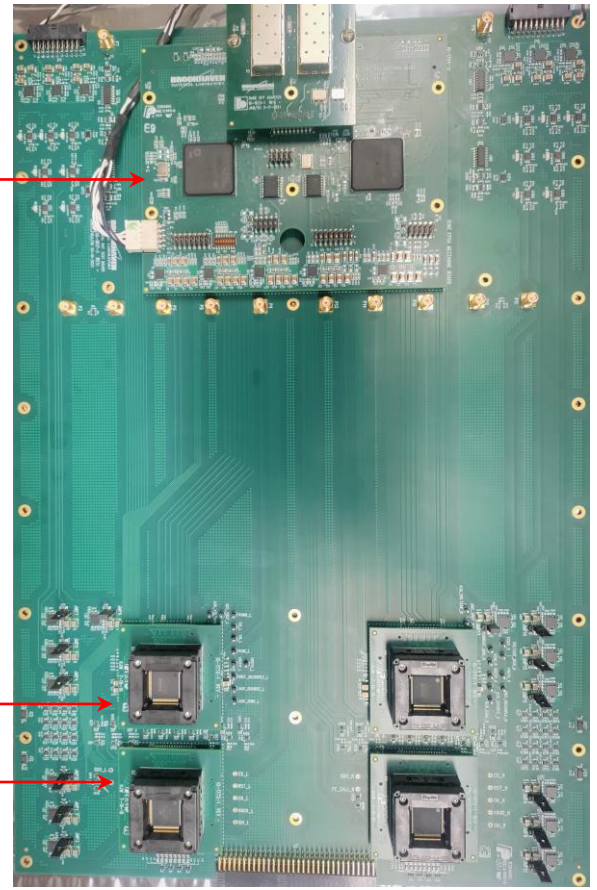
- DIY Faraday's Cage
- Dual-FPGA board and Dual-DUT board (+ two ColdADC P2)
- Grounding connection the cage to block out LSU radio station noise, etc.
- DP832 Power supply
- Banana plug cables for Ground connection to Faraday Cage
- Mini IC Vacuum Tool
- Grounding Mat & Anti-static wrist strap
- Digital Multimeter
- Ethernet Cable
- "DAQ" (desktop)
- Magnify tool



Dual-DUT Test Board

- FM + Test Motherboard + 2 DUTs
  - Can characterize LArASIC thoroughly
  - The assembly will be submerged in LN2
- Interface:
  - Data is readout through UDP interface of Dual FPGA mezzanine
  - Can be readout by WIB as well (require FW update)
- Support LArASIC/ColdADC characterization





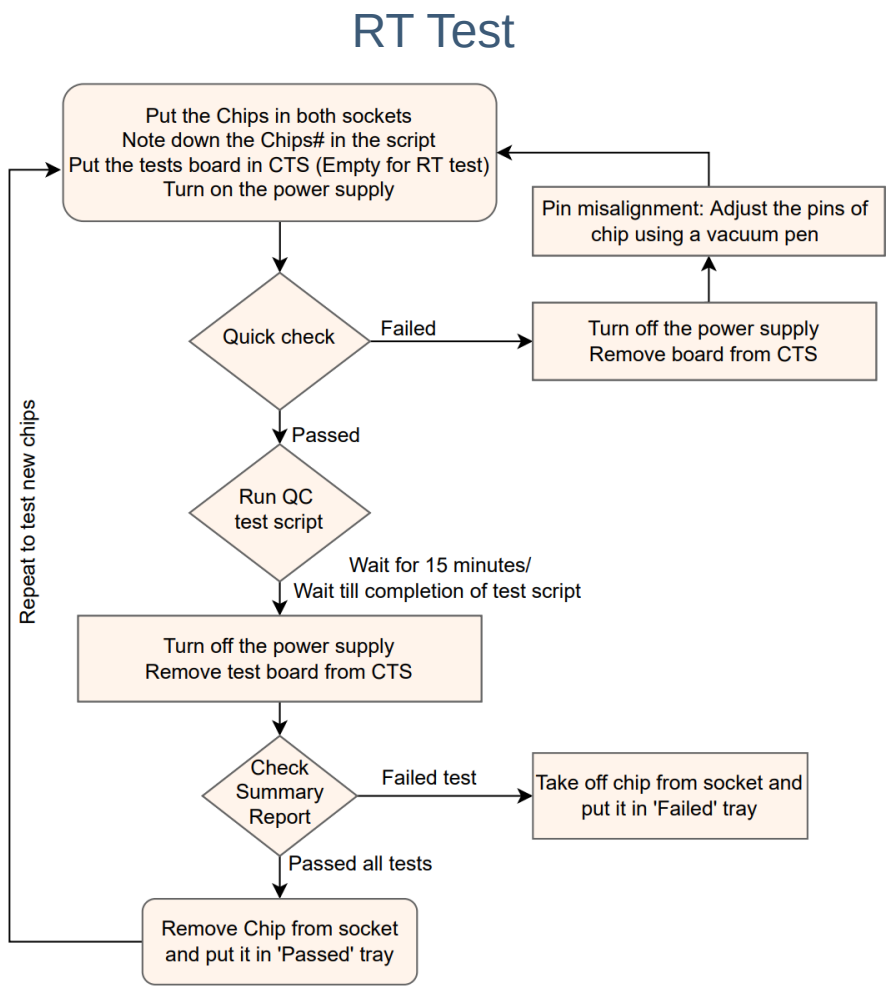
LArASIC QC Items based on Dual-DUT board

Items	Description
QC items for LArASIC QC using Dual-DUT board	
Power consumption	Each LArASIC has 3 power rails (VDDP, VDDA, VDDO) of which voltage and current are recorded under 3 configurations (default, SE on, and SEDC on)
Power cycle	Pulse response checking in each power cycle (3 cycles)
SPI checkout test	Write and read to LArASIC register
Charge pulse direct to input	To check that input is connected to preamplifier (rare case)
Channel pulse response checkout (pulsing from internal DAC)	• To check that output pins are proper connected with packaged pin • Baseline measurements (200mV/900mV) • Pulse response with different peaking time
Monitoring	• Check response from each channel (through test pad) • Baseline measurements (through commercial ADC) • BGR voltage measurement
BL restore test	Check the baseline after 200mV to 900mV baseline configuration and vice versa
Noise measurements	With different peaking time and buffer configuration
Full chain linearity measurements (LArASIC+ColdADC)	• Input from internal DAC • Direct input from external pulse generator • Input from test pin and through internal calibration capacitor • Gain, linearity and pedestal measurements

Testing Procedure & Equipment

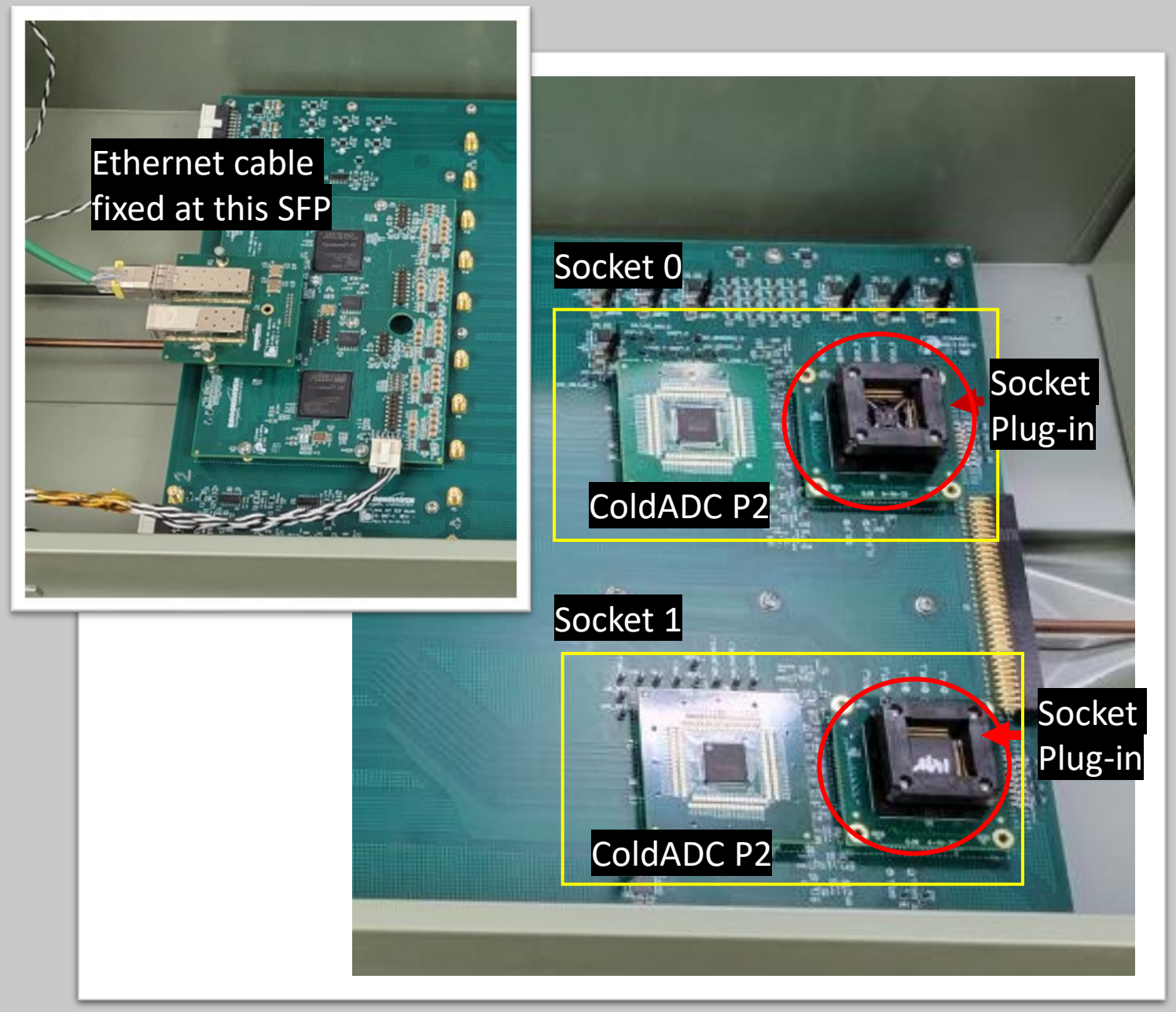
Testing Procedure per test:

1. Power supply set to 5V and 3A for Dual-DUT board and Dual-FPGA board, confirm output with digital multimeter
2. Place ASIC chips into socket with vacuum pen with the correct orientation
3. Open “dual_dut_preset.py”, enter in RT, chip number based on socket placement.
4. Check network adapter settings for IPv4 properties for the IP address and Mask
5. Verify connection
6. Run “Socket0.bat” or “Socket1.bat”



Current Results

- **Completed 2 batches of 270 in total 540 P5B LArASIC chips**
  - ~900 P5B from 3 engineering wafers
  - Packaged by ASE with Serial number: 001-xxxxx
- **536 out of 540 P5B LArASIC chips passed the test**
  - Yield >99%
  - Four chips **00276, 00301, 00677, 00844** failed due to manufacture faulty
- Average of ~10min testing with Socket 0
- Average of ~15min testing with Socket 1



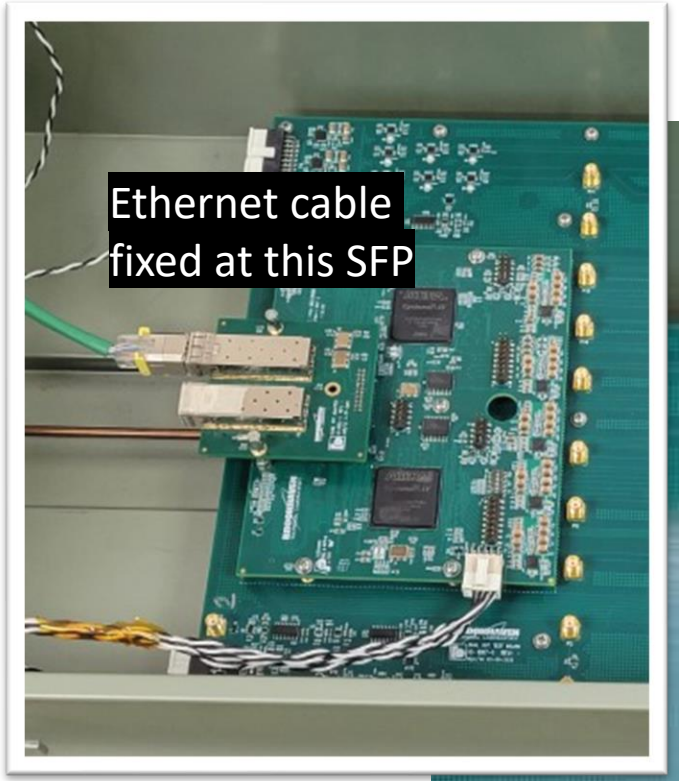
Chip failure in RT test

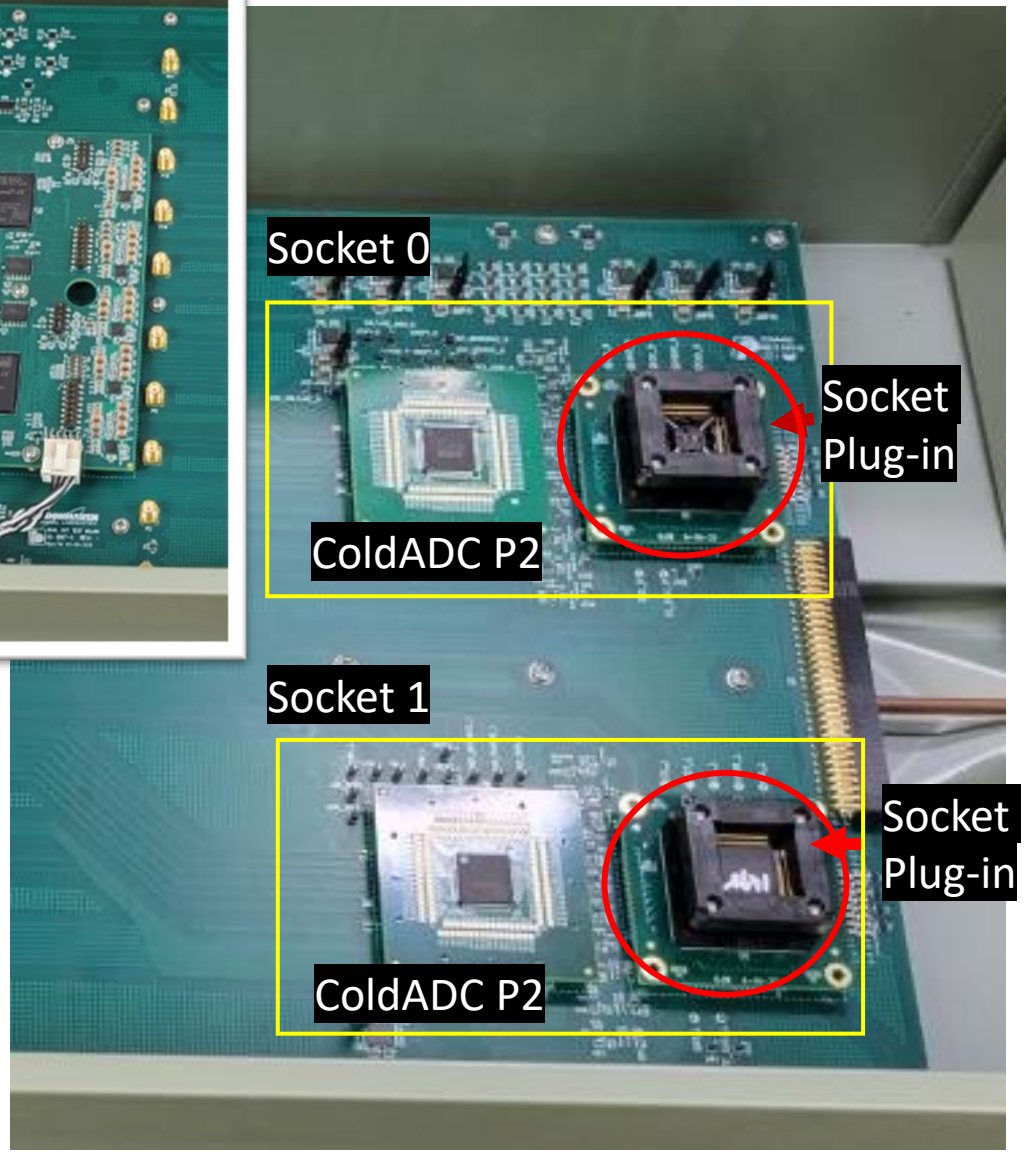
- **0276**: FE Power, FE gain plot, Channel Resp., BL restore test failed
  - BNL: VBGR pin shows less drive capability than other chips. Voltage of VBGR was pulled-down by monitoring ADC.
- **0301**:
  - there was no connection to the Ethernet, the volts from the machine stop at 3V and will not go to 5V
  - BNL: 1 Ohm between VDDA and GND (bad chip)
- **0677**: Power measurement Fail; Channel response (Internal DACs & Ext pulse) Failed; FE power cycle Failed; FE gain plot Failed; Channel #4 is not responding from 1st, 3rd, and 4th round, so it might be a "dead" channel
  - BNL: VDDA (28 Ohm to GND) = 77mA (nominal: 21mA) , bad chip
- **0844**: FE gain (DAC pulsing) Failed
  - BNL: VBGR pin and TST/MON pin show less drive capability than other chips. Voltage of VBGR was pulled-down by monitoring ADC.

Thanks Shanshan and BNL experts!

Issues and what we learned

- Consistent test results in Socket 0 and inconsistency (~50% failure) in Socket 1
- Test parameters were arbitrarily inconsistent in socket 1 failure
  - Main failure mode: power rail of VDD, VDDO, and VDDP with twice the value in current or voltage compared to the successful chip testing
- Swapped the socket plug-in from both sockets to test circuitry, socket plug-in faulty
  - Results were still inconsistent if tested in Socket 1 area while Socket 0 area is good
- Issue is very likely caused by the unstable data communication between the primary FPGA chip (“socket 0” in the side consistent with ethernet cable connection) and secondary FPGA chip (“socket 1”).



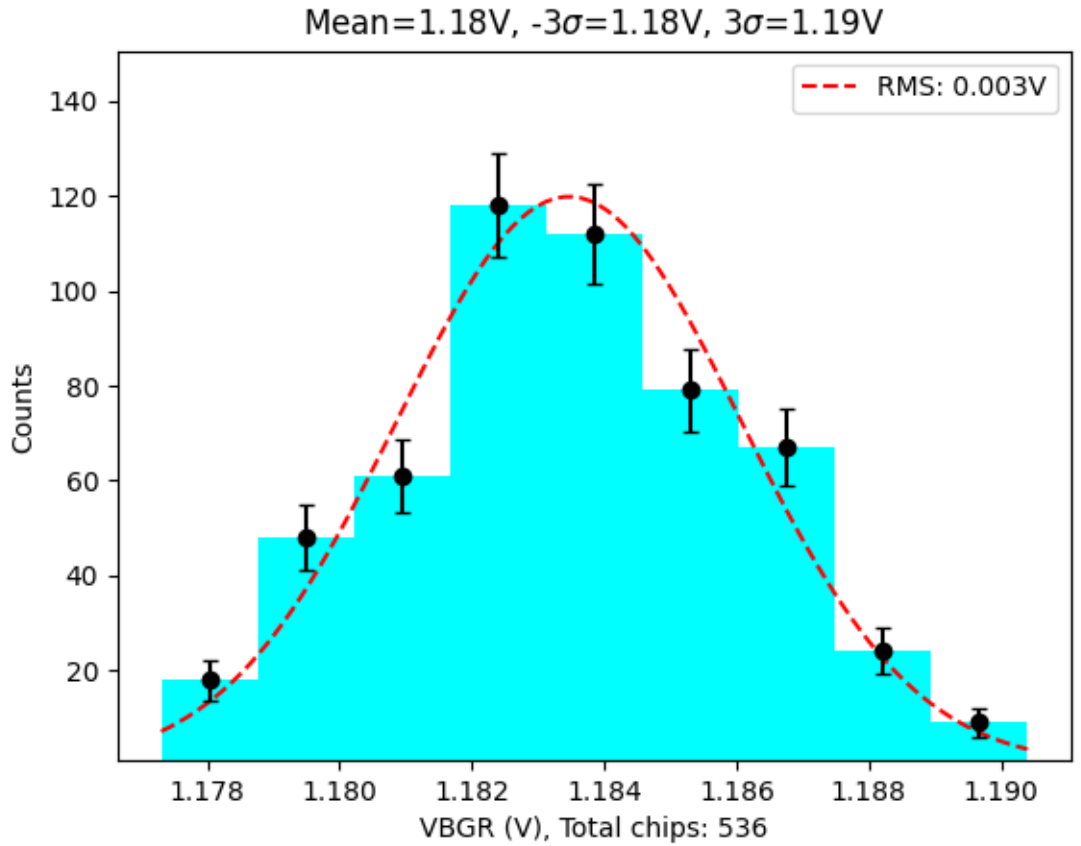


Distributions of good chips' test parameters

- almost all parameter distributions are statistically consistent with a normal distribution
- power distribution is a bit "odd" but this parameter seems not as important as the others and a relatively large deviation is expected

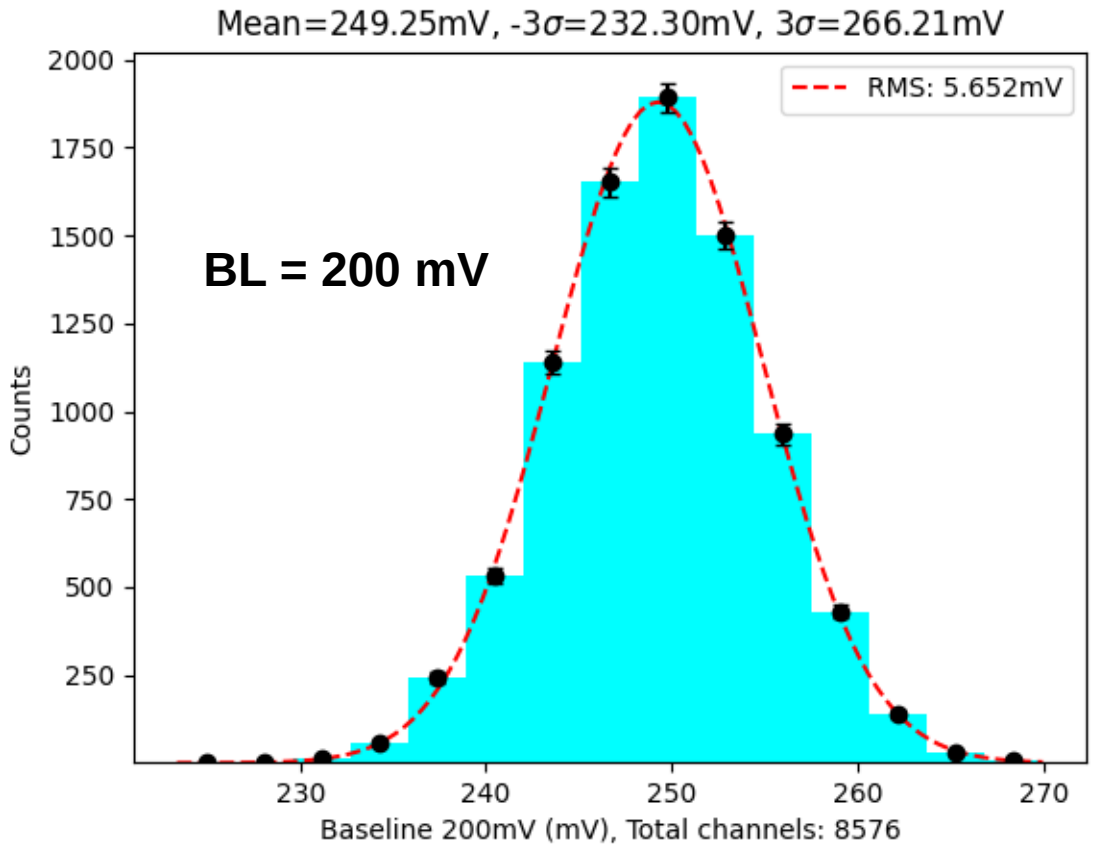
Bandgap reference voltage

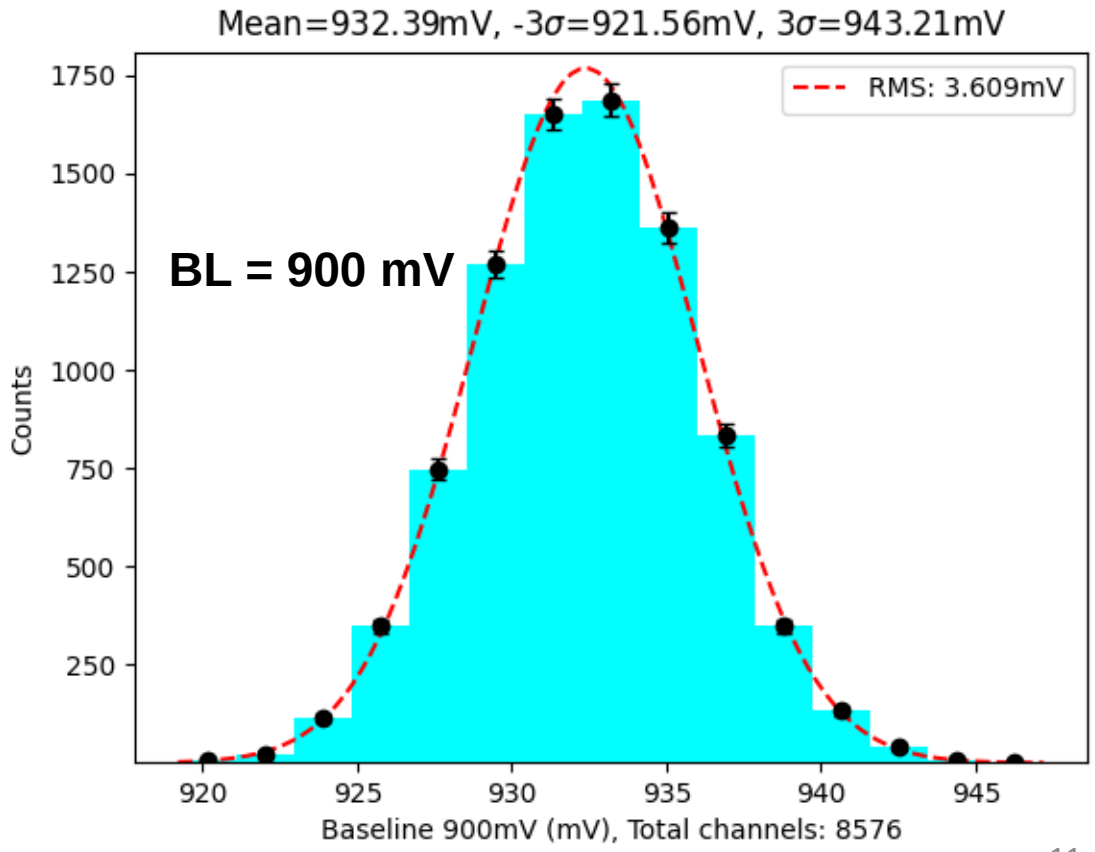
	Mean	SD
BGR Voltage (V)	1.183	0.003



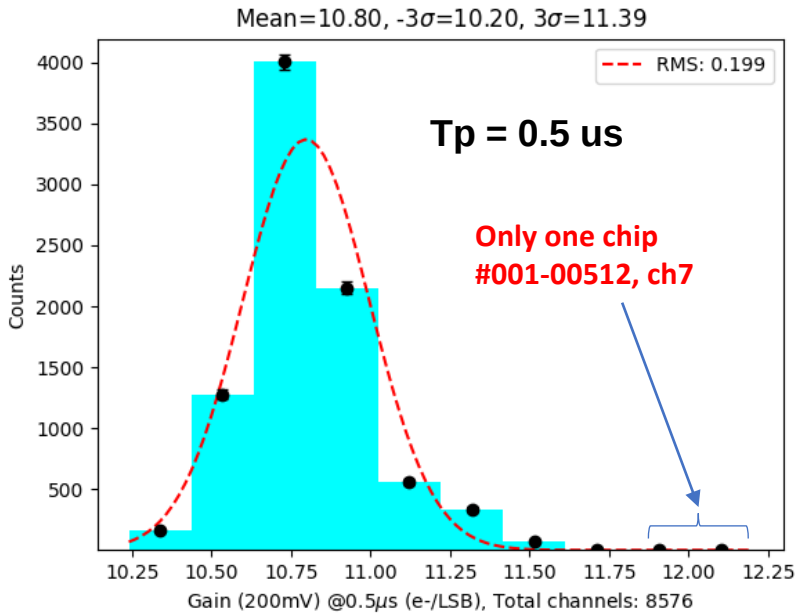
Baseline measurement for each channel (by monitor ADC)

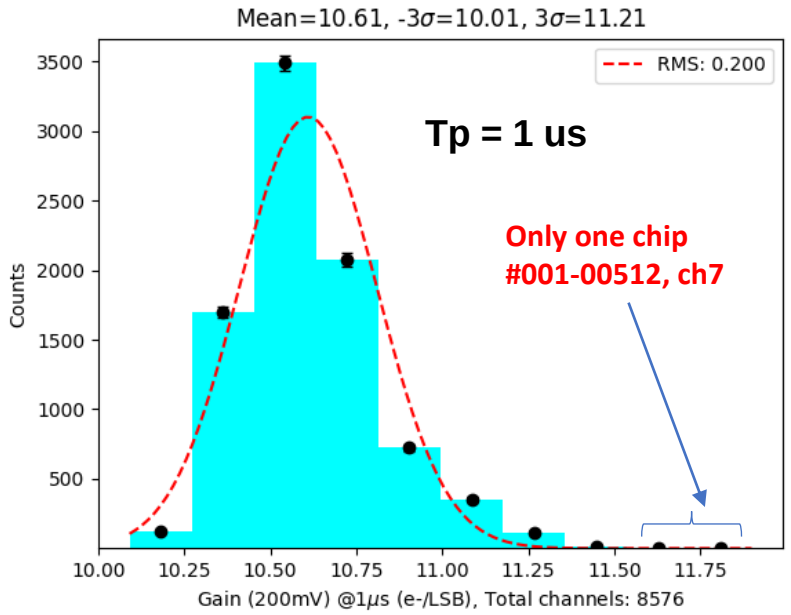
Measured by monitor ADC	Mean	SD
Baseline 200mV (mV)	249	6
Baseline 900mV (mV)	932	4

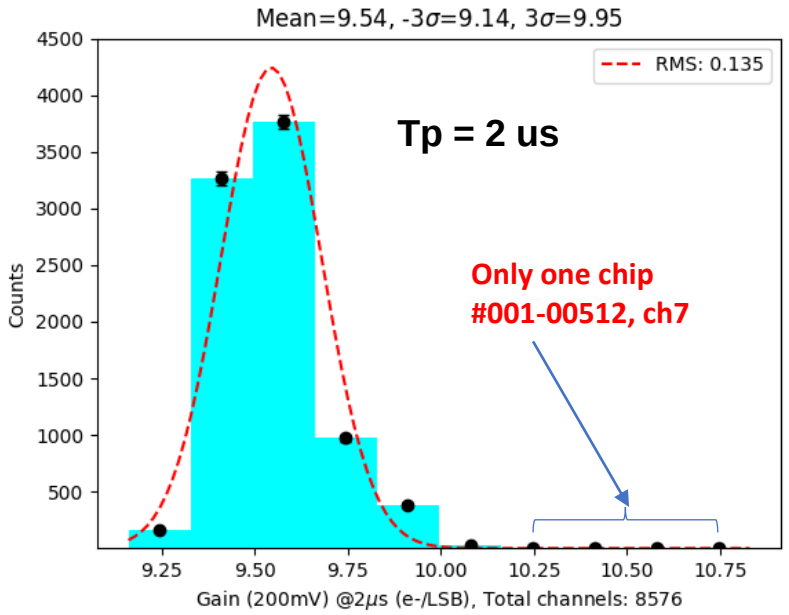


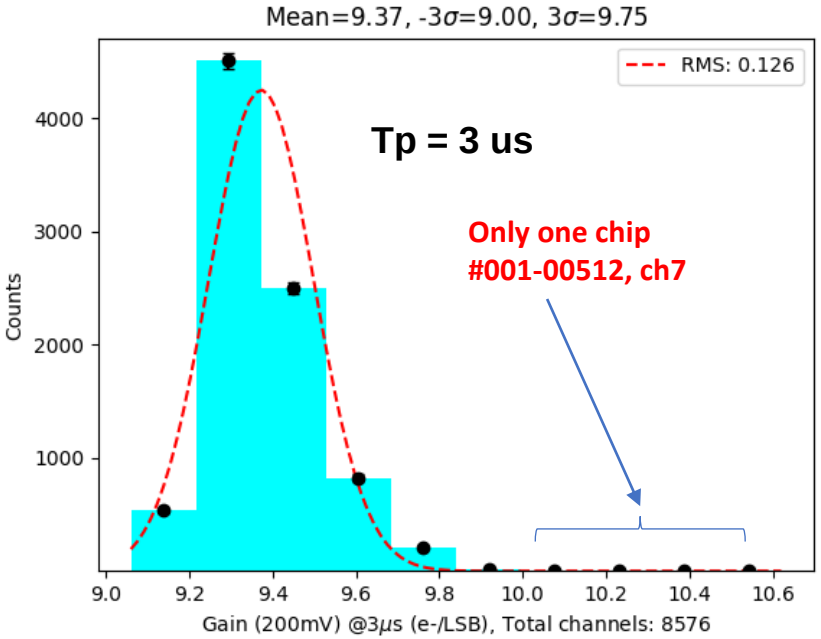


Gain measurement (BL=200mV) for each channel





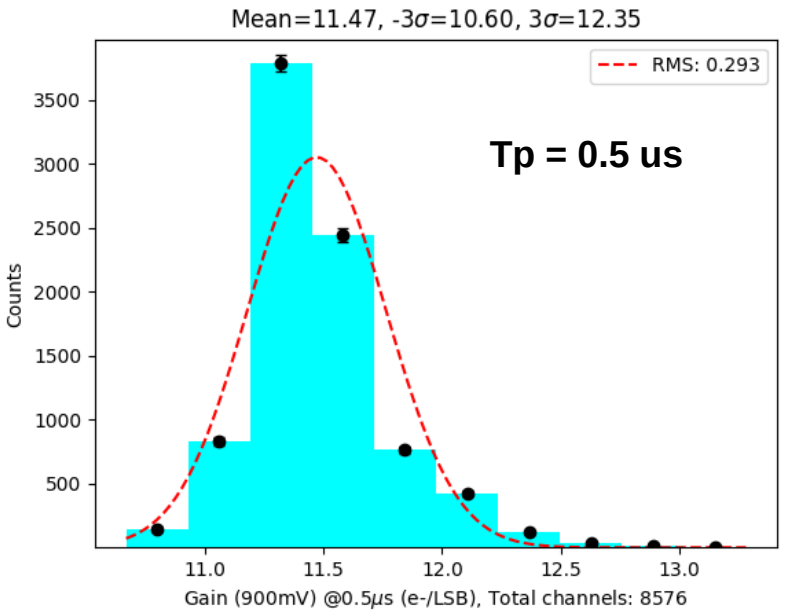


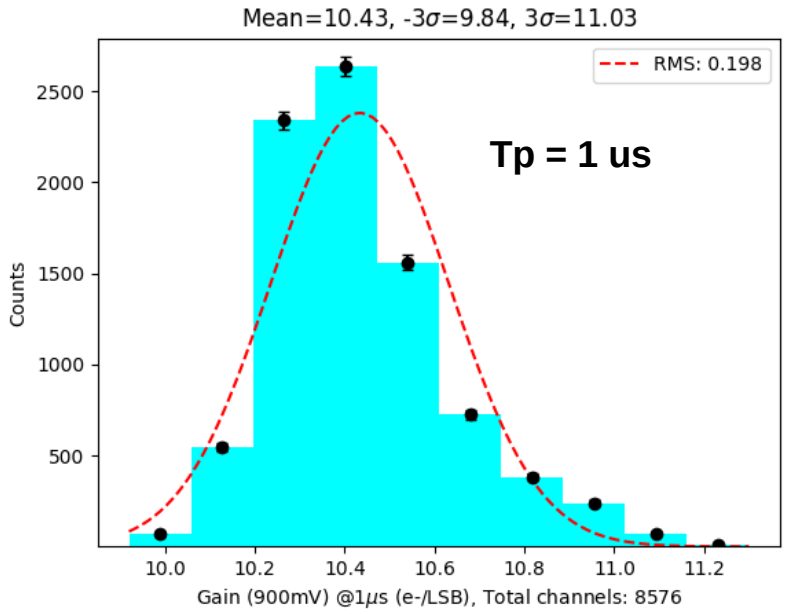


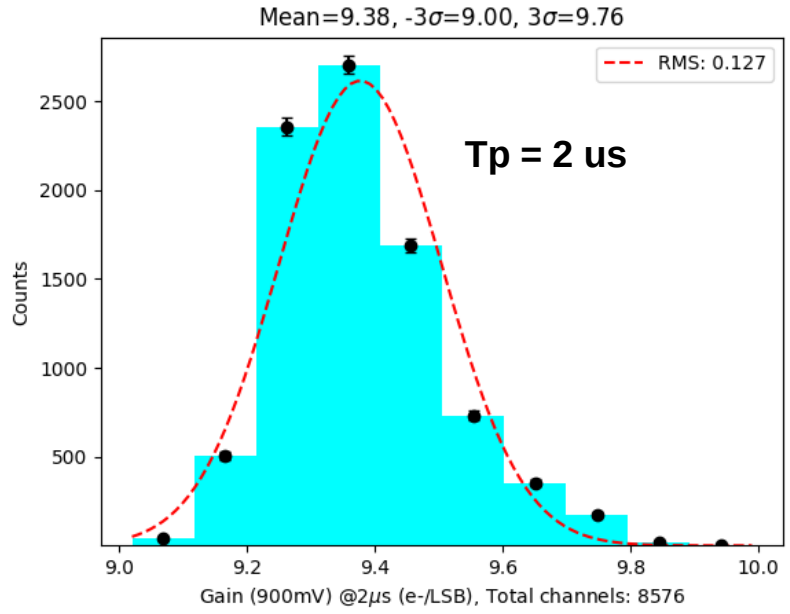
One "outlier" (pass the test) corresponds to one channel while the tther test parameters of this chip look reasonably good.

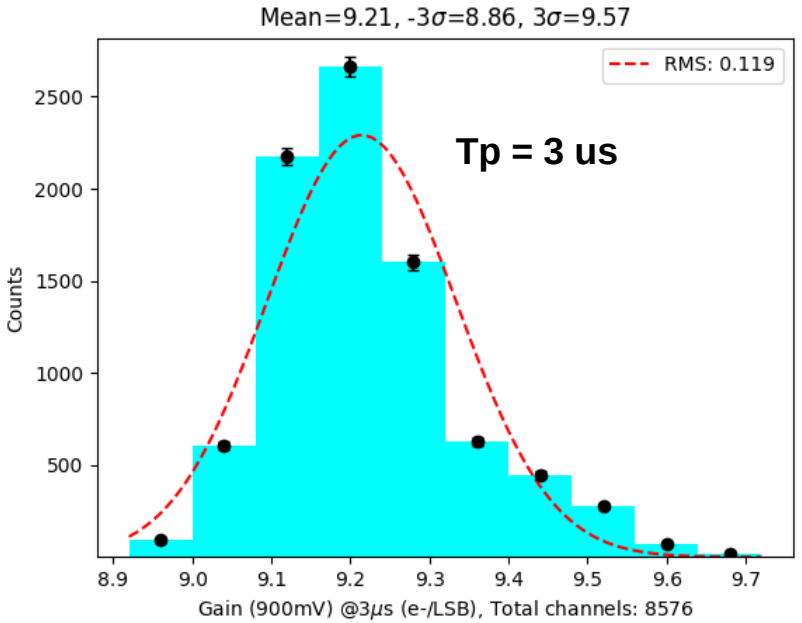
Gain 200mV (e-/LSB)	Mean	SD
Tp=0.5us	10.8	0.2
Tp=1us	10.6	0.2
Tp=2us	9.5	0.1
Tp=3us	9.4	0.1

Gain measurement (BL=900mV) for each channel







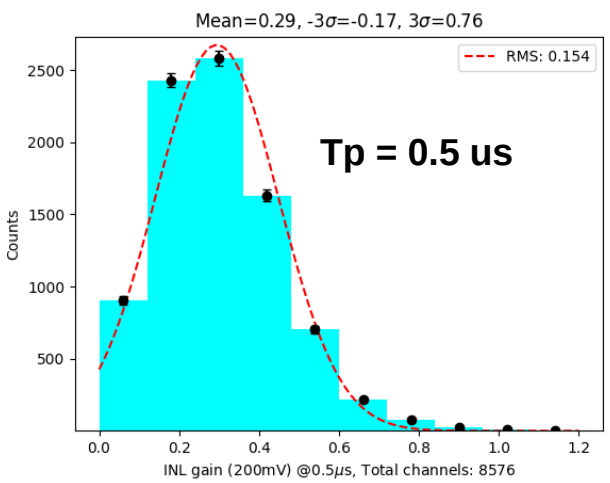


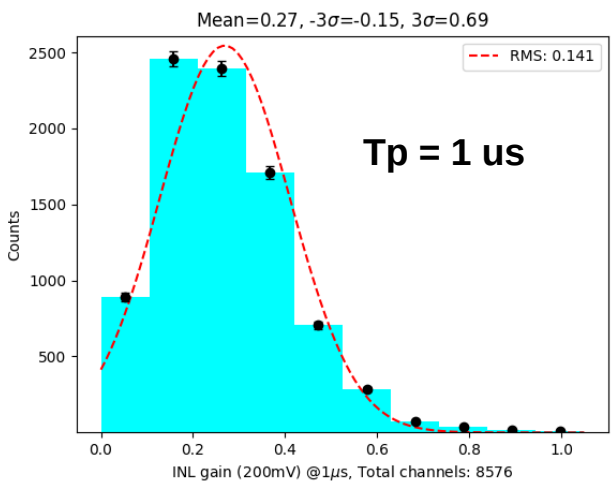
Gain 900mV (e-/LSB)	Mean	SD
Tp=0.5us	11.5	0.3
Tp=1us	10.4	0.2
Tp=2us	9.4	0.1
Tp=3us	9.2	0.1

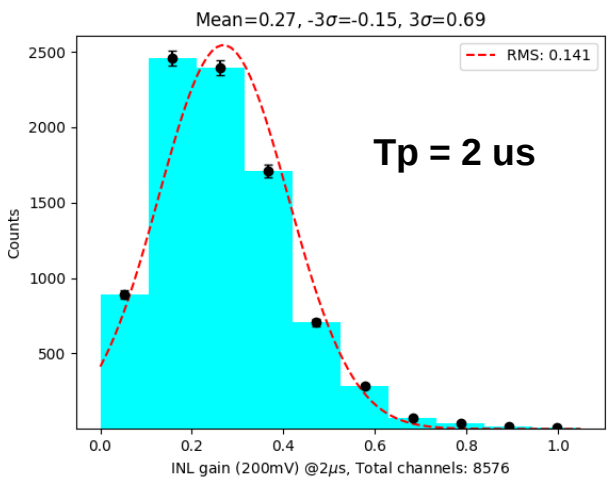
Consistent between BL=200mV and BL=900mV measurements

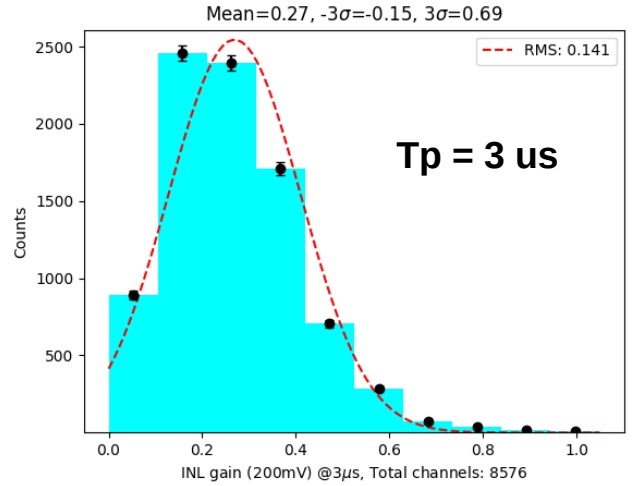
Full chain (LArASIC+ColdADC) gain linearity measurement for each channel

BL = 200 mV [INL = (0.3+-0.1)%]

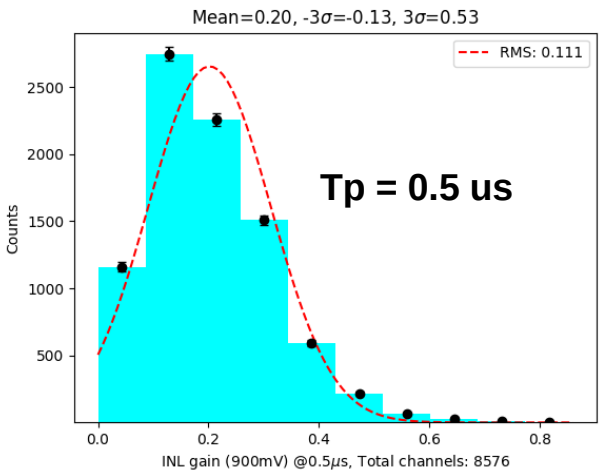


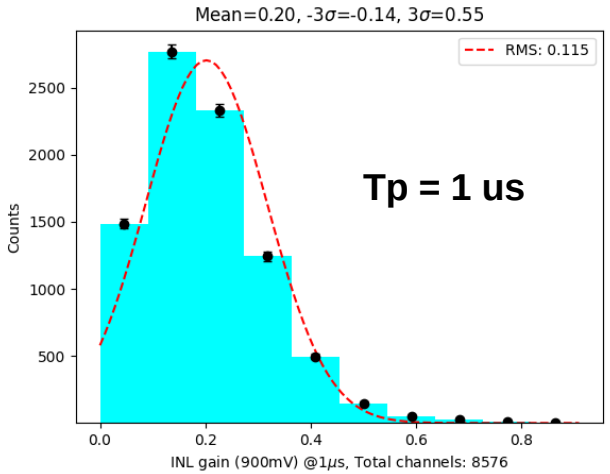


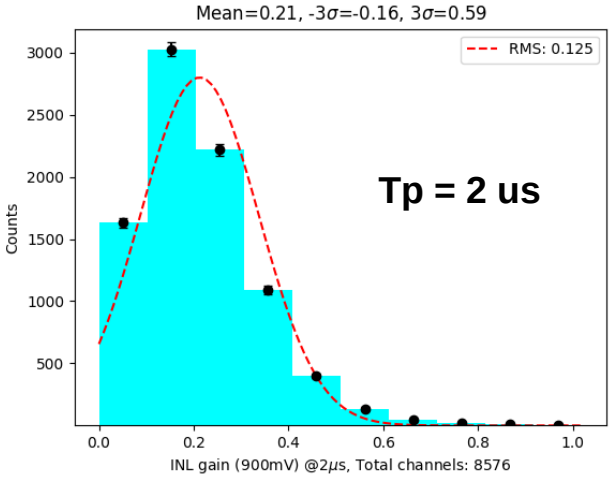


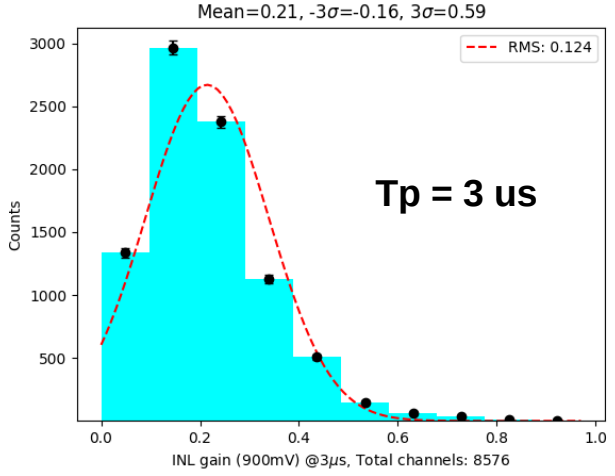


BL = 900 mV [INL = (0.2+-0.1)%]

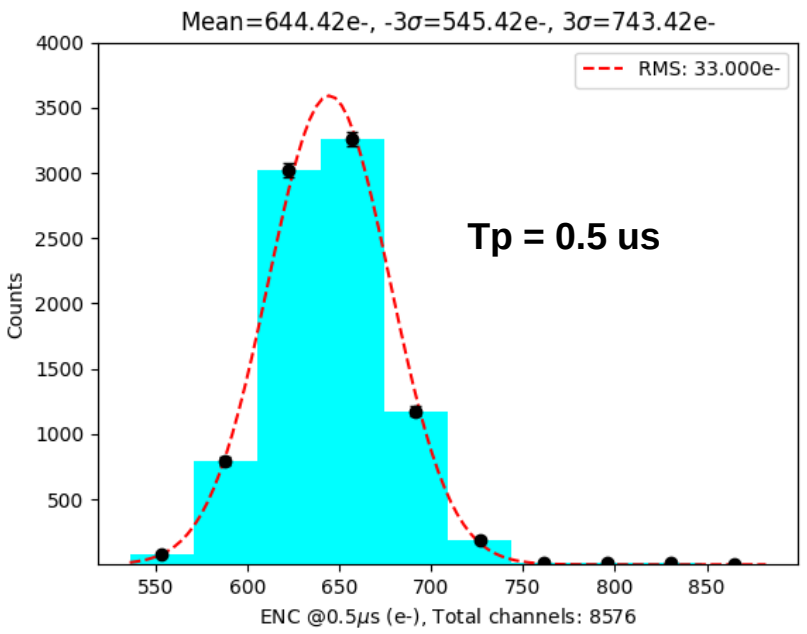


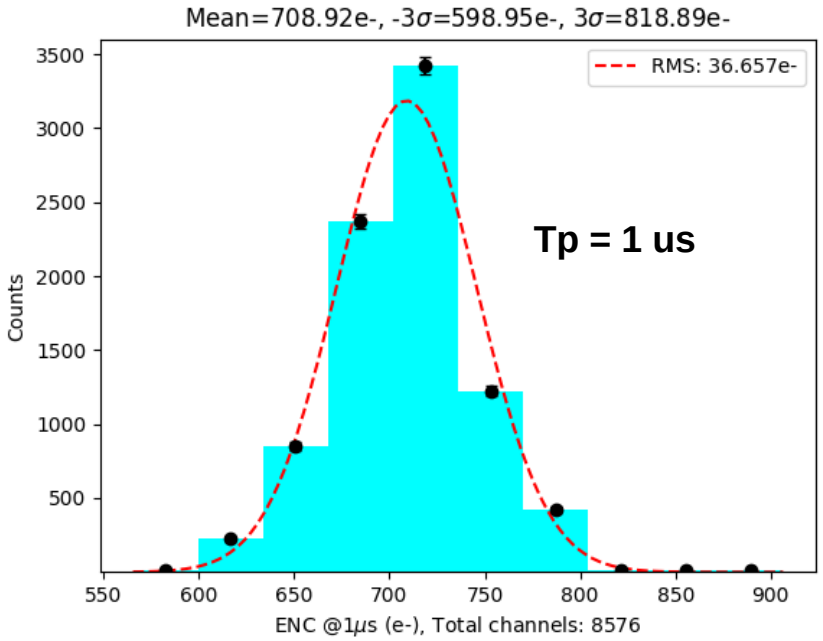


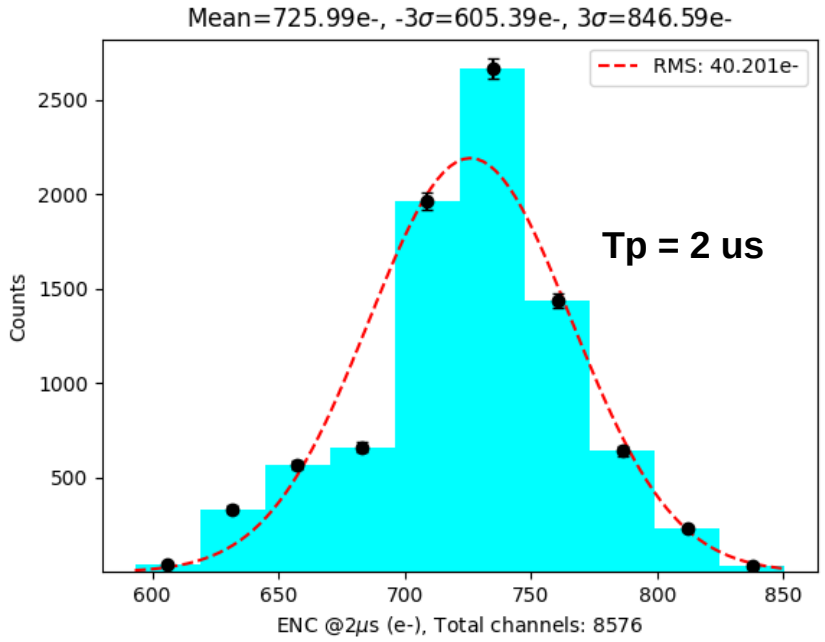


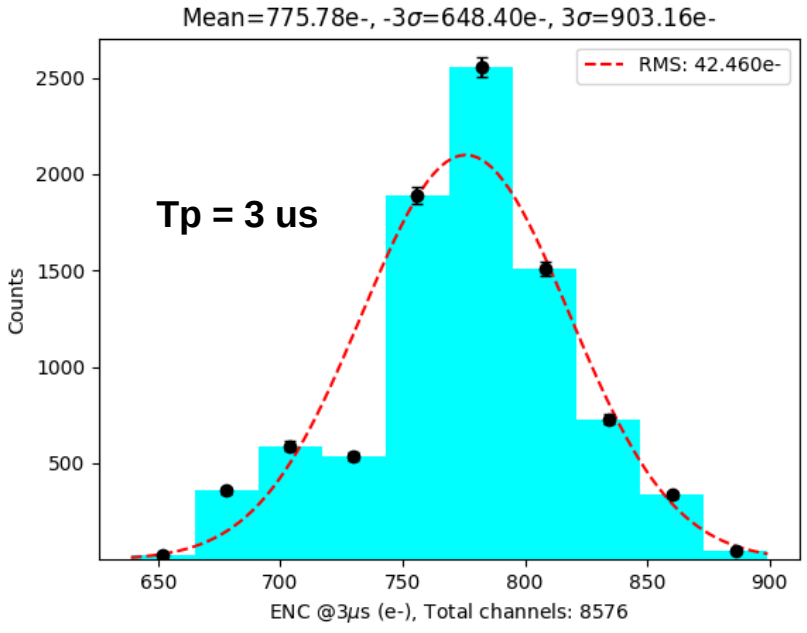


Noise level measurement for each channel



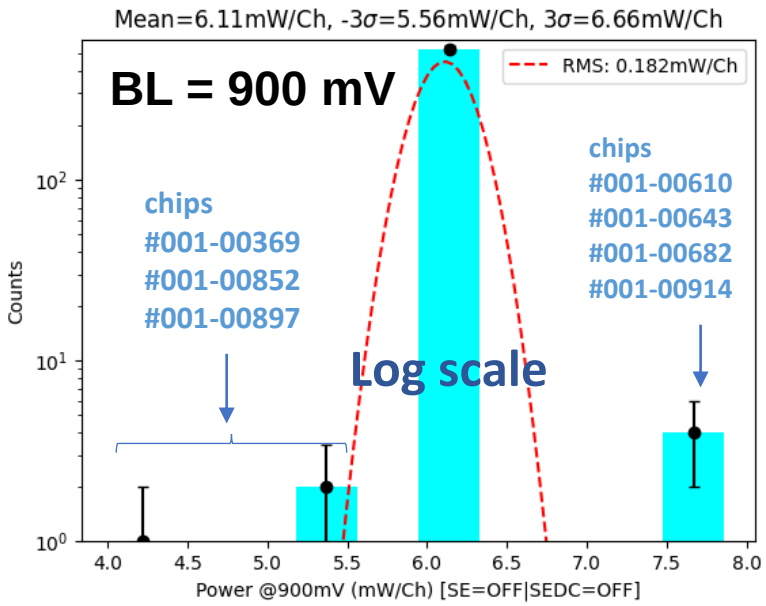


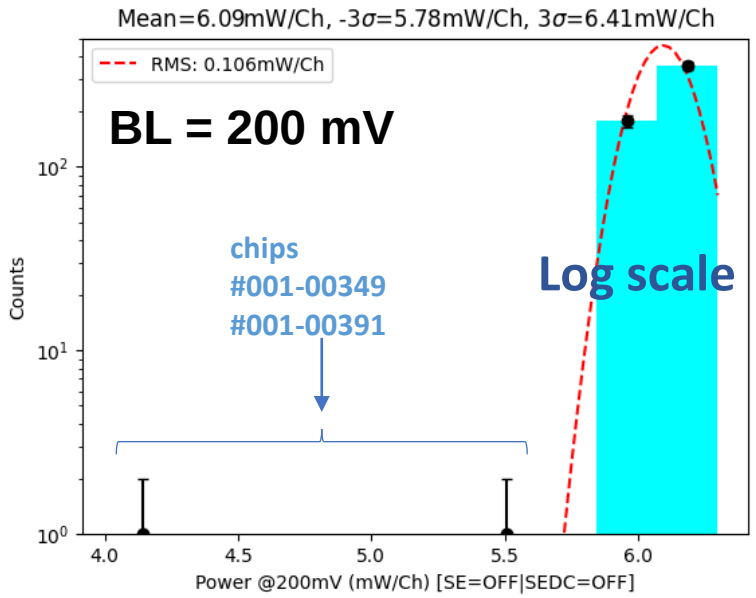


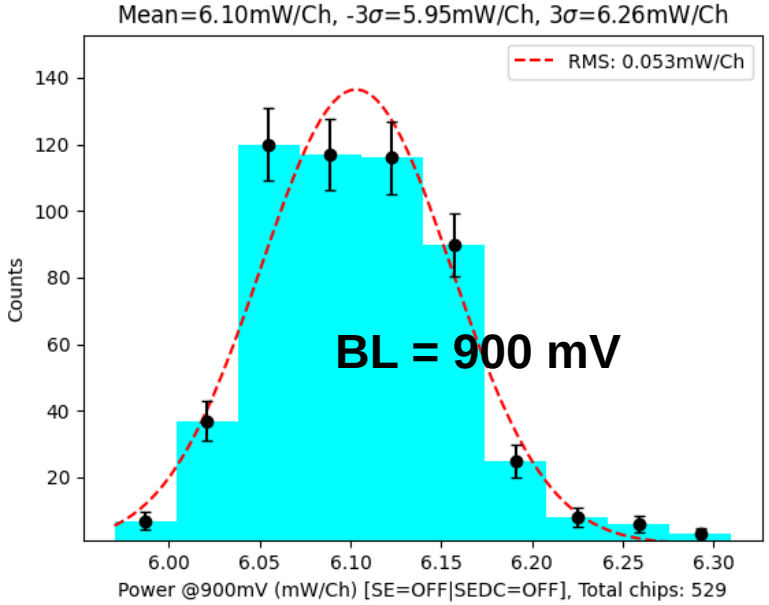


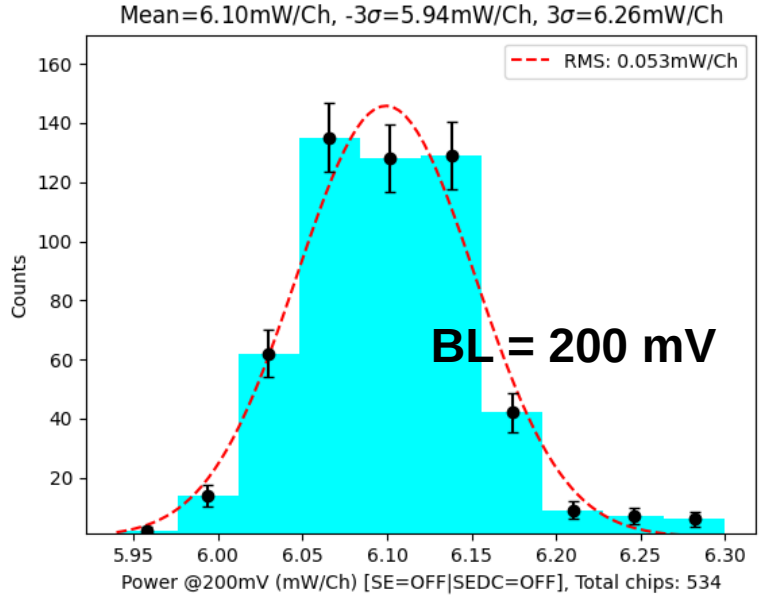
ENC (e-) when C_d = 0 pF	Mean	SD
Tp=0.5us	644	33
Tp=1us	709	37
Tp=2us	726	40
Tp=3us	776	42

Power measurement (buffer OFF)









Power (mW/Ch)	Mean BL=200mV/BL=900 mV	SD BL=200mV/BL=900 mV
All 536 chips	6.1/6.1	0.2/0.1
'Outliers' removed	6.1/6.1	0.05/0.05

Current "power" is kind of an average from all three power rails VDD, VDDO, and VDDP.

- Loose "good chip criterion"
- Is it good to break it into each power rail?

LArASIC Test Overall Summary

Batch	#wafers	#P5B	#P5	Pkg house	SN	#tested RT	#tested LN2	RT yield	LN2 yield
0	6 engineering	~1800	~1800	GTK	none	1786	815	98.9%	99.4%
1	3 engineering	~900	~900	ASE	001-xxxxx	370 (BNL)	32	99.5%	93.75%*
						540 (LSU)	-	99.3 %	-
2	25 production	~7500	~7500	ASE	002-xxxxx	145 (BNL)	53	97.2%	75.47%*
						54 (LSU)	-	100%	-
1.1	3 engineering	~900	~900	ASE	0011-xxxxx				

*Chips that failed LN2 test need to be retested, actual yield expected to be higher

- Batch 0: All P5B tested at RT and used in FEMB production of ProtoDUNE-HD/VD
- Yields from a couple of hundred P5B chips from batches 1 and 2 will provide important information for developing the production QC test strategy for cold test

Summary and near-term plan

- LSU achieves >99% passing rate of LArASIC RT test, consistent with BNL test result
  - 4 bad chips identified in the first 540 chips
  - A few “outlier” chips found in power measurement.
- Test parameter distributions look good and the mean/variance are consistent with BNL results
- Continuation of LArASIC RT testing using DUT board
- Get prepared for the FD1/FD2 LArASIC QC testing campaign using the new DAT board