DAPHNE Test at Milano-Bicocca

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Topics

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- DAPHNE DMEM HD HPK SNR test
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 - SNR results for different undershoot mitigations configurations.



Undershoot mitigation



Undershoot mitigation – Input impedance





Undershoot mitigation – Input impedance



 At around 80KHz, we have a valley in the input impedance value, causing a mismatch at those frequencies. This mismatch in term causes those components to be seen with larger amplitude at the AFE input.



Undershoot vs R_b



• Increasing the value of R_b decreases the undershoot but increases the recover time of the signal.



Parameters $C_{coldamp}$, C_{daphne} and R_b





- *C_{coldamp}* is the capacitor that decouples the bias and trim voltages in the cold amplifier's feedback loop. Operates at cold.
- *C_{daphne}* capacitor that decouples the bias and trim voltages from the transformer primary.
- R_b is the termination resistor connected at the center tap of the transformer's primary and secondary.
- These studies concluded that the contribution of *C*_{coldamp} to the undershoot behavior is not significant.





- R_b and C_{daphne} dominates the undershoot response, yielding up to around 17% points reduction when $R_b = 25\Omega$ and $C_{daphne} = 1000 nF$.
- For now on, C_{daphne} will be referred as C_{in} .



Transformers



- We propose to change DAPHNE's H1164NLT transformer, which has a center tap connected to adyacents channels, to a transformer which has independent center taps.
- The main reason is to avoid any excess crosstalk between adyacent channels sharing these center taps.
- The HX5004ENL was proposed as a candidate.



HX5004ENL

-0 24 MCT1

-0 23 MX1+

-0 22 MX1-

-0 21 MCT2

20 MX2+

-0 19 MX2-

-0 18 MCT3

-0 17 MX3+

-0 16 MX3-

-0 15 MCT4

o 14 MX4+

-0 13 MX4-

Undershoot Measurements



- On a small perforated board, we replicated DAPHNE's input analog circuitry to measure different configurations using the HX5004ENL transformer.
- The HD (HD ganging scheme) coldamp was used, triggering with an LED 48 FBK SiPMs.
- The output is 50 Ω terminated to the oscilloscope. (50 Ω R_o)



Undershoot Measurements



- Severeal thousands waveforms were acquired with different R_b values and $C_{in} = [100 \text{nF}, 1 \text{uF}]$.
- The mean waveform was calculated, and from the positive peak amplitude waveforms, the undershoot value can be extracted.





- According to the simulation, the minimum R_b value for the undershoot should be around 25 Ω .
- Measurements on the other hands, puts the minimum value around 39 Ω to 50 Ω .
- Therefore, $R_b = 47\Omega$ was selected to test with DAPHNE.



Measurements – DAPHNE V2A



- On DAPHNE V2A, we removed the H1164NLT transformer, and we replaced it with the HX5004ENL.
- Only 1 channel is available for readout (CH32).
- Values tested are $R_b = [0\Omega, 47\Omega]$ and $C_{in} = [100nF, 1uF]$.
- We tested $R_b = 47\Omega$ and $C_{in} = [100\text{nF}, 1\text{uF}]$ in CH32, and $R_b = 47\Omega$ and $C_{in} = 100\text{nF}$ in CH0 (unmodified).



Measurements – DAPHNE V2A



- HD ganging scheme and DMEM HD waveforms were acquired.
- As expected, we see a reduction in the undershoot behavior. What was not expected is the large contribution of the AFE AC coupling.



Measurements – DAPHNE V2A



- Inspecting the undershoot behavior, we can see that changing the R_b value from 0Ω to 47Ω does no affect the recovery time of the signal. The shape although changes, eliminating the positive overshoot.
- Changing C_{in} from 100nF to 1uF, reduces the undershoot but affects the recovery time.
- Here, considering a 5% settling condition, the latter configurations yields the best results (4.4 μs 275 ticks). Considering for example, 1%, the signal takes 12.3 μs (769 *ticks*) to settle with $C_{in} = 100 nF$ and 27 μs (1688 ticks) to settle with $C_{in} = 1 uF$.



Crosstalk



- For the crosstalk measurements, we injected a 100kHz sinusoid at ch0 of AFE0. The center tap was disconnected in the DAPHNE side, while it was grounded in the transmission side. Channels from 2 to 7 were not modified.
- A significant crosstalk of around -6.93dB was observed in this configuration between CH0 and CH1, which share the center tap.
- Negligible crosstalk of -78dB was observed in channels 2-7



Discriminator module (self-trigger)



Discriminator module











FPGA filter waveform





FPGA Filter

 $y[n] = b_1 x[n] + b_2 x[n-1] + b_3 x[n-3] + (-d_1) y[n-1] + (-d_2) y[n-2]$



- The figure on the left is the schematic of the implementation of the IIR filters HPF and Mov. Avg.
- Right now, the coefficients values are fixed but they can be easily modified to be configurable. Allowing the user to choose any king of filtering strategy if it is a second order IIR.
- The module has been programmed in order to use the least amount of DSP units (5), by setting the length of the input to 25bits (16 for AFE data and 9 for decimals) and 18bits for coefficients (3bits including sign and 15 bits for decimals)



FPGA Resources



DAPHNE GUI interface

| ~ | DAPHNE GUI TOOL | - 🗆 😣 |
|--|---|--------------------------|
| Tools Configuration | | |
| Messages | | |
| DAPHNE GUI V2_01_01 Author: Ing. Esteban Cristaldo, MSc | | |
| Communications | Commands | |
| Select Serial Port | Channel: 0 - AFE: 0 - All AFEs GET CONFIG SET CONFIG | RD FPGA |
| ttyS0 👻 Refresh | Bias Voltage Gain Active Termination LP | F |
| BaudRate: 921600 \$ Connect Disconnect | Value: 0 + LNA: 12dB • Enable Impedance Trim: 0 + Integrator (HPF) Impedance 50 • ADC Format Channel Offset LNA PGA PGA 24dB • ADC Format | ut-off freq: 10 Mhz 🔻 |
| Send Raw Command | Value mV All AFE Gain Apply V Offset binary | MSB First |
| | V GAIN I NA Clamp PGA Cla | mp |
| Send | | |
| Take Multiple Waveforms | | -2 dBF * |
| 1 A Enable | Sweep channel orrset Eth | iernet |
| Mult. CH Cont. | Start value: 0 \Leftrightarrow End Value: 0 \Leftrightarrow Step: 0 \Leftrightarrow Enable | Enable |

| | AFE configuration | | \otimes |
|--|-------------------|------------------|-----------|
| AFE Configural | tion | | |
| Digital Block | | | |
| Digital High Pass Filter | К: 9 🗘 | FPGA Filter | |
| Digital Gain | Gain: 0,00 | *Output: 0 | |
| OFFSET remover | | | |
| | | | |
| Low Frequency Noise | Supressor | | |
| * Output Values: 0: Filt. Ped. Rec. 1: Mov. Mean. 2: Filt. Ped. Rem. 3: Unfiltered | | ● <u>C</u> ancel | |
| ~ | Dialog | 8 | |
| Trigger C | onfiguration | | |
| | Johnigaración | | |
| Source | Channel | Level | |
| Source Internal External Software | Channel | Level | |
| Source Internal External Software | Channel | Level | |
| Source Internal Software Pre Trigger *Multiplier: 0 | Channel | Level | |







Integration filter for Hamamatsu waveform

- Using the same architecture used for the "HPF" filter, we approximated a $\frac{\mu s}{m}$ ving average filter of 25 samples.
- The integration is performed by the filter and is given by the peak value.
- The peak value is extracted, and a histogram can be performed.
- Then, after calibration, we can trigger at any point in the histogram (e.g., 1.5 P.E.) just by setting a threshold in the integrated waveform (green).
- In the FPGA implementation, we multiply by a factor of 2 to reduce the quantization error.



Zero-crossing detector



- To avoid the time walk jitter in the threshold flag, we • use a zero-crossing detector.
- The input signal is inverted and delayed by a fixed ٠ number of samples (15 in this case).
- The input signal and the delayed are summed. The ٠ zero crossing is detected, and the flag is asserted.
- The final trigger signal is the logical and of the ٠ threshold flag and the zero-crossing flag.





Discriminator processor hardware simulation



- The HDL simulation of the trigger processor hardware is done using RAW daphne data (i.e. unfiltered data).
- Using the approximated filter, the module is calibrated with different thresholds.
- The result of the simulation is the orange histogram, where one can see that the trigger module cuts most of waveforms that have an integral value below the corresponding discriminator threshold.



Receiver Operating Characteristics Curve



- Performing multiple HDL simulations, with different threshold values, the true positive and false positive rates can be calculated. ٠
- For this simulations specifically, a tolerance of 1.2 ADU was included. (i.e the lower limit where a signal can still be considered a valid threshold). ٠
- In the figure to left, the ROC curve, the closer to the left upper corner, the better the discrimination process. ٠
- A tradeoff has to be considered between true positive rate and false positive rate, and the tolerance. ٠



Receiver Operating Characteristics Curve







Acquired data with the Discriminator – FBK HD system



- The discriminator module was tested with the FBK HD system with an SNR around 4.2.
- The system was calibrated and the threholds were set to positions corresponding to 2.5 P.E ; 1.5 P.E. and 1 P.E.
- We can see from the histogram that the discriminator is able to cut almost all waveforms below the threshold, even as low as 1P.E.



DMEM HD HPK tests



DMEM HD HPK tests





- The DMEM HD test was performed with the latest revision of the cold amplifier addresing the issue of the oscilations seen at the coldbox test.
- The feedback resistor was set to $1.2K\Omega$ (390 Ω for the HD ganging).
- 4 HPK flexes boards @ 44.5V (45% PDE), 45V (50% PDE) and 47V* were tested for 1000P.E and 2000P.E. dynamic range.





- The calibration process consist in setting the overall amplification of the AFE to allow for either 1000P.E. or 2000P.E. dynamic range independently of the input, which is fixed. (Setting the correct amplitude for a single P.E.)
- Given that the LNA and PGA gains are fixed to 12dB and 24dB for best noise performance, the only parameter that can be configured is the VGAIN value (voltage-controlled attenuator).



VGAIN to obtain the required dynamic range

- To obtain the required VGAIN to achieve a specific dynamic range (DR), we proceeded as follows:
 - 1. For a PDE configuration, in this case 45%, we took the measured DR value at a high VGAIN configuration (0,3V). In this example the value is 216.
 - 2. With this value, we find that the average single P.E. is

$$A_{1P.E.(0,3V)} = \frac{2^{14}}{216} \approx 76 \,ADU$$

For VGAIN = 0.3V (27,39dB)(23,4).

3. Then, the target amplitude for a single P.E. to obtain 2000 P.E. (for example) dynamic range is

$$A_{2000P.E.DR} = \frac{2^{14}}{2000} \approx 8 \,ADU$$

4. Then, the desired GAIN to obtain a single P.E. of amplitude 8 ADU is $A_{20000} = 8 + G_{0.2V} = 8 + 23.4$

$$G_{1P.E.(8ADU)} = \frac{M_{2000P.E.DR} + G_{0,3V}}{A_{1P.E.(0,3V)}} \approx \frac{G + 23,1}{76} \approx 2,48(7,89\text{dB})$$

These GAIN values are referenced to table 16 (AFE5808 datasheet page 57), for the specific configuration (LNAG = 12dB, PGAG = 24dB).



VGAIN to obtain the required dynamic range

Taking the values of GAIN of table 16 at the given configuration, we made a fit to extract the VGAIN value for the desired GAIN = 7,89dB, calculated previously.



 $VGAIN_{1P.E.(8ADU)} = Fit(7,89dB) \approx 0,86V$





DMEM HD SNR for different DAPHNE input configurations - DR: 1000P.E.

The SNR values for the case of D.R. = 1000P.E. ranges from 5 to 7.38. In the case of D.R. = 2000 P.E. the SNR ranges from 4.04 to 5.08. with ٠ increasing Vbias votages.

- The SNR reduction can be explained by the fact that at D.R. = 2000 P.E., the 1/f noise dominates (higher attenuation is required) to which the ٠ DAPHNE filters are more susceptible. (this noise is not dependant on VGAIN value).
- There is not significant evidence to say a configuration has better SNR response. We will repeat these measurements with the FBK flexes.





 $C_{in} = 100nF$; $R_b = 0\Omega - 1000 P.E. -V_{bias} = 44.5V - 45\%$ PDE





 $C_{in} = 100nF$; $R_b = 0\Omega - 1000 P.E. -V_{bias} = 45V - 50\% PDE$





 $C_{in} = 100nF$; $R_b = 0\Omega - 1000 P.E. -V_{bias} = 47V - ** %PDE$







 $C_{in} = 100nF$; $R_b = 0\Omega - 2000 P.E. -V_{bias} = 44.5V - 45\%$ PDE

















 $C_{in} = 100nF$; $R_b = 0\Omega - 2000 P.E. -V_{bias} = 47V - ** %PDE$







 $C_{in} = 100nF$; $R_b = 47\Omega - 1000 P. E. -V_{bias} = 44.5V - 45\%$ PDE





 $C_{in} = 100nF$; $R_b = 47\Omega - 1000 P.E. -V_{bias} = 45V - 50\% PDE$









 $C_{in} = 100nF$; $R_b = 47\Omega - 2000 P.E. -V_{bias} = 44.5V - 45\%$ PDE







 $C_{in} = 100nF$; $R_b = 47\Omega - 2000 P.E. -V_{bias} = 45V - 50\%$ PDE







 $C_{in} = 1 u F$; $R_b = 47 \Omega - 1000 P. E. -V_{bias} = 44.5V - 45\% PDE$





 $C_{in} = 1 u F$; $R_b = 47 \Omega - 1000 P. E. -V_{bias} = 45V - 50\% PDE$





 $C_{in} = 1uF$; $R_b = 47\Omega - 1000 P.E. -V_{bias} = 47V - ** %PDE$





 $C_{in} = 1 u F$; $R_b = 47 \Omega - 2000 P. E. -V_{bias} = 44.5V - 45\% PDE$







 $C_{in} = 1 u F$; $R_b = 47 \Omega - 2000 P. E. -V_{bias} = 45V - 0\% PDE$







 $C_{in} = 1uF$; $R_b = 47\Omega - 2000 P.E. -V_{bias} = 47V - ** %PDE$



