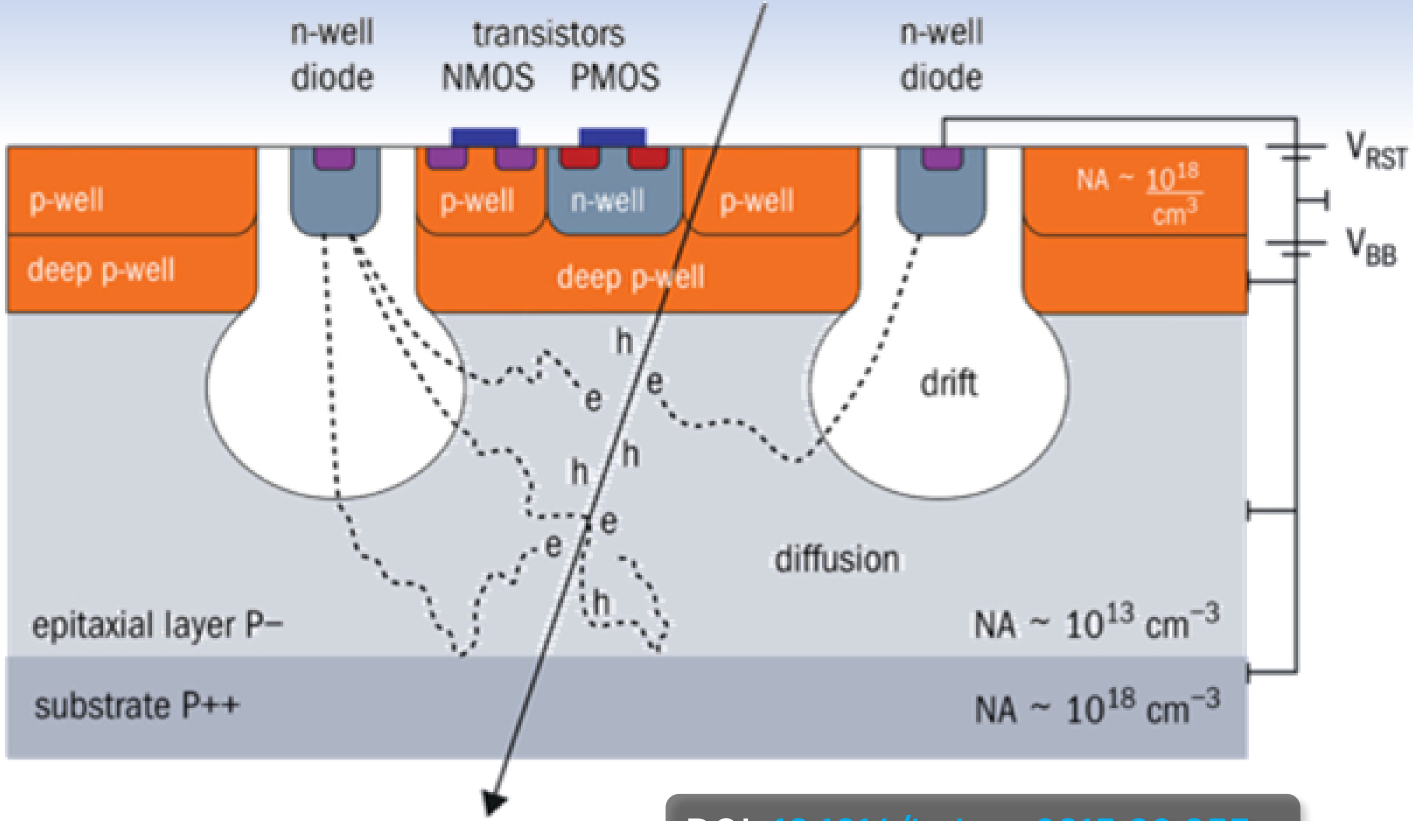
MAPS for (next) HEP tracking

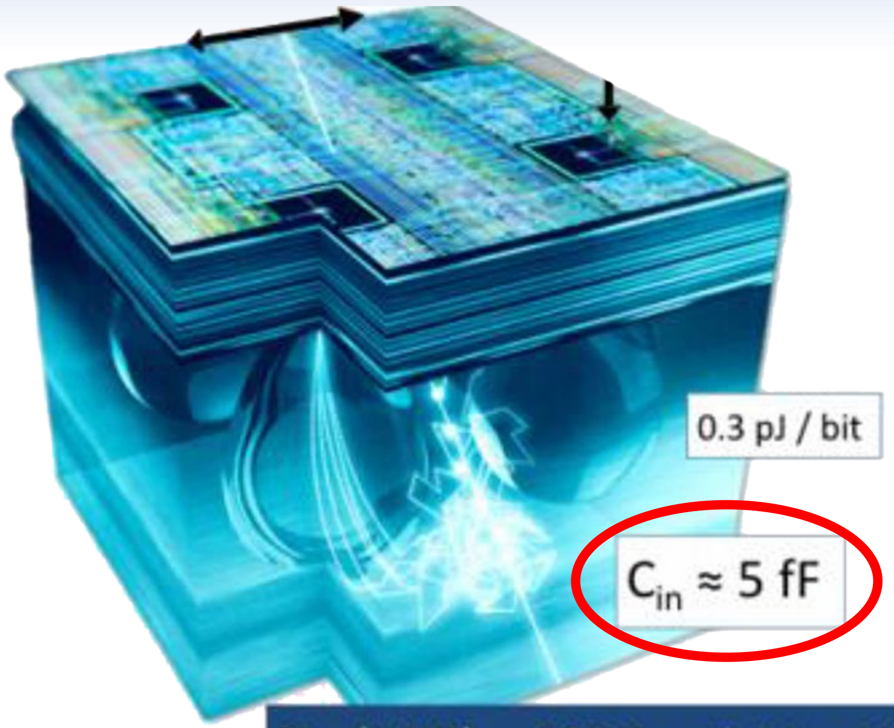
- Introduction and disclaimer
- Ongoing R&D
- Next step R&D

P. Giubilato, Padova University and INFN, CERN

Monolithic are well known



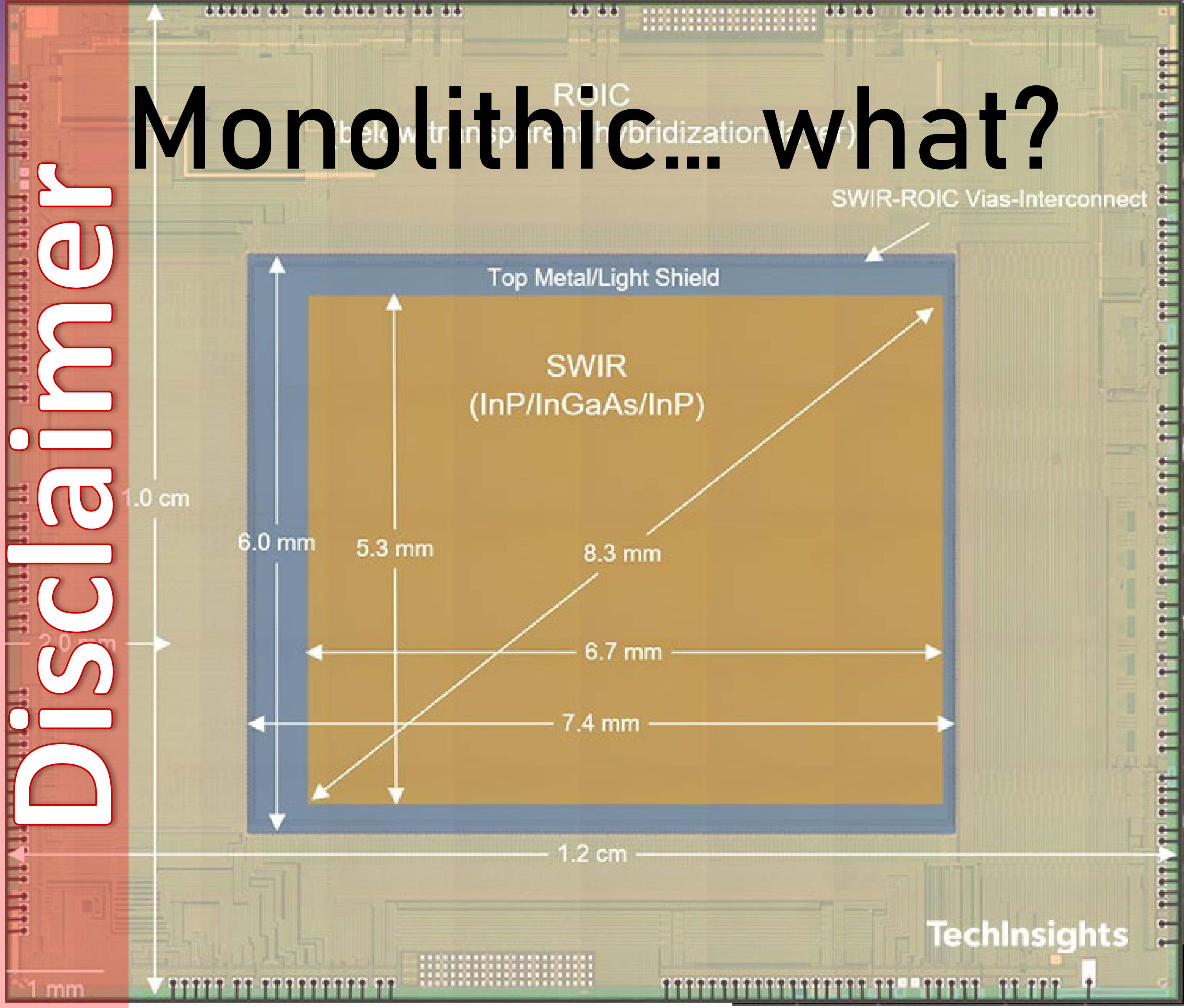
DOI: 10.1016/j.nima.2015.09.057

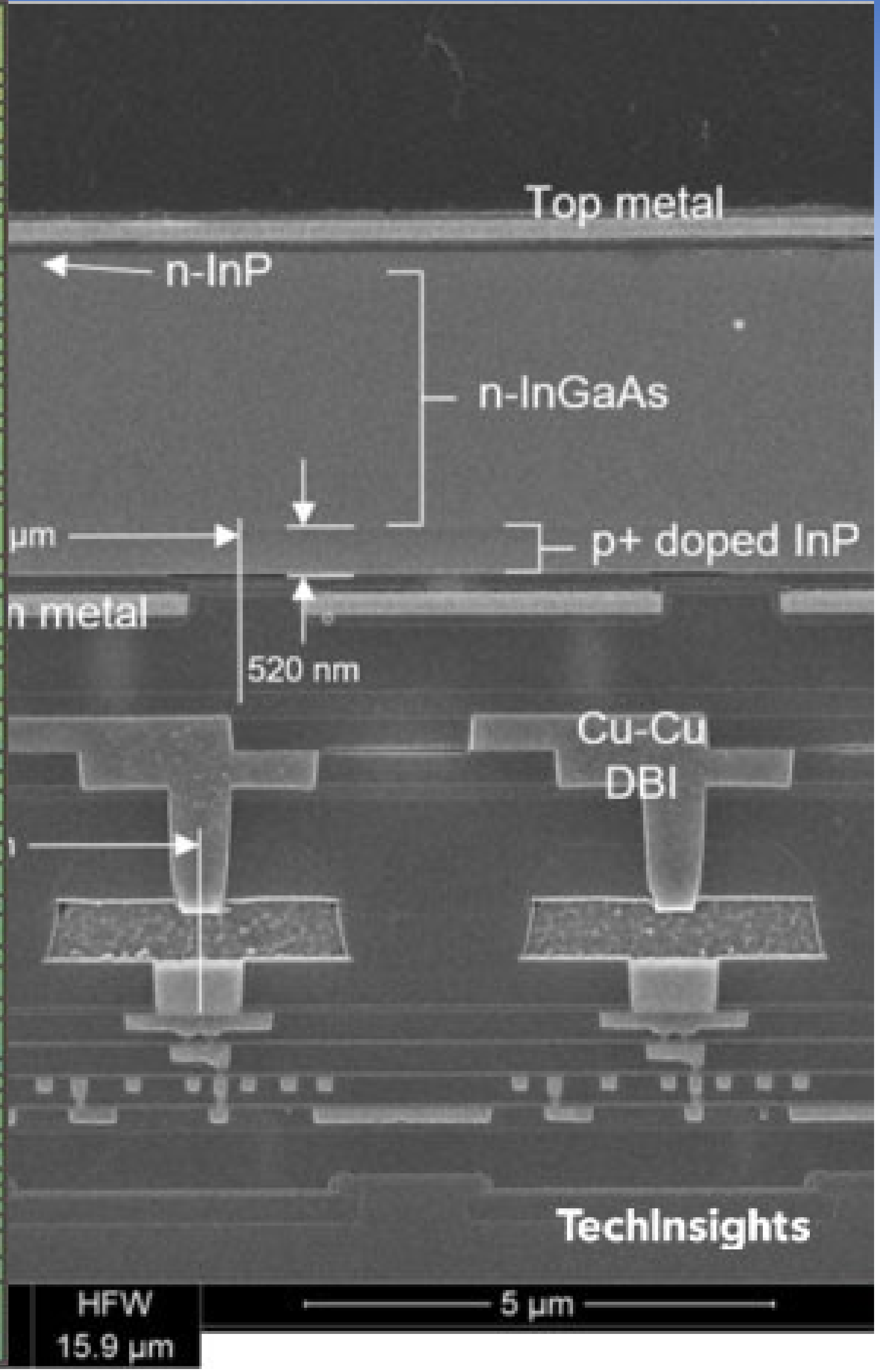


Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV

Monolithic… what?

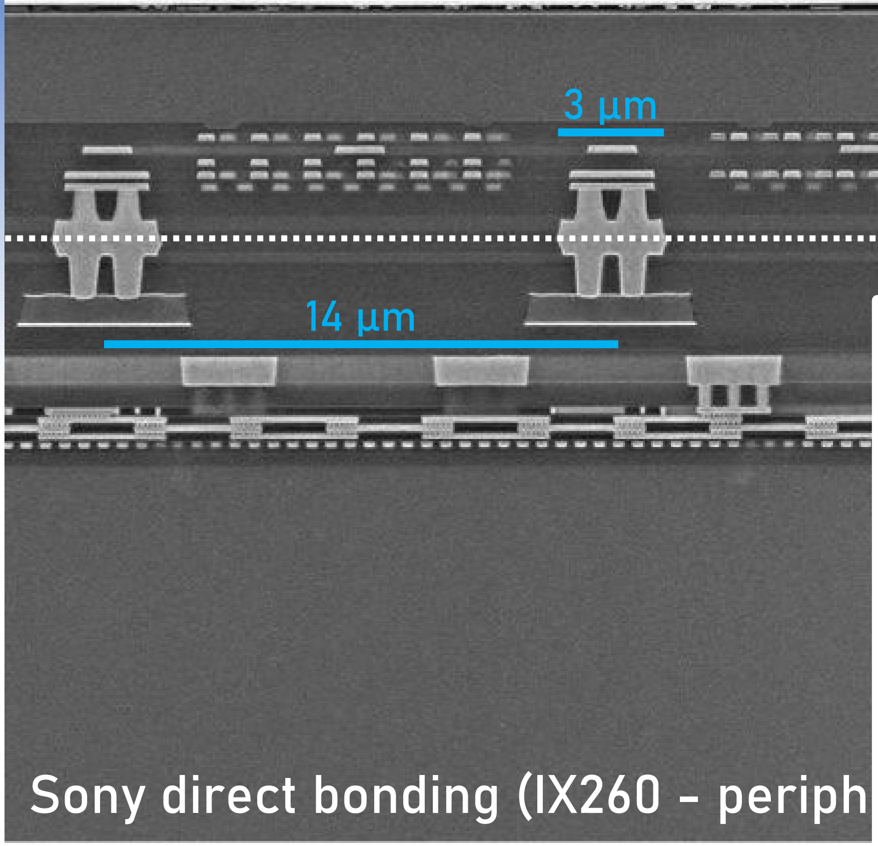
Disclaimer

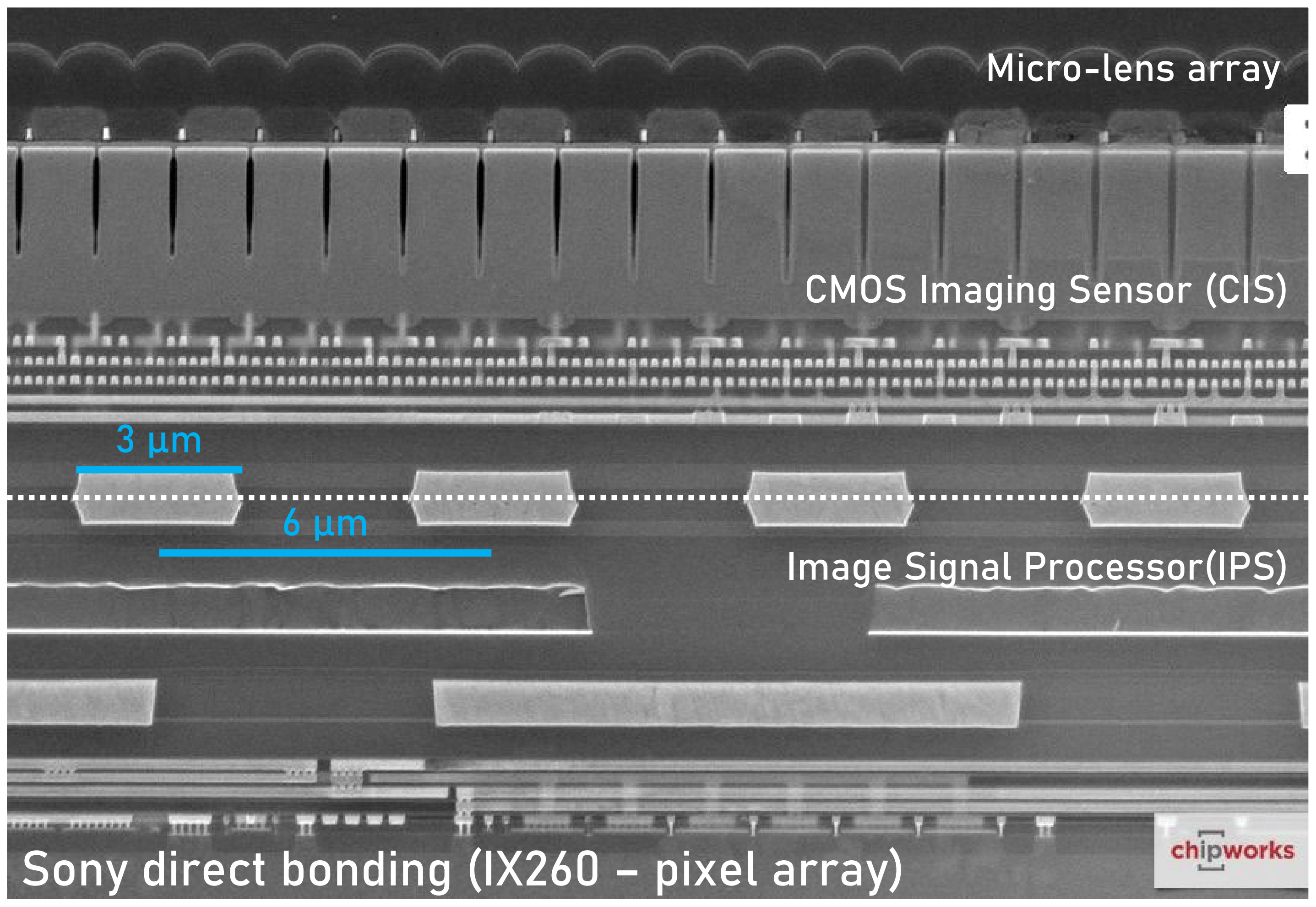




Disclaimer

Difference is shrinking



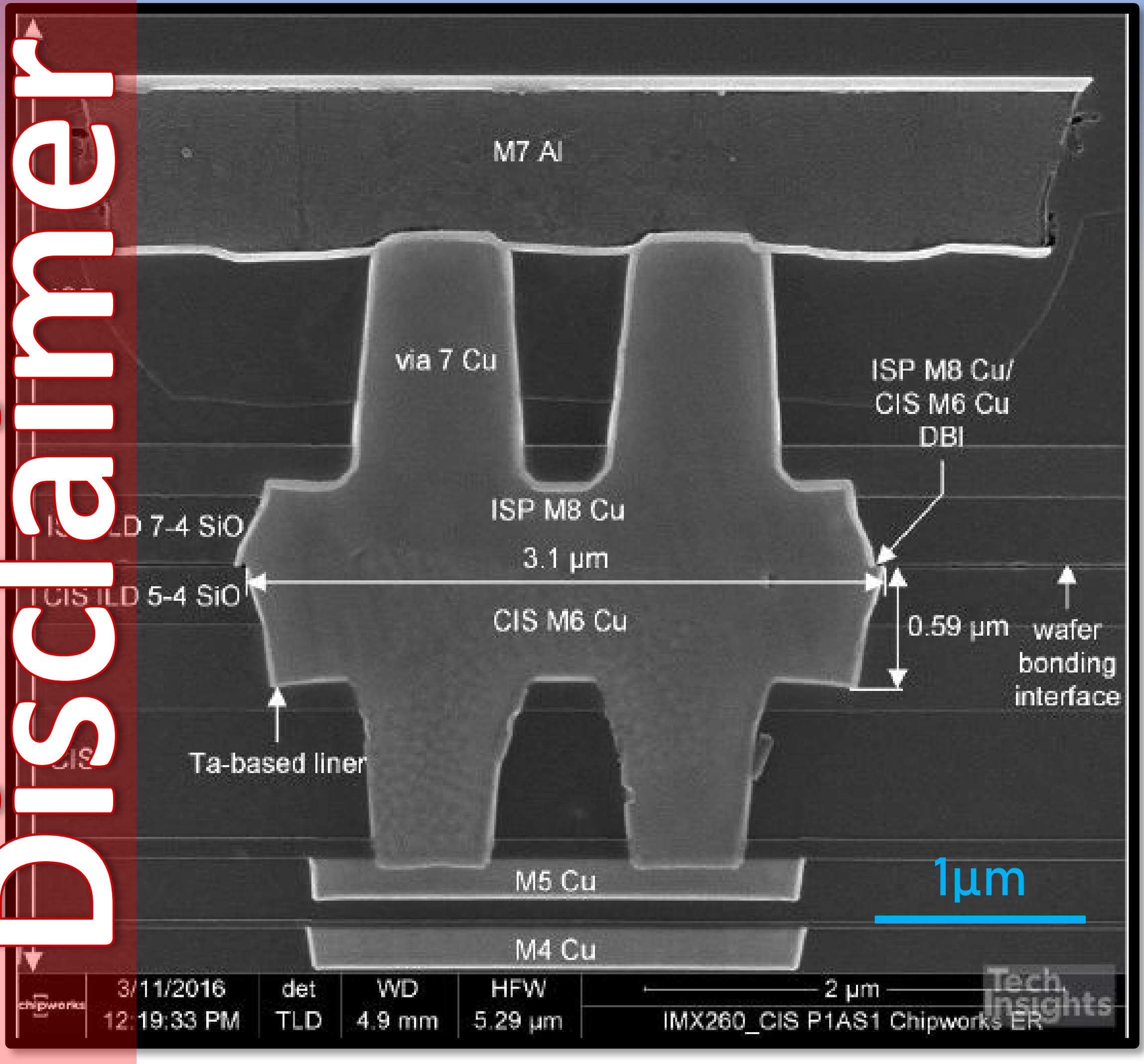


DOI: 10.1109/EDTM.2019.8731186

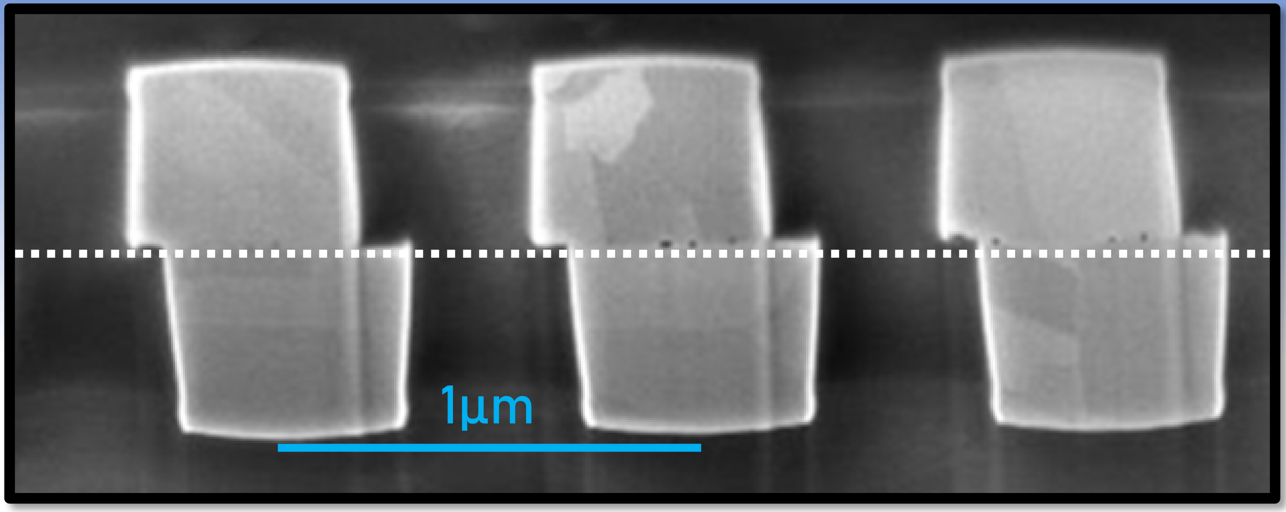
Difference is shrinking – 1 µm pitch possible

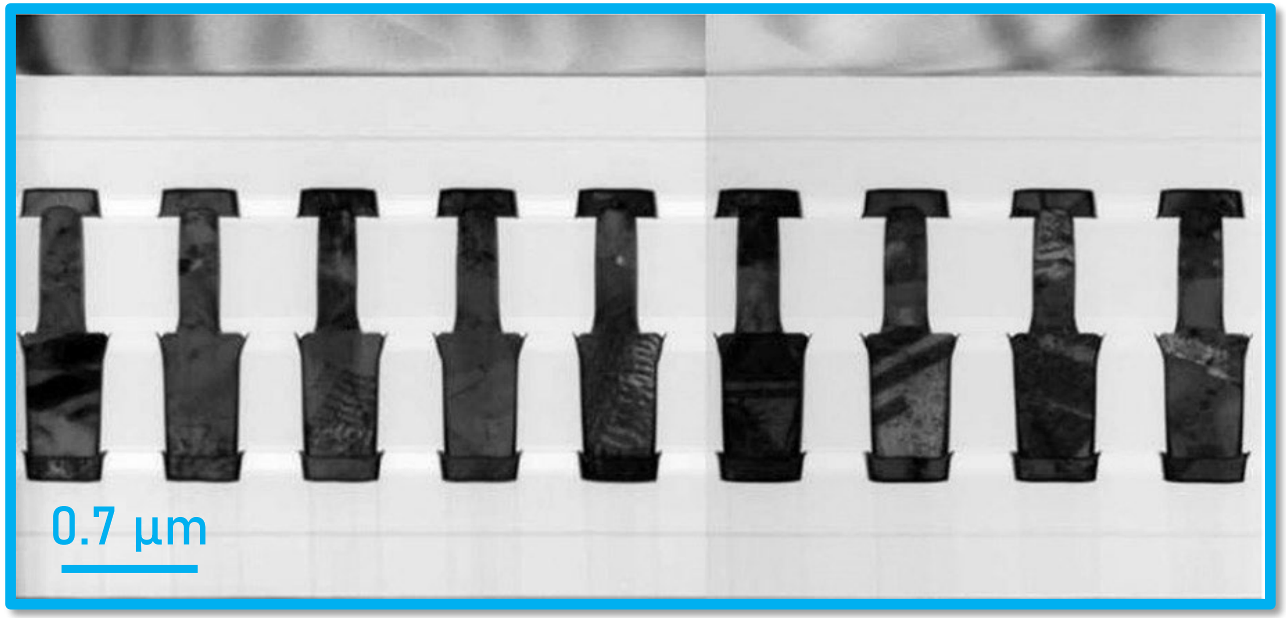
DOI: 10.1109/EDTM.2019.8731186.

Disclaimer



Sony direct bonding (Cu Cu) 1st gen

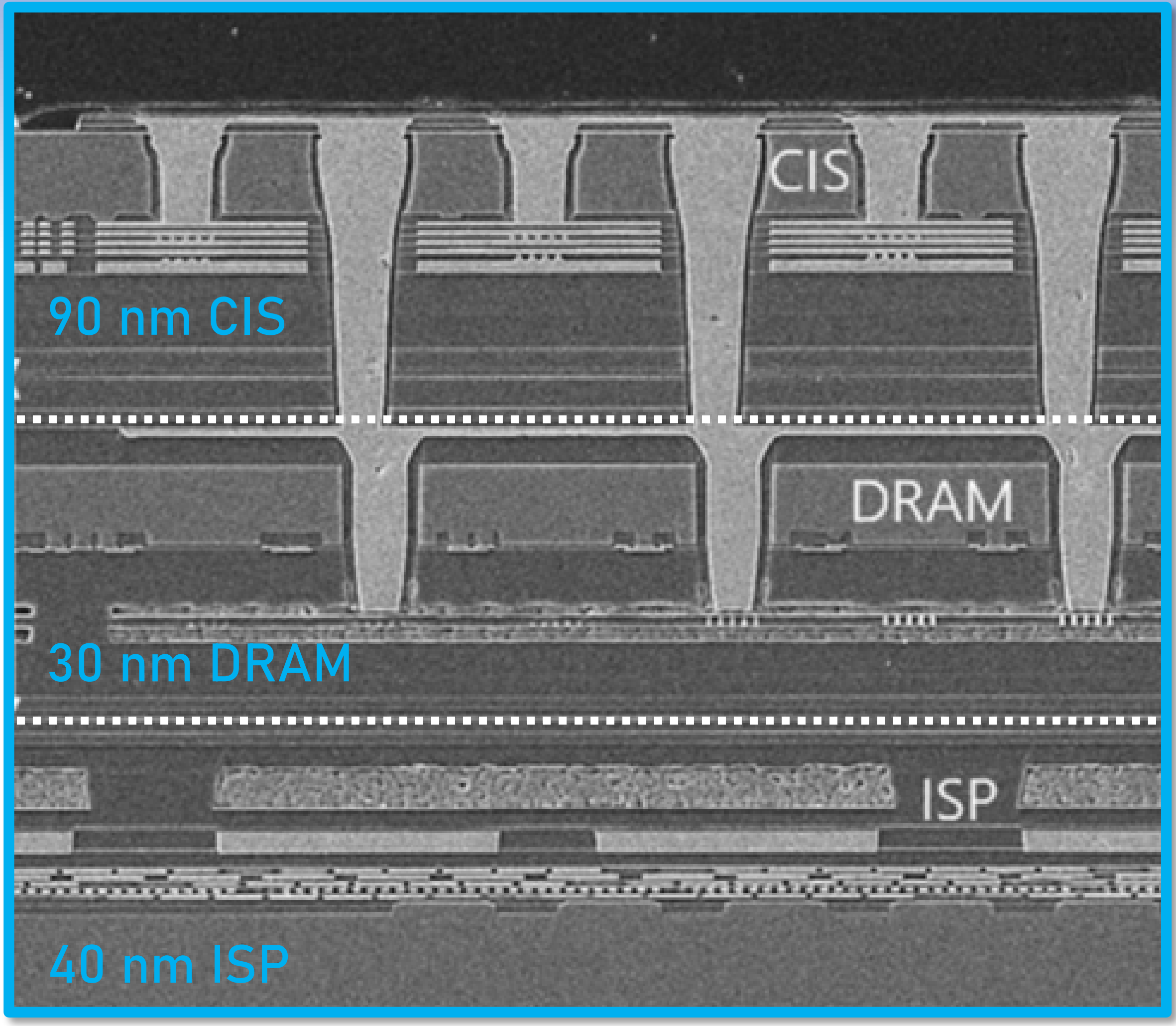




IMEC hybrid bonding

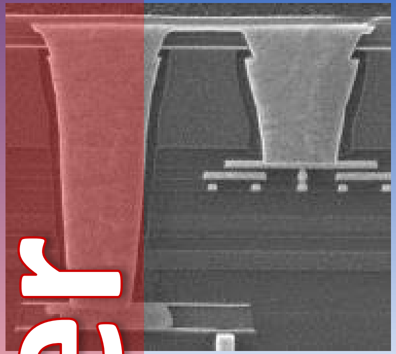
And more can be add…

Disclaimer

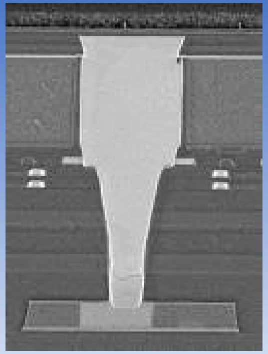


Sony 3-stacked imager (IX400, 2017)

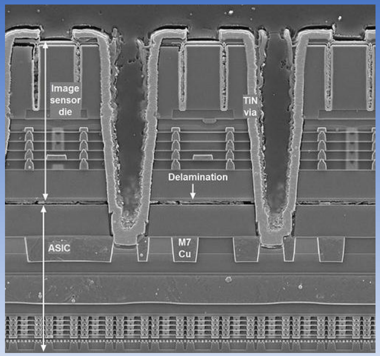
Disclaimer



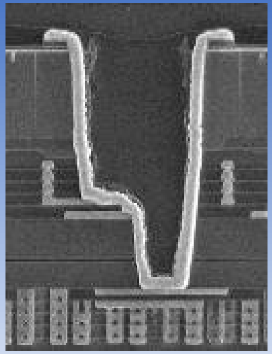
Sony 1st TSV (2013)



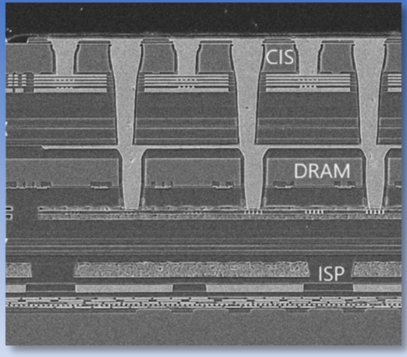
Sony 2nd TSV (2015)



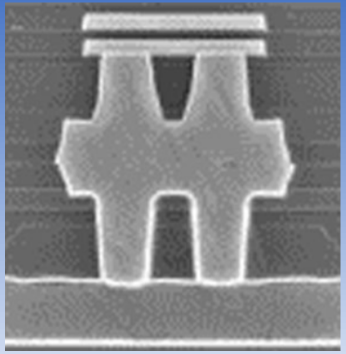
Samsung TSV (2016)



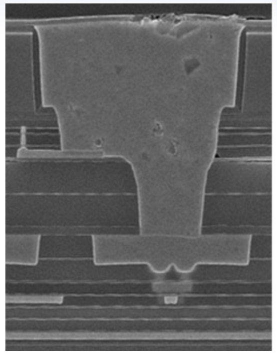
Samsung butted TSV



Sony 3 layer (2017)

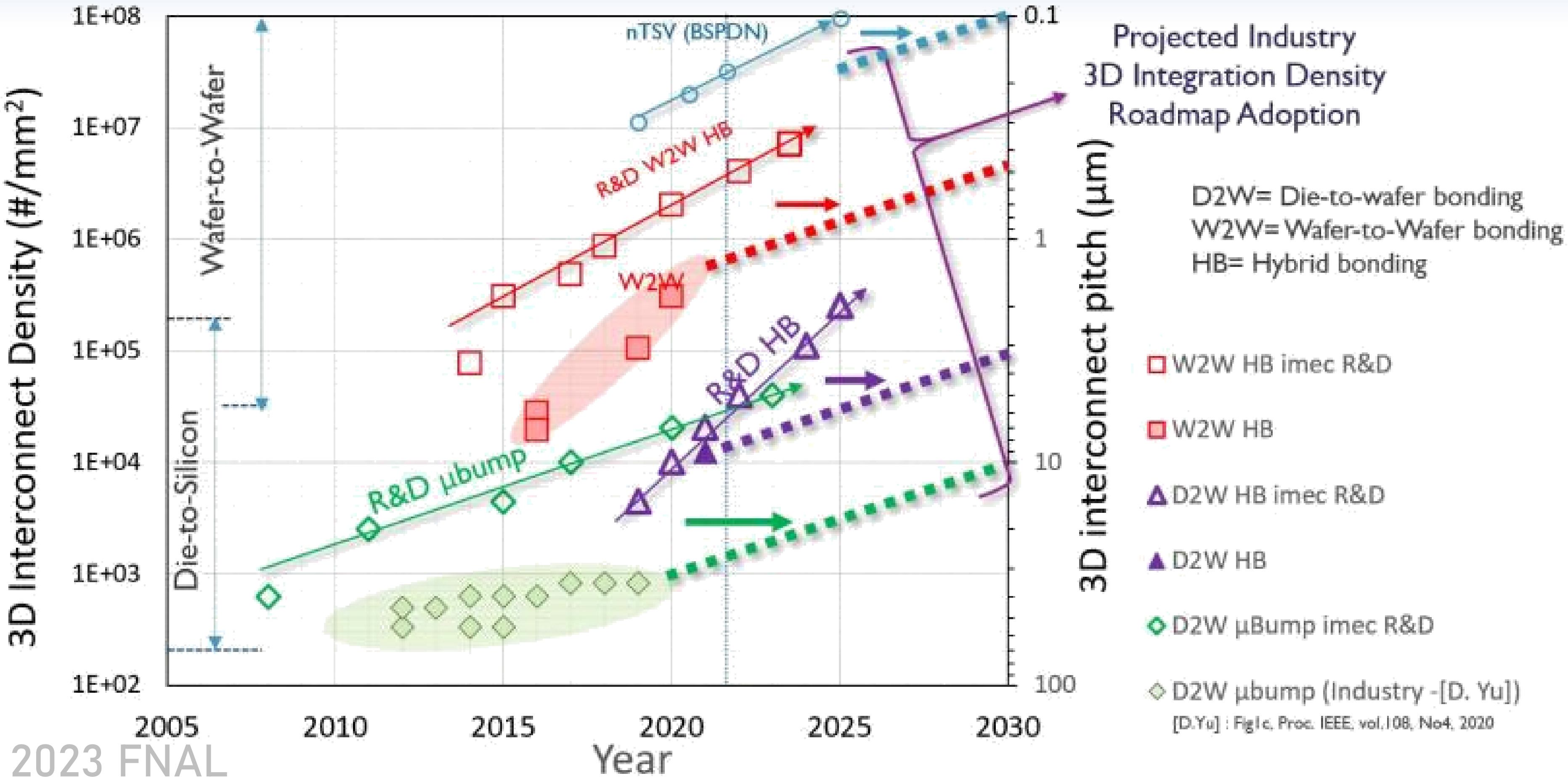


Sony 1st DBI (2018)



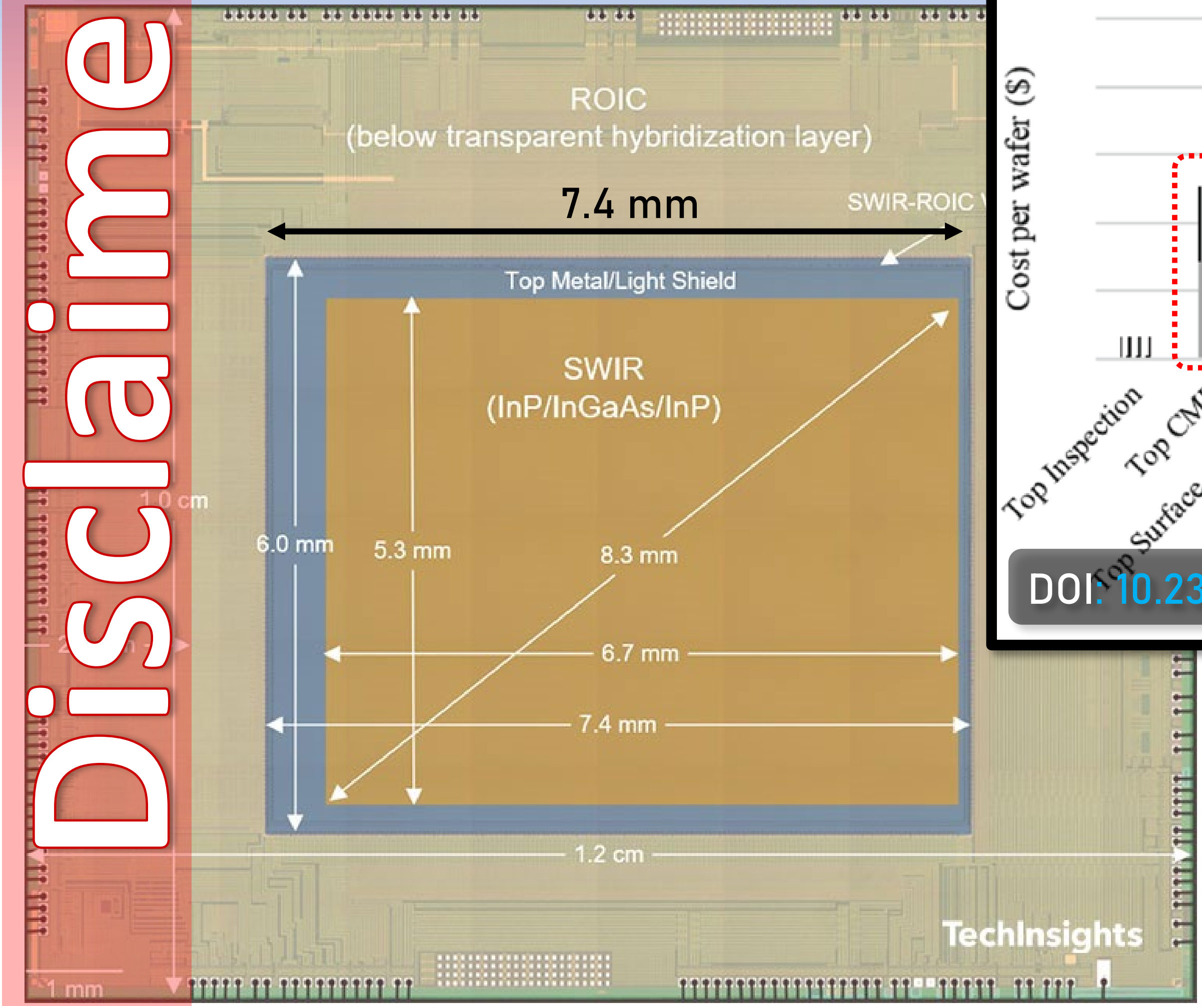
Omnivision 1st TSV (2013)

Omnivision 2nd TSV (2017)

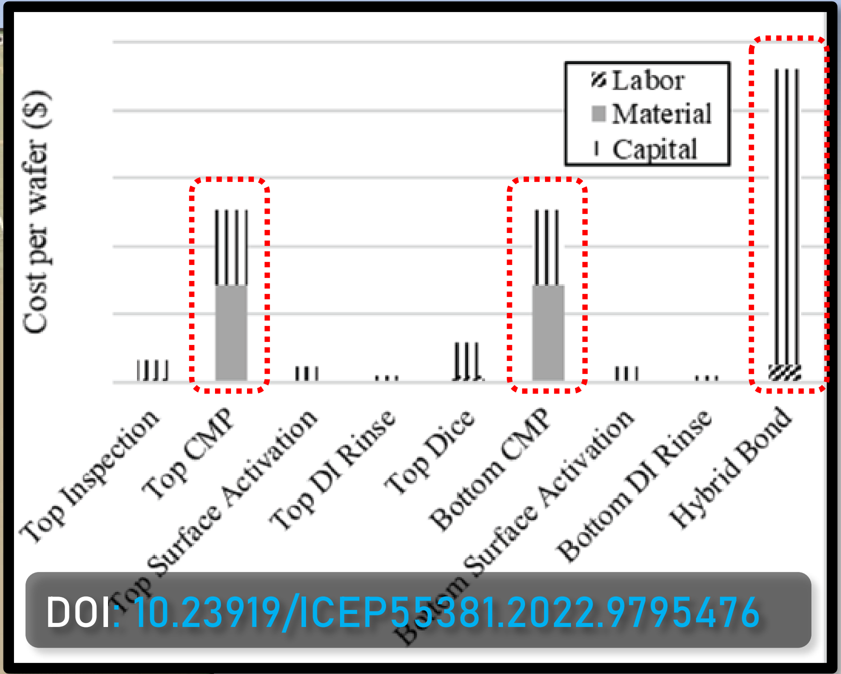


Unfortunately, not yet there for large area sensor

Disclaimer

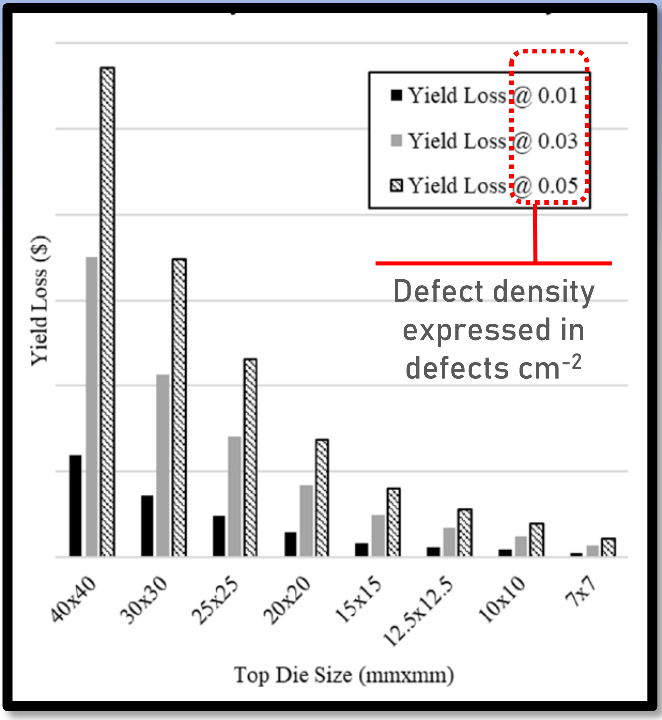


Processing costs breakdown for D2W Hybrid bonding



DOI: 10.23919/ICEP55381.2022.9795476

Yield Loss by Die Size and Defect Density

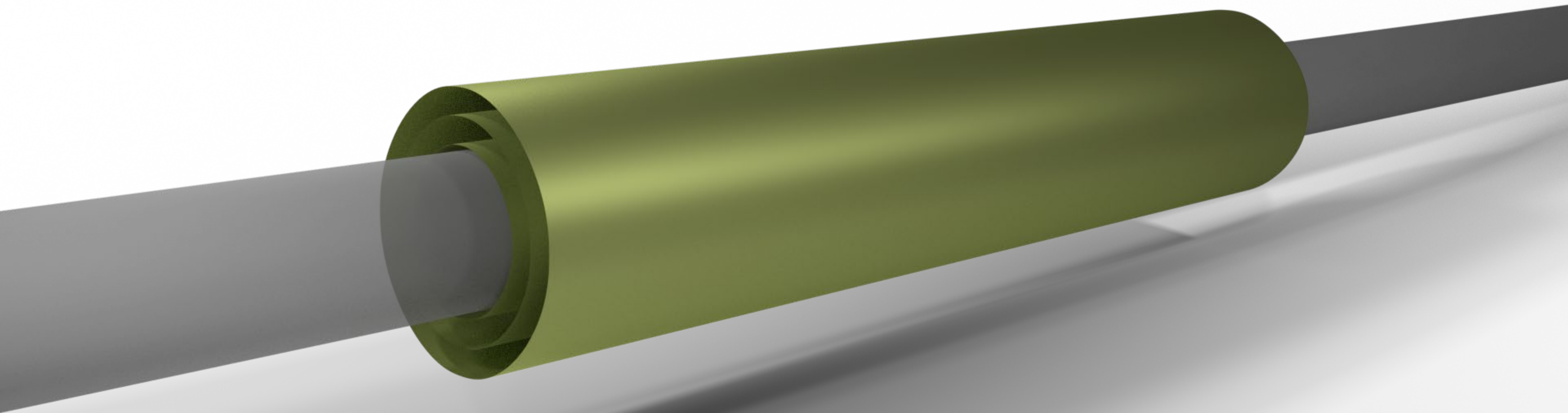


Practical limitation for (our) tracking application are

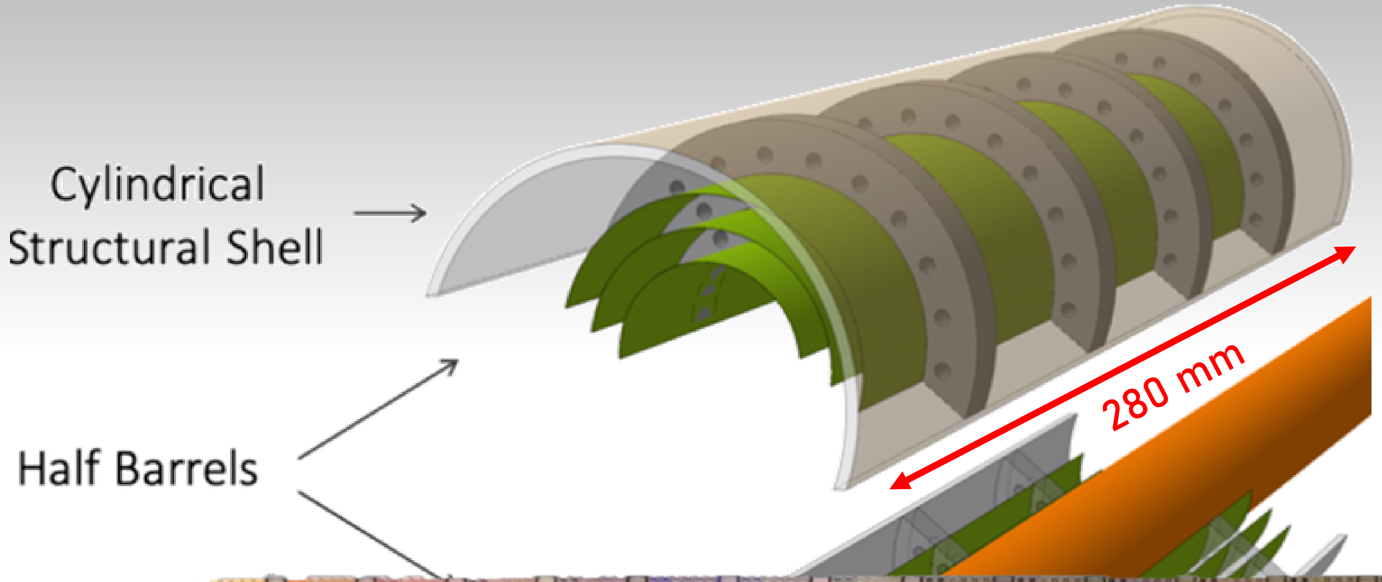
- accessibility: intended for **1000nds chips/hour**
- **yield/cost** (for large area)
- maximum area: **40x40 mm^2** at present
- capacitance to be understood for low power

Ongoing R&D

Mostly ITS3



Vertexing – 280 mm long sensors, self sustaining

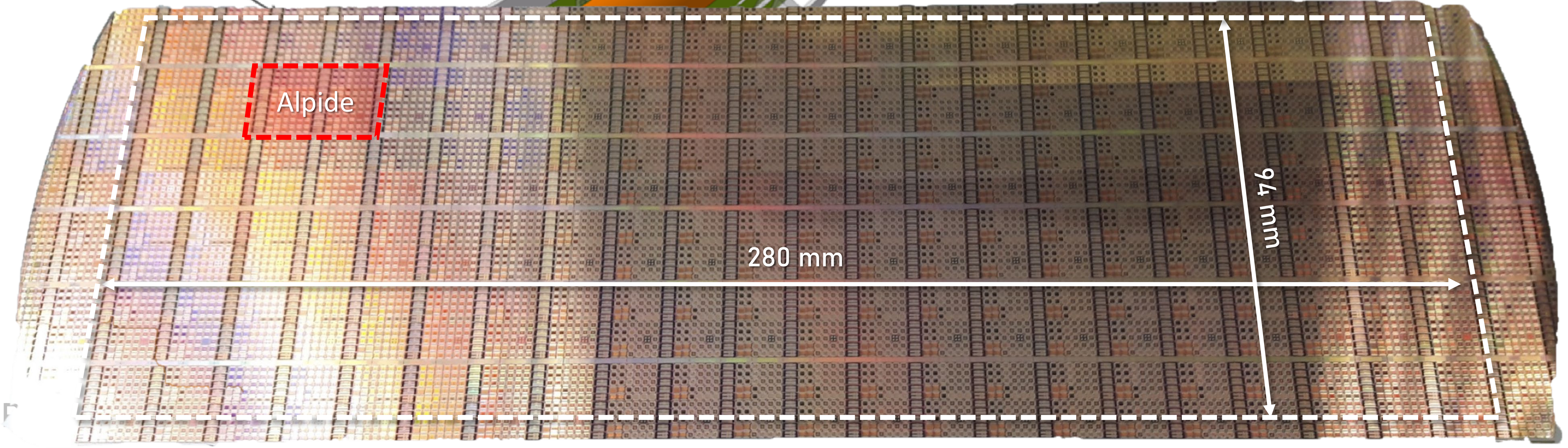


Tower Partner Semiconductor Ltd. Co.

- 65 nm CMOS Imaging Sensor (CIS) process
- 300 mm wafer

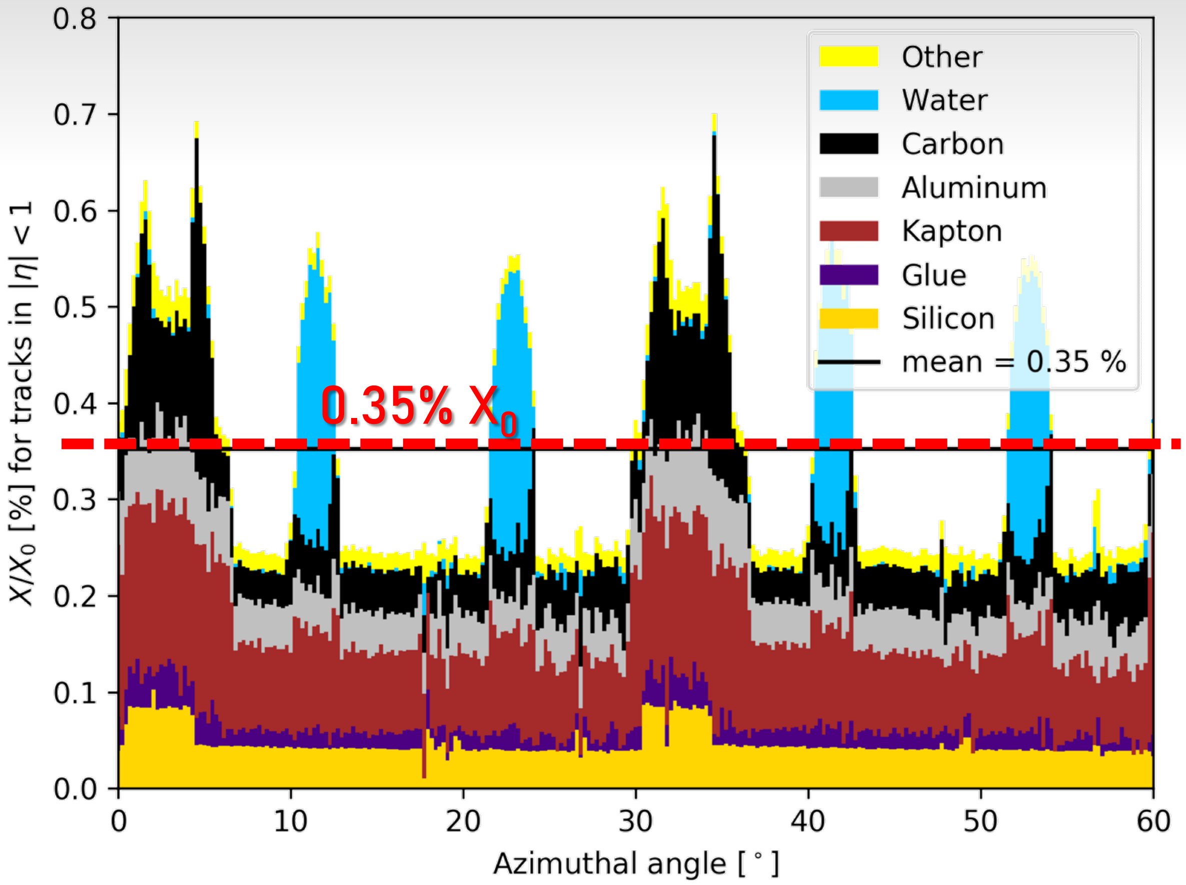
Challenges

- Very large 280×94 mm^2 single silicon piece
- Thinned down to 30-50 µm
- **yield** is crucial: ways of dealing with imperfections need to be built in.

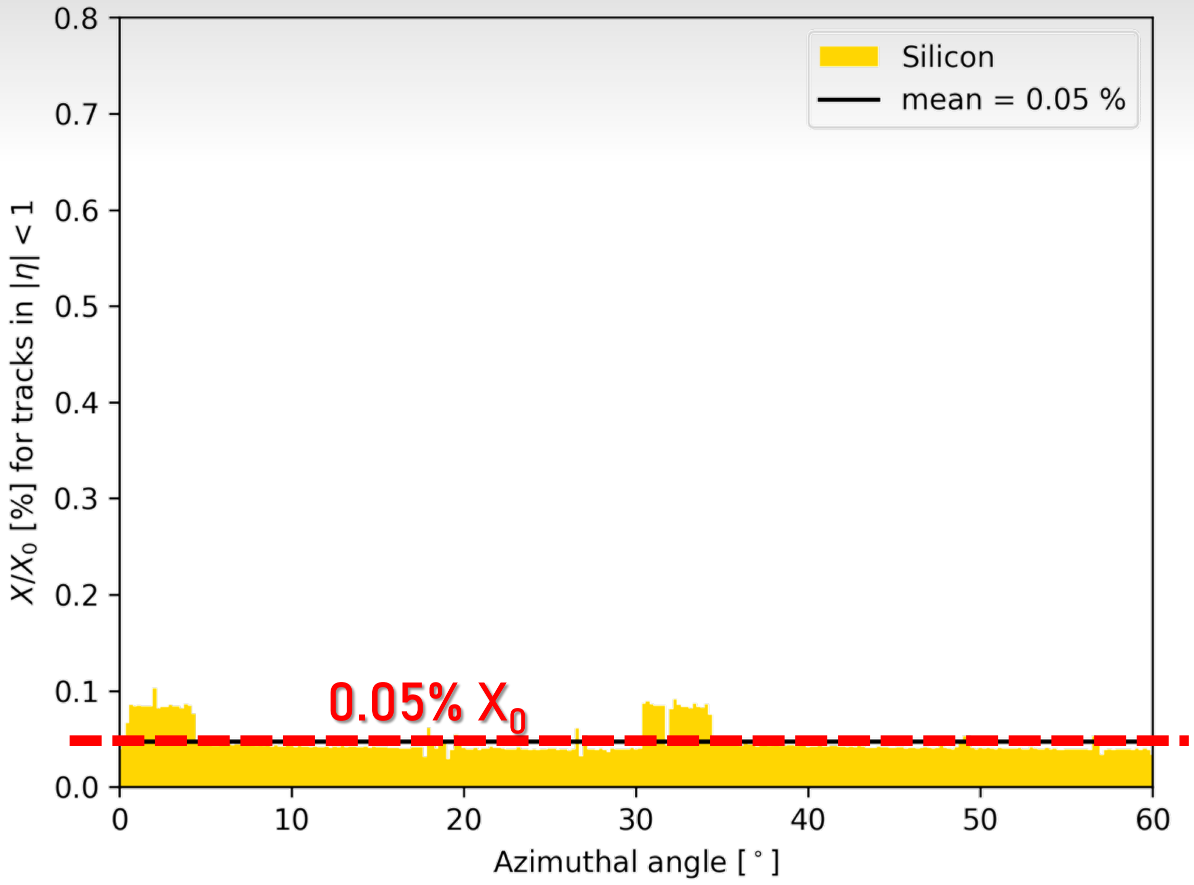


Vertexing – material budget advantage

Material budget – current ALICE ITS2



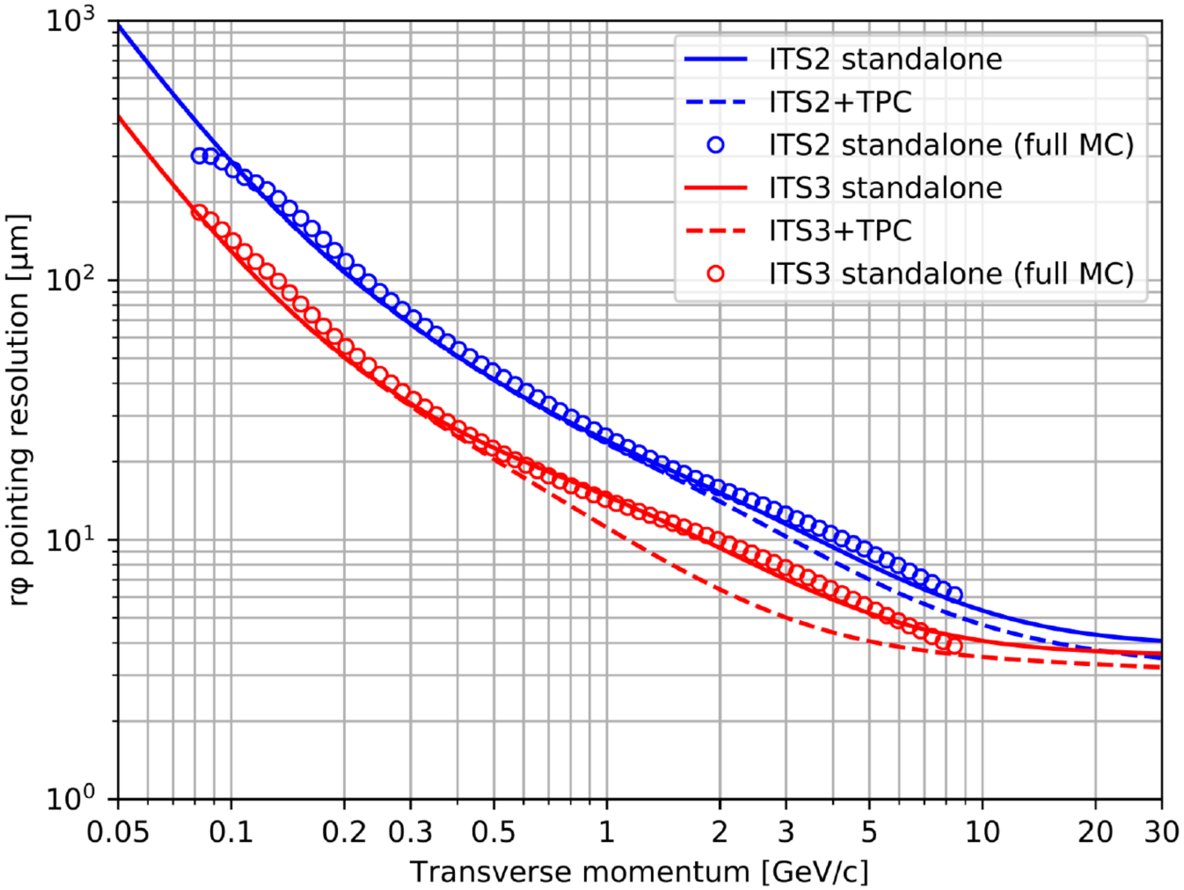
Material budget – foreseen ALICE ITS3

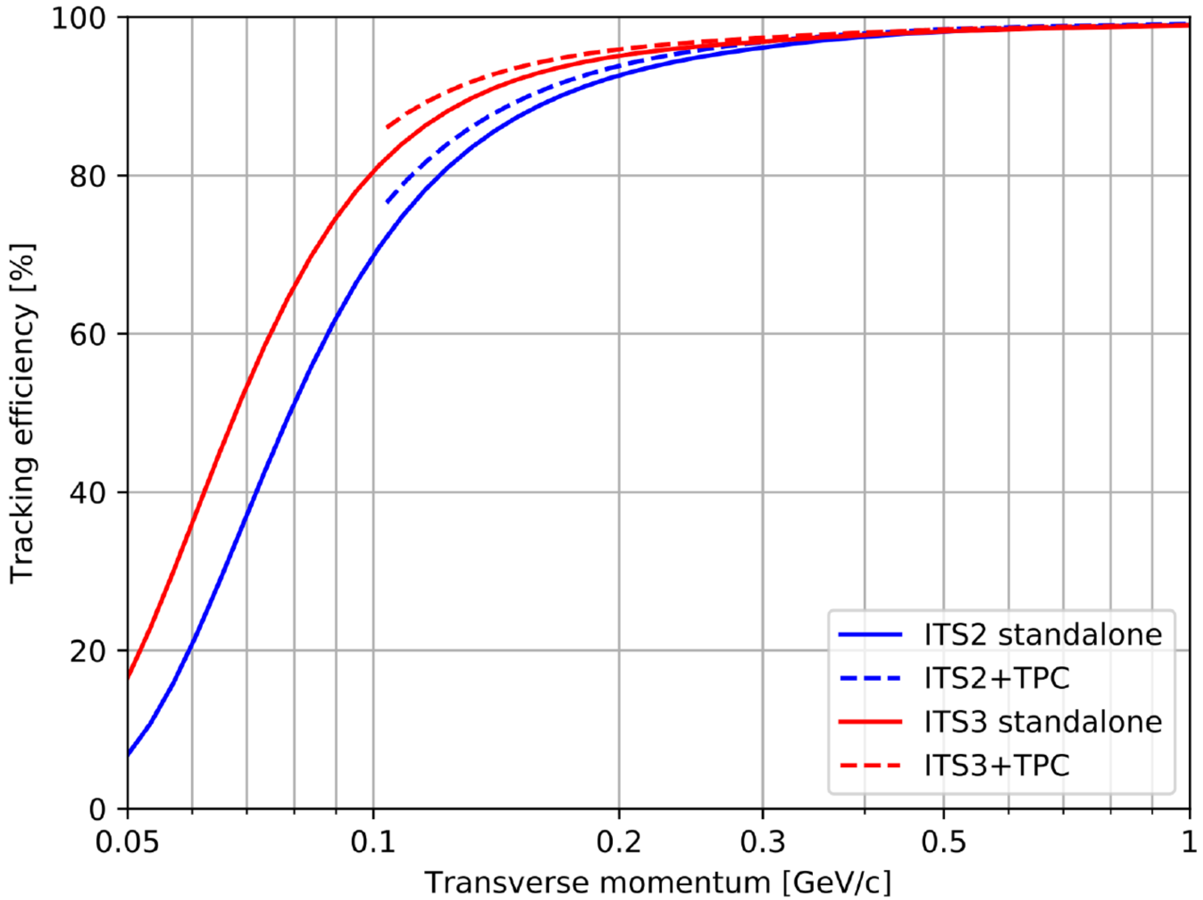


Vertexing – improved performance by material reduction

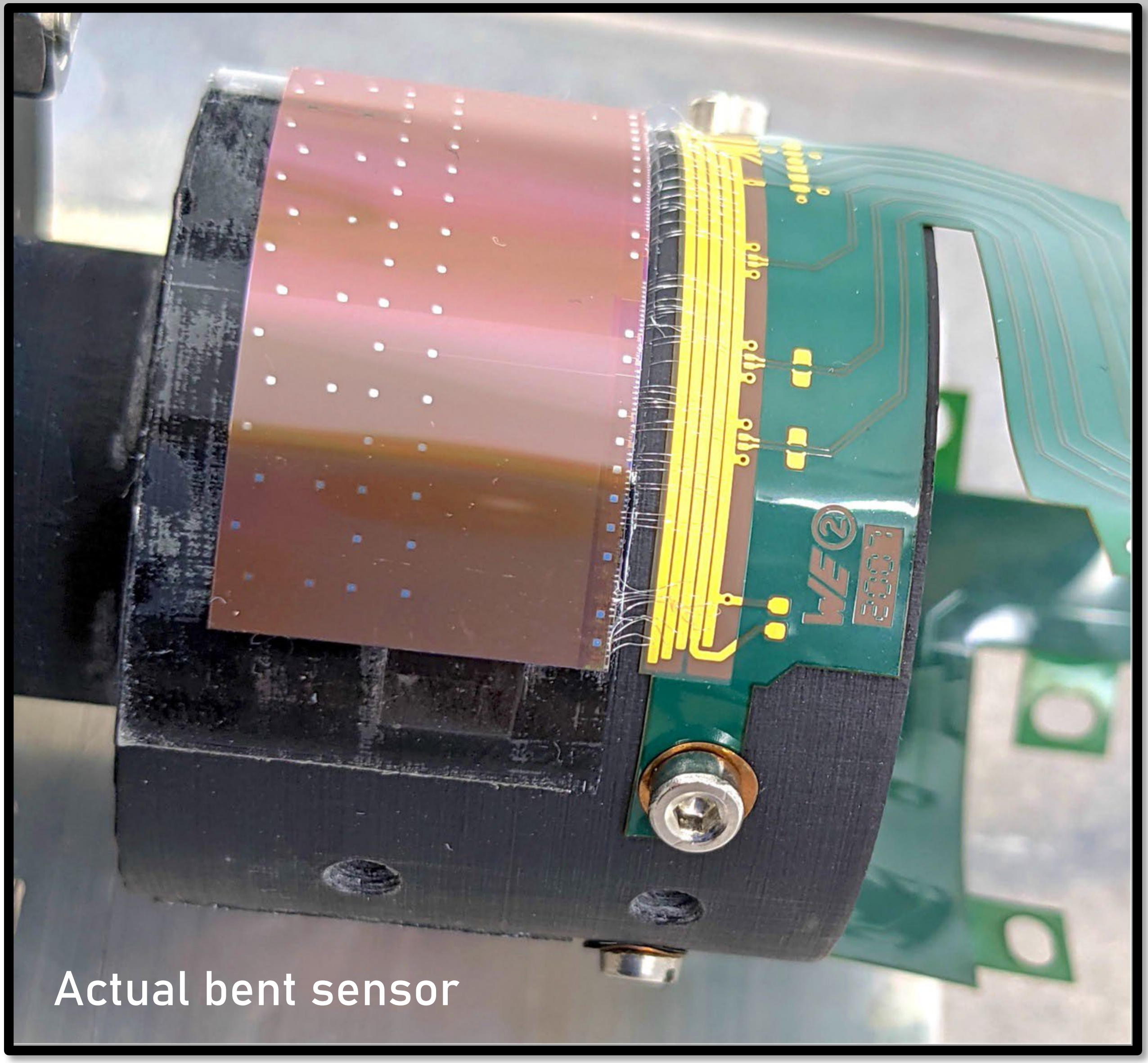
3 Cylindrical layers
- Made with 6 curved wafer-scale single-die
- Monolithic Active Pixel Sensors
- Radii 18/24/30 mm, length 27 cm
- Thinned down to <50 µm

Position resolution ~5 µm
- Pixels O(20 µm)
- No flexible circuits in the active area
- Distribute supply and transfer data on chip to the short edge

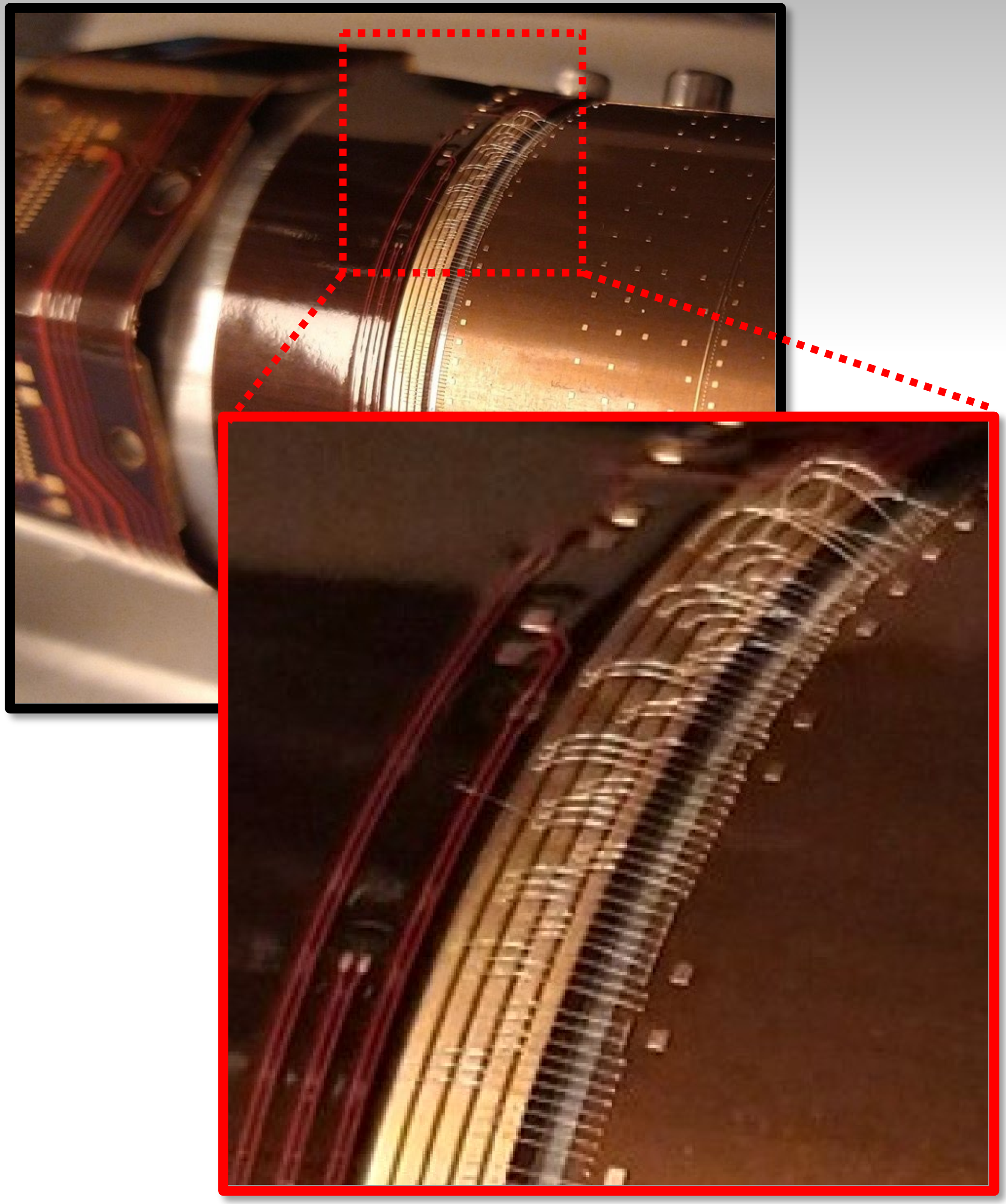




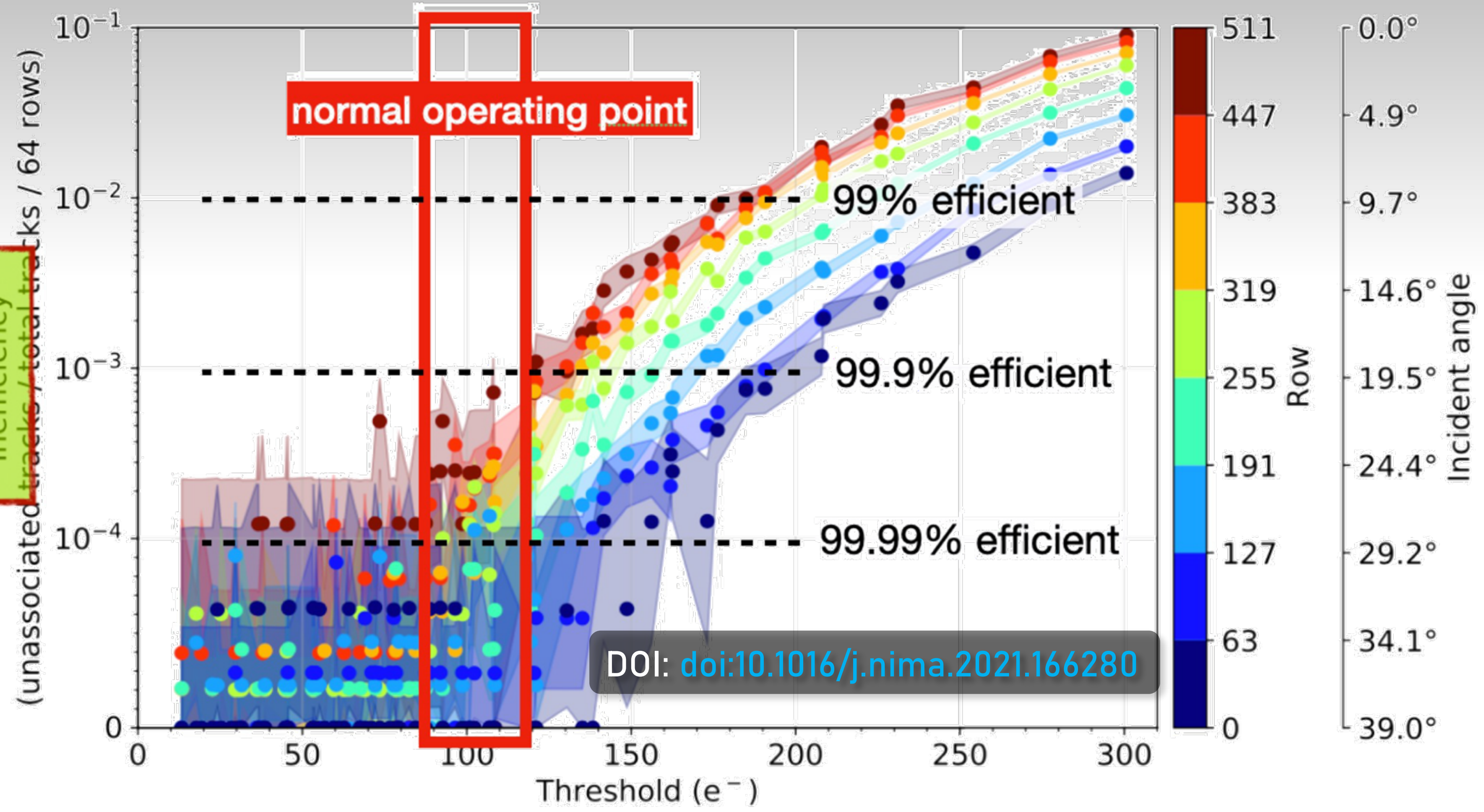
Bending – improving jigs and connections

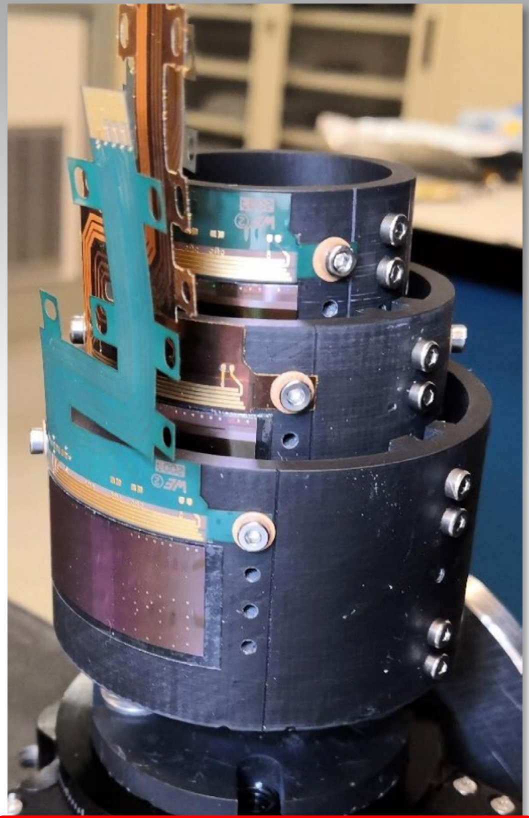


Actual bent sensor



Bending – sensors work (ONGOING R&D)





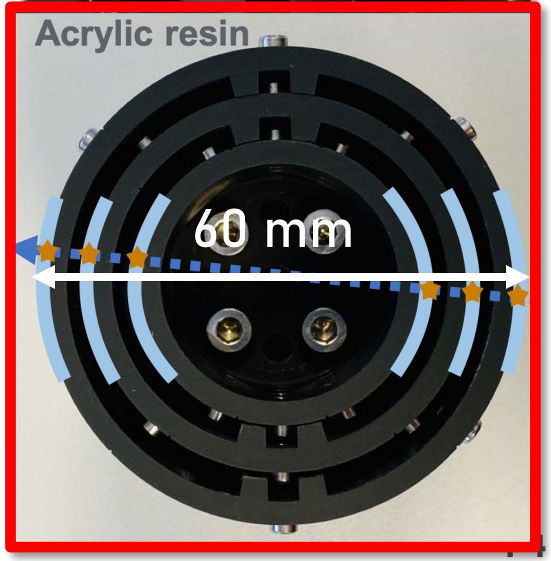
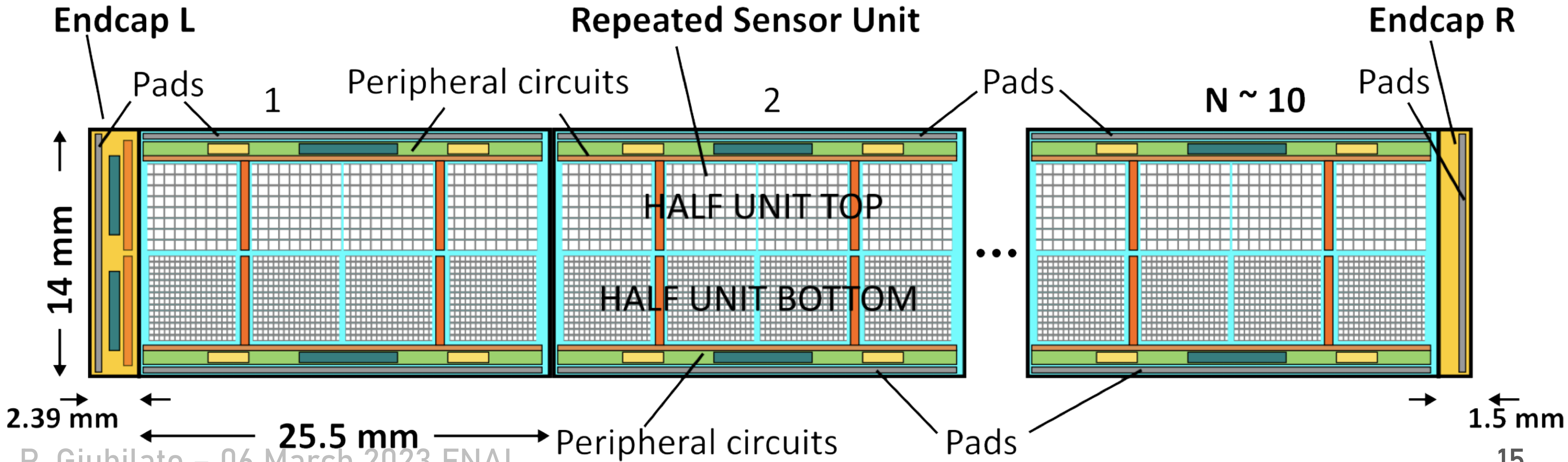


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

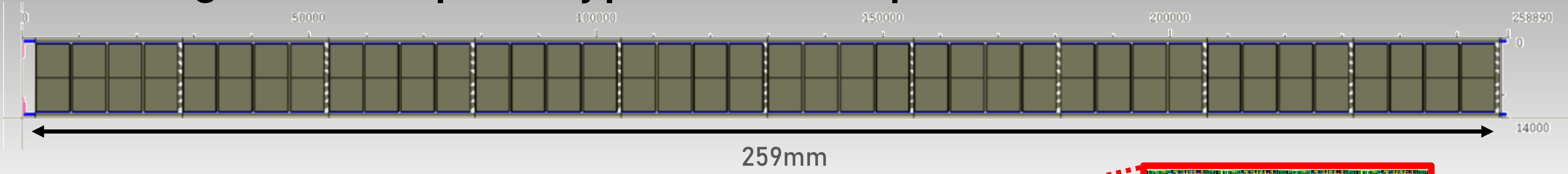
Stitching – single piece, 280 mm long sensor

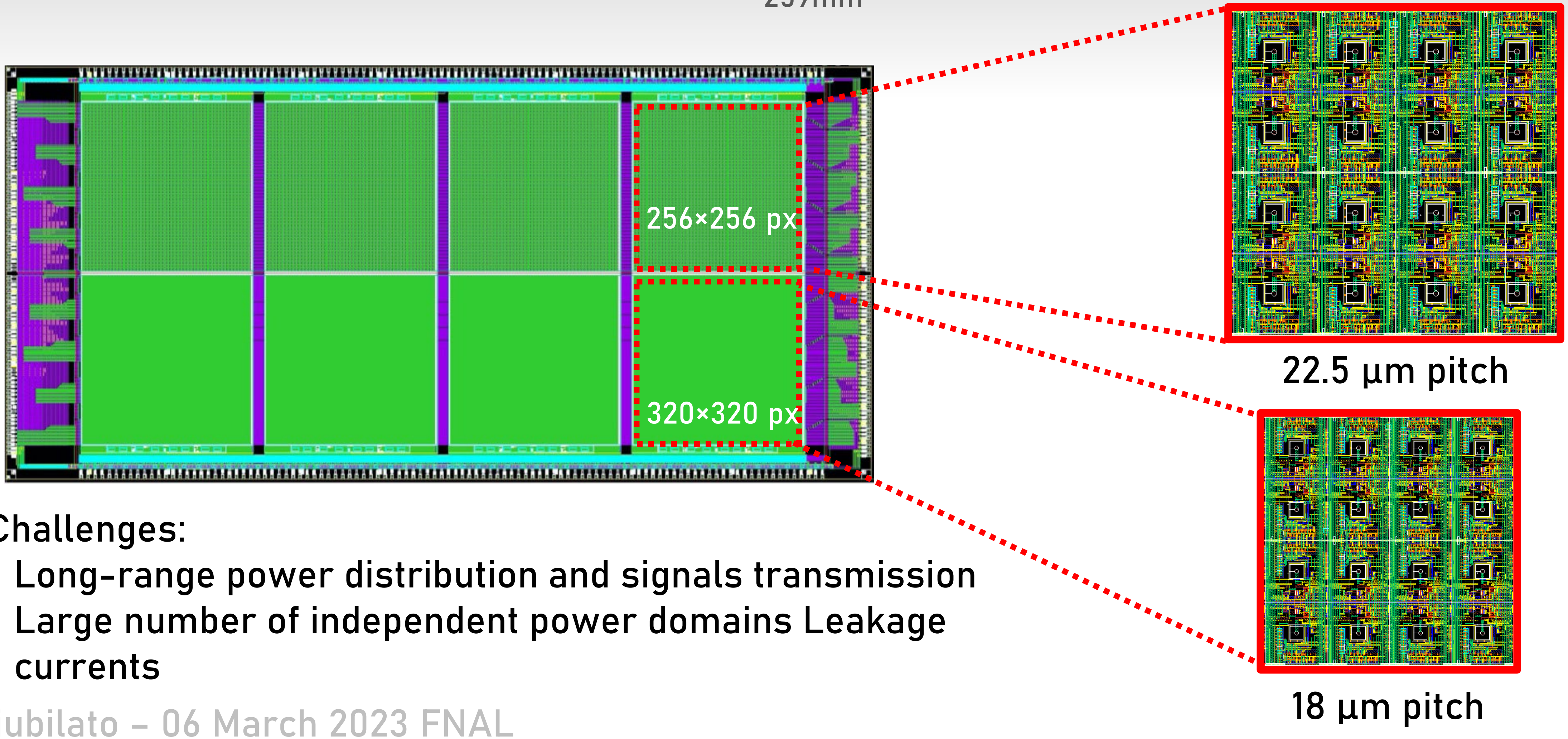
Stitching: "easy on paper" but requires substantial R&D:
- design methodology is new: needs to be learned and exercised
- **yield** is crucial: ways of dealing with imperfections need to be built in
- power consumption/voltage **drops become significant** (scales quadratically with chip size)

MOSS and **MOST** address the stitching in two complementary ways
- **MOSS** is a more conservative repetition of sensor blocks, being generous in the line spacing and circuit density to avoid shorts
- **MOST** relies on a very fine-grained way of turning off malfunctioning parts instead



Stitching – MOSS prototype (due 2nd quarter 2023)



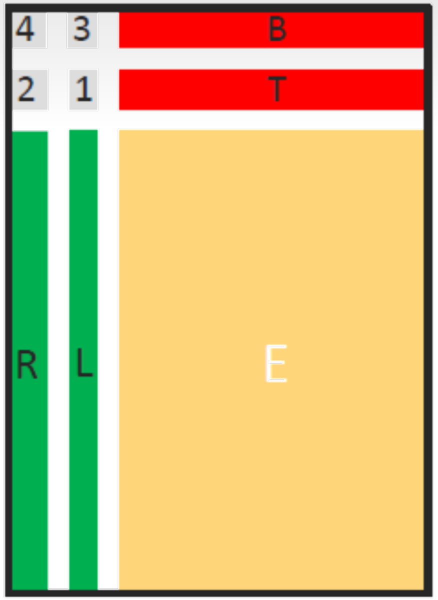


Challenges:

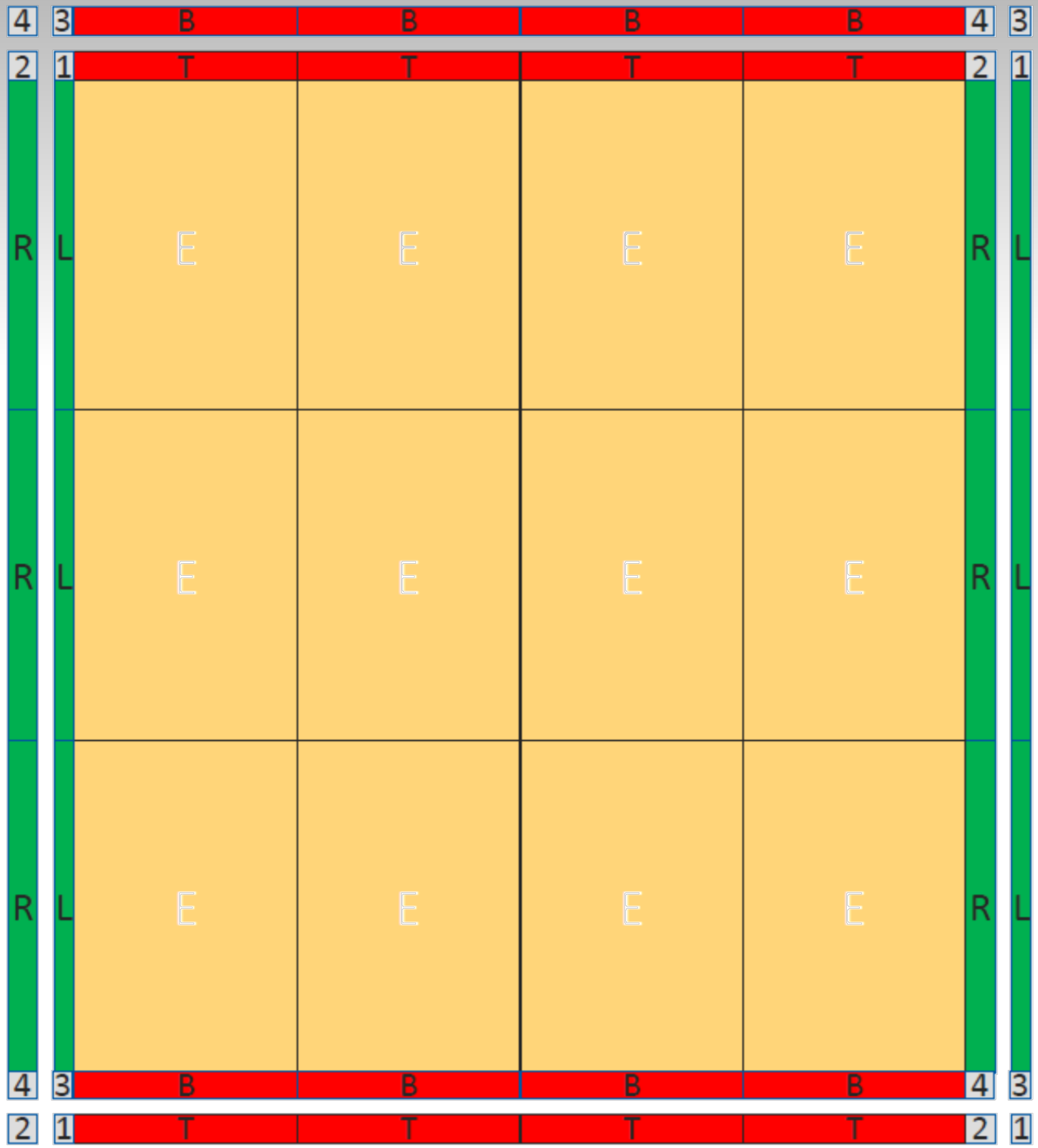
- Long-range power distribution and signals transmission
- Large number of independent power domains Leakage currents

Stitching – design strategy

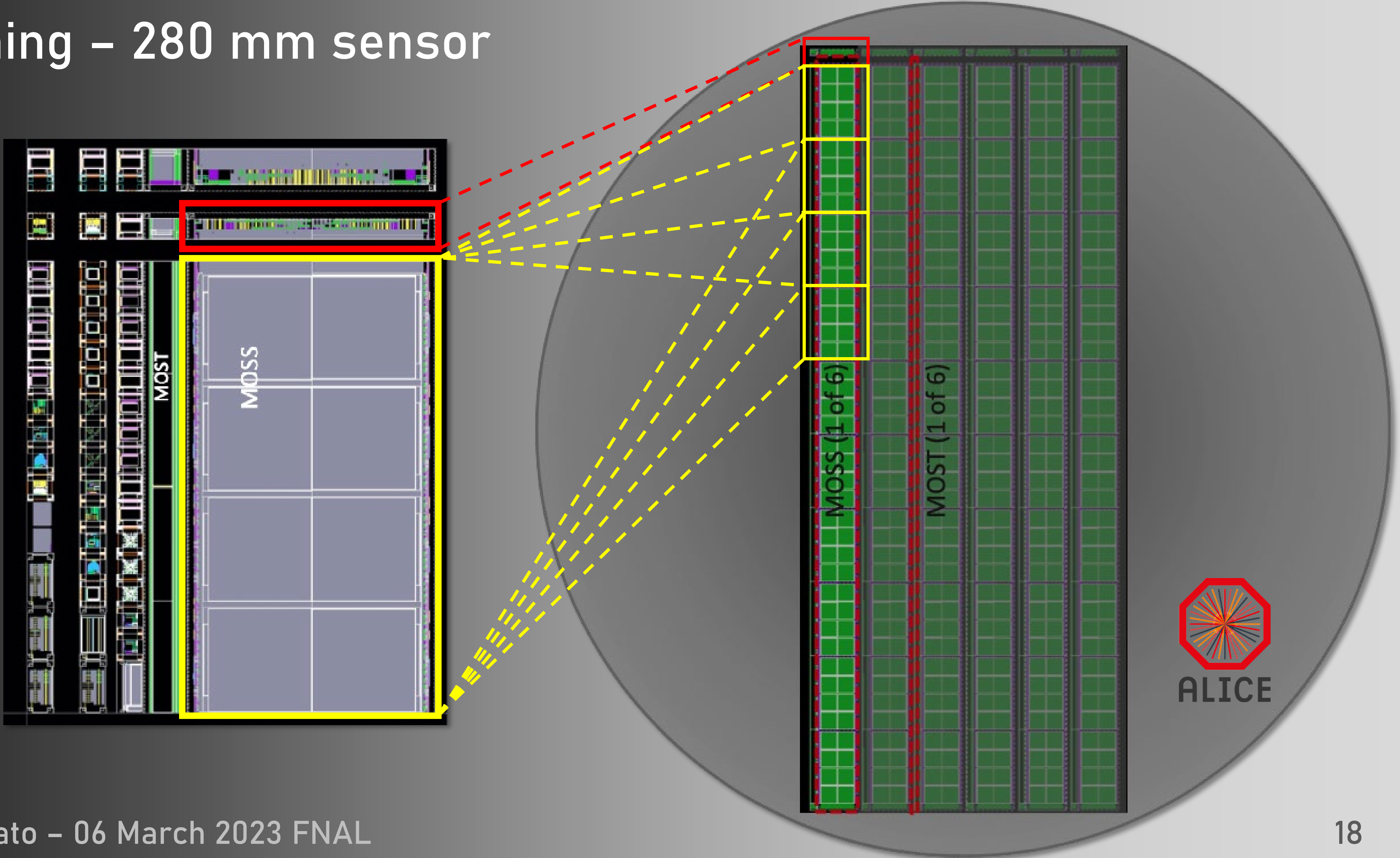
Design reticle



Stitched design



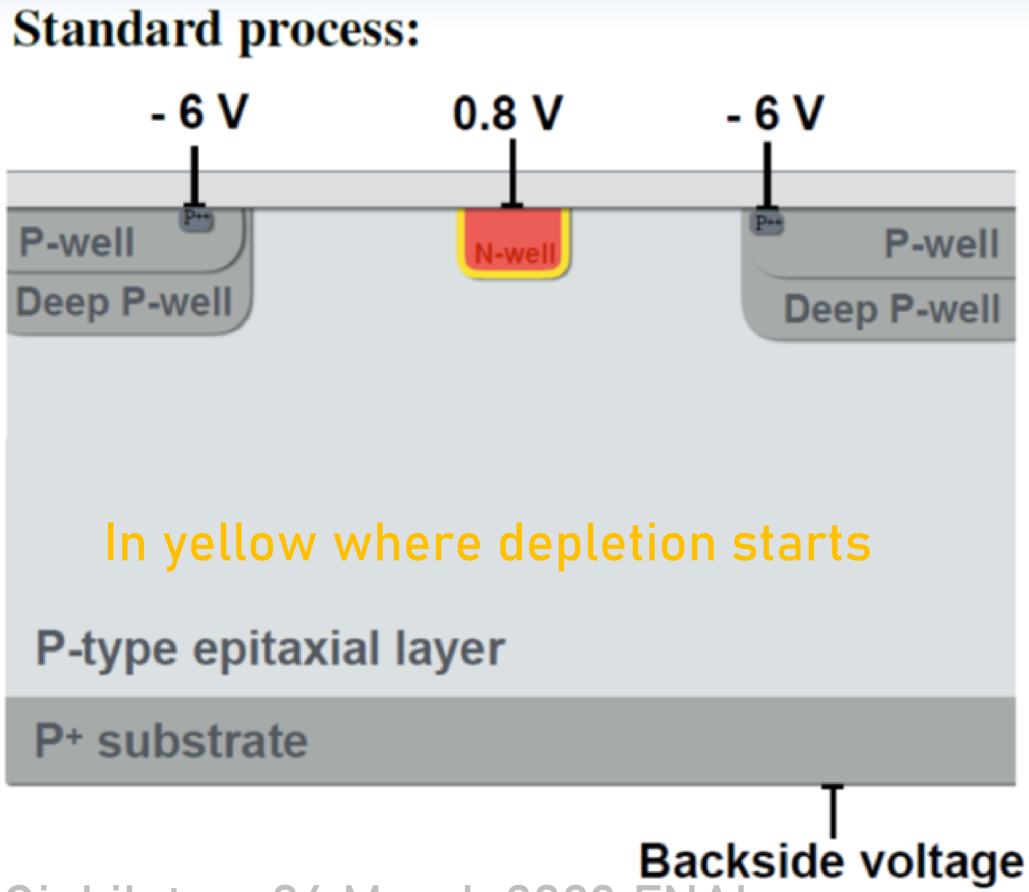
Stitching – 280 mm sensor

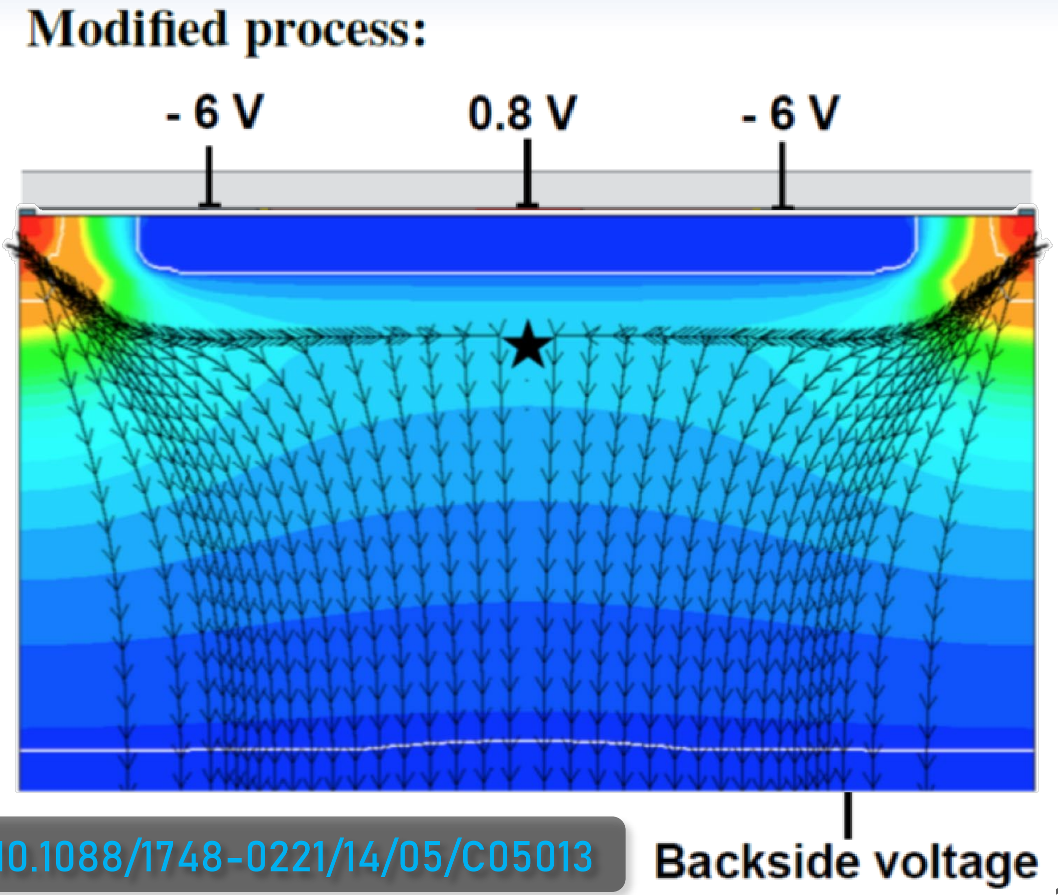


Monolithic requires some tweaking

Standard process (left): difficult to make the depletion layer extend from the junction around the small collection electrode laterally

Modified process: the deep low-dose n-type implant creates a planar junction under the existing implants, so that the depletion starts at the junction, making full depletion easier



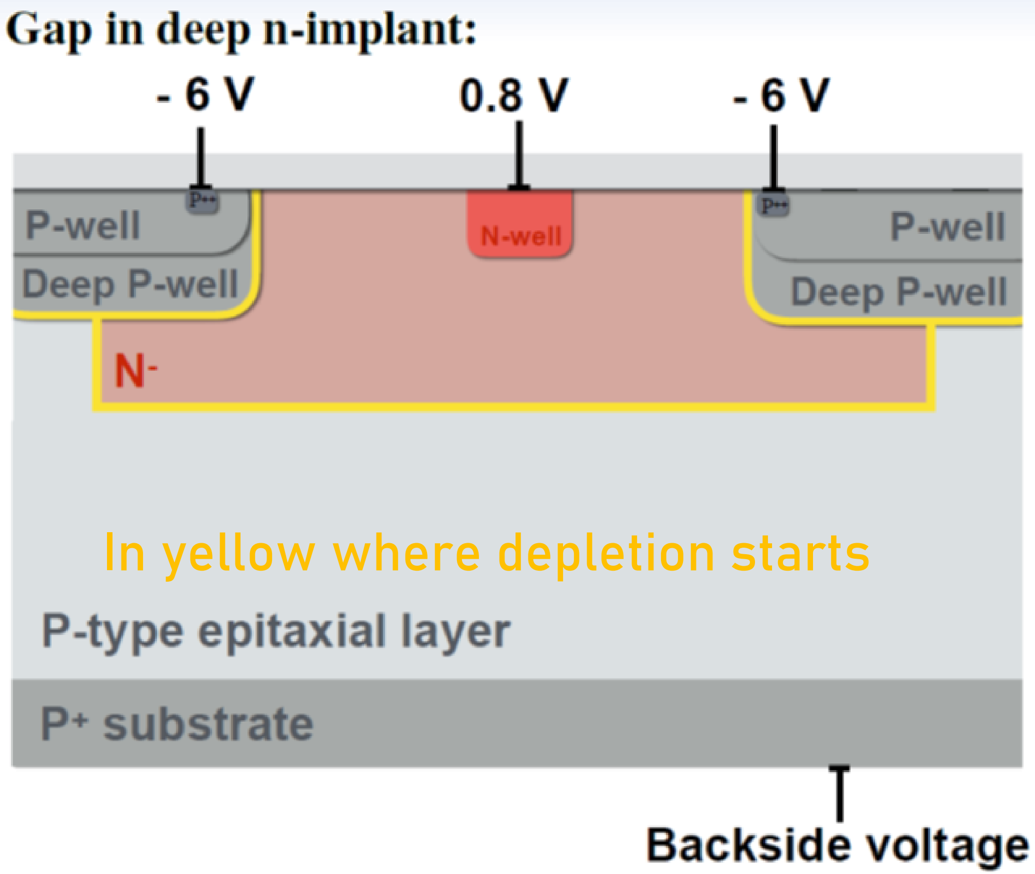


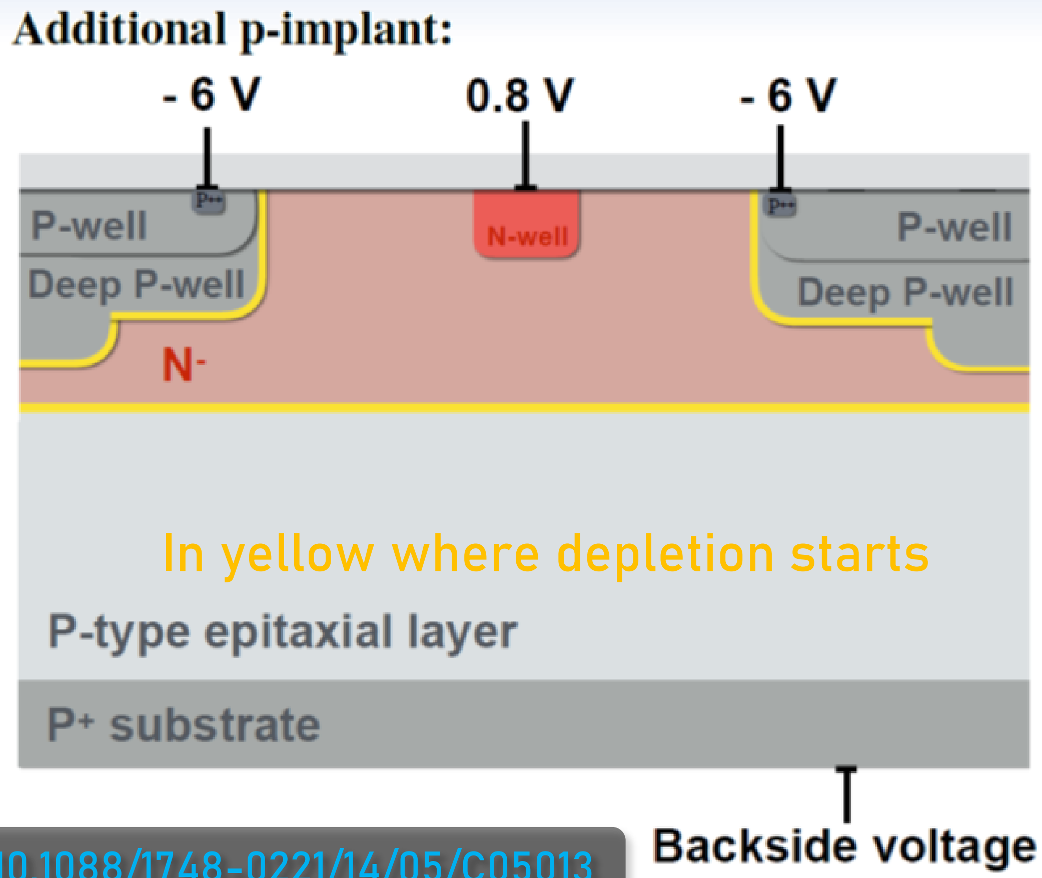
DOI: 10.1088/1748-0221/14/05/C05013

Further modifications to increase charge collection speed

Additional gap in the deep n-implant helps making the E-field stronger at the sides

Extra p-implant improves field strength at sides as well





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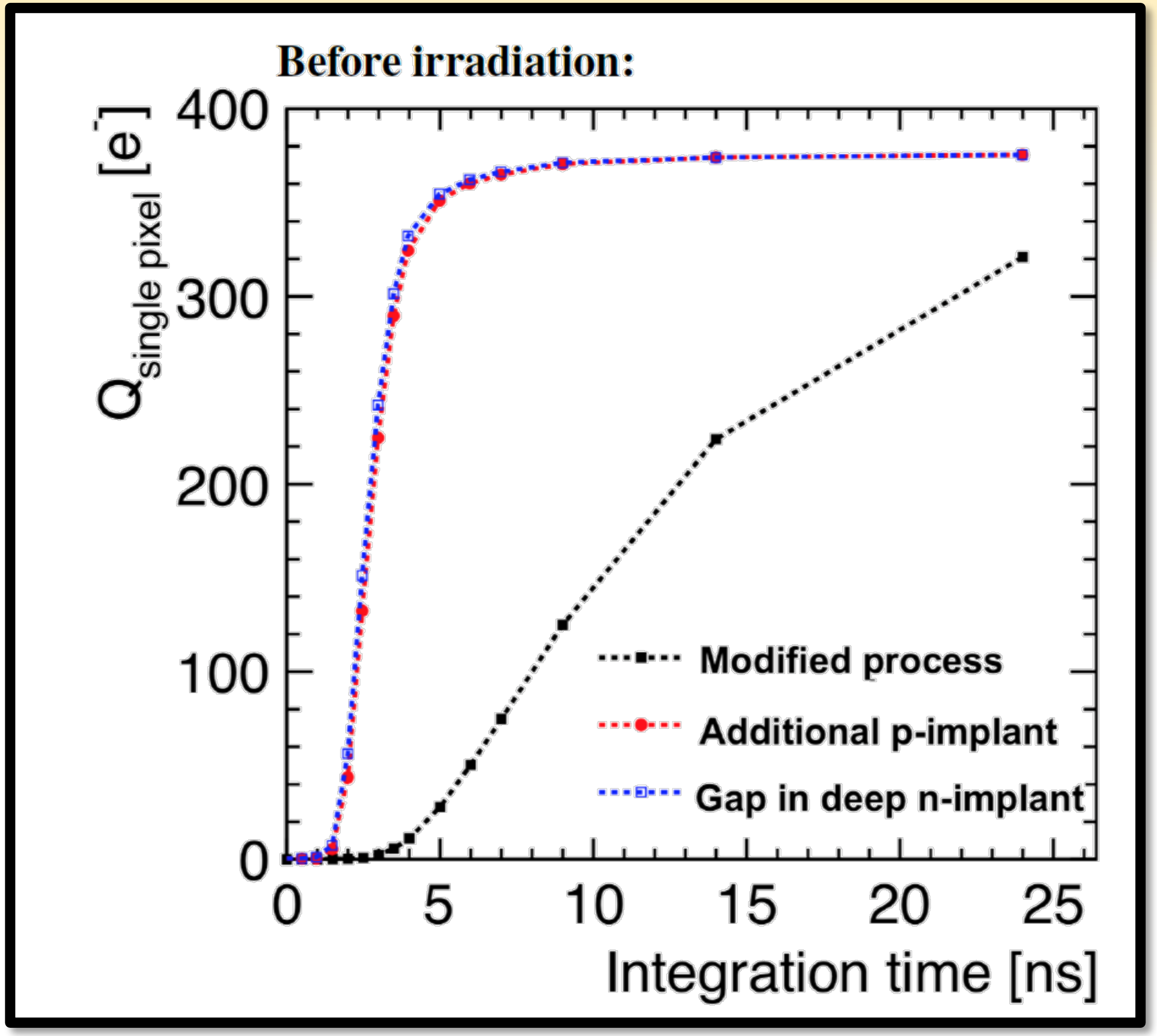
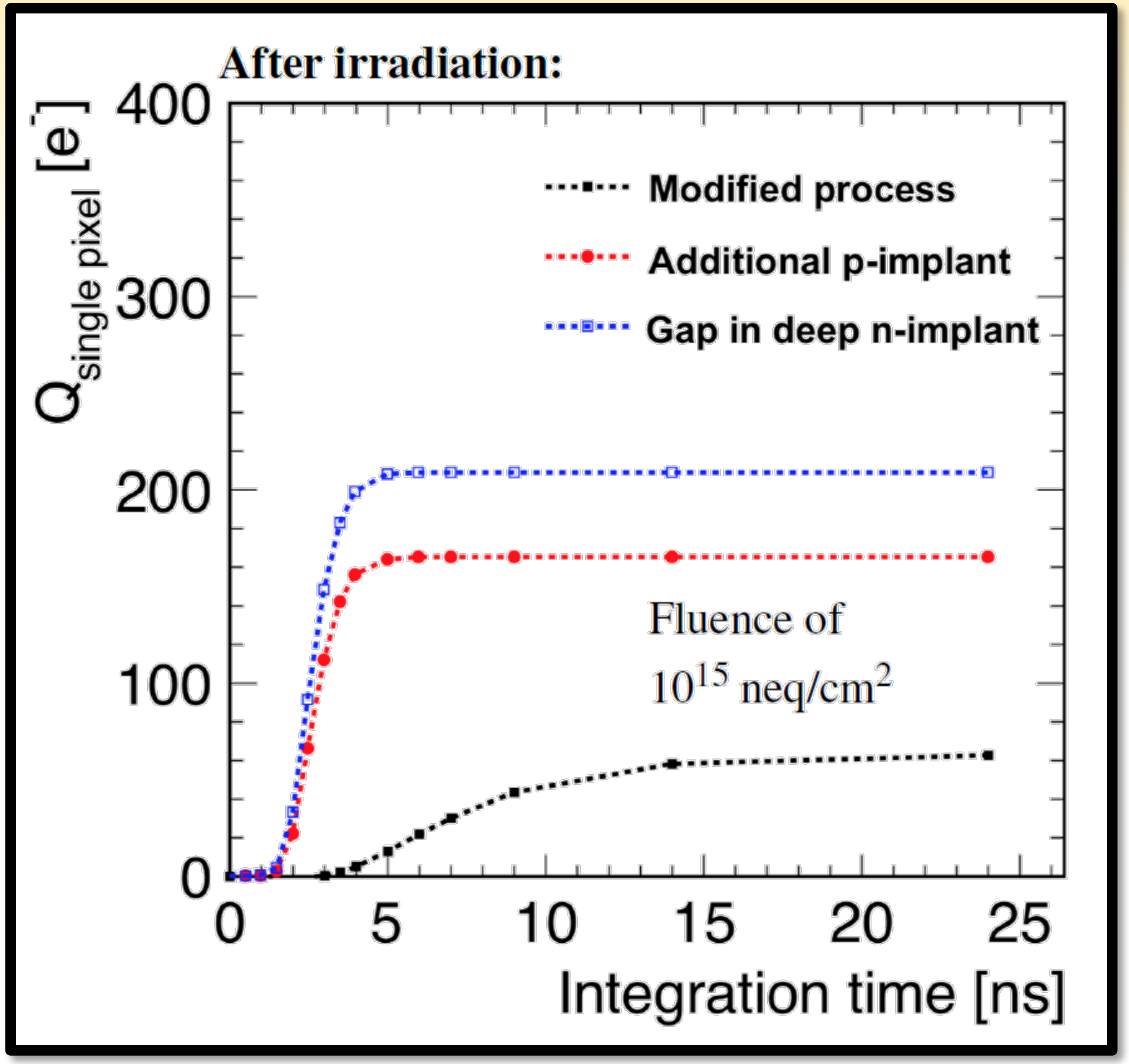
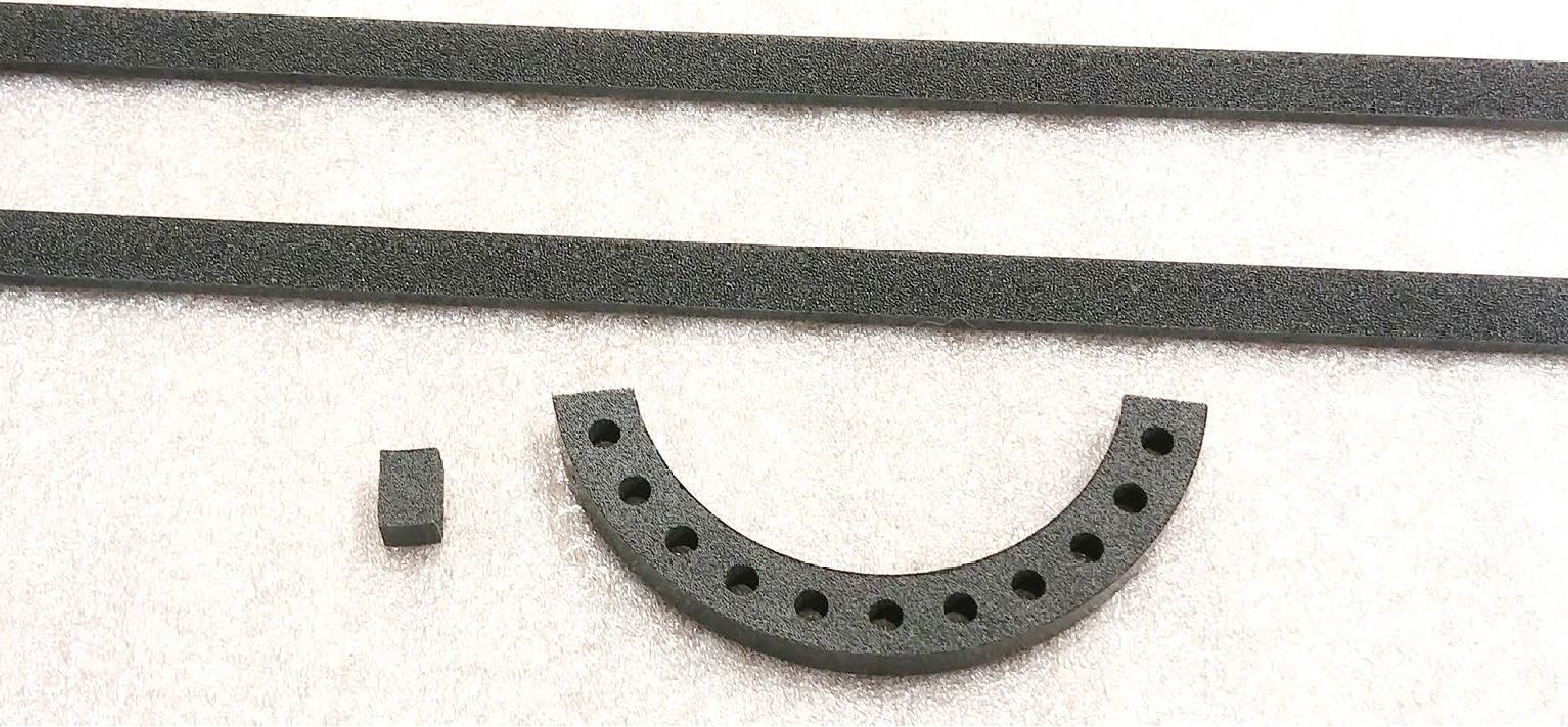
Speed and radiation tolerance are both improved





Integration



Wafer scale sensor and minimal support structure

ALICE

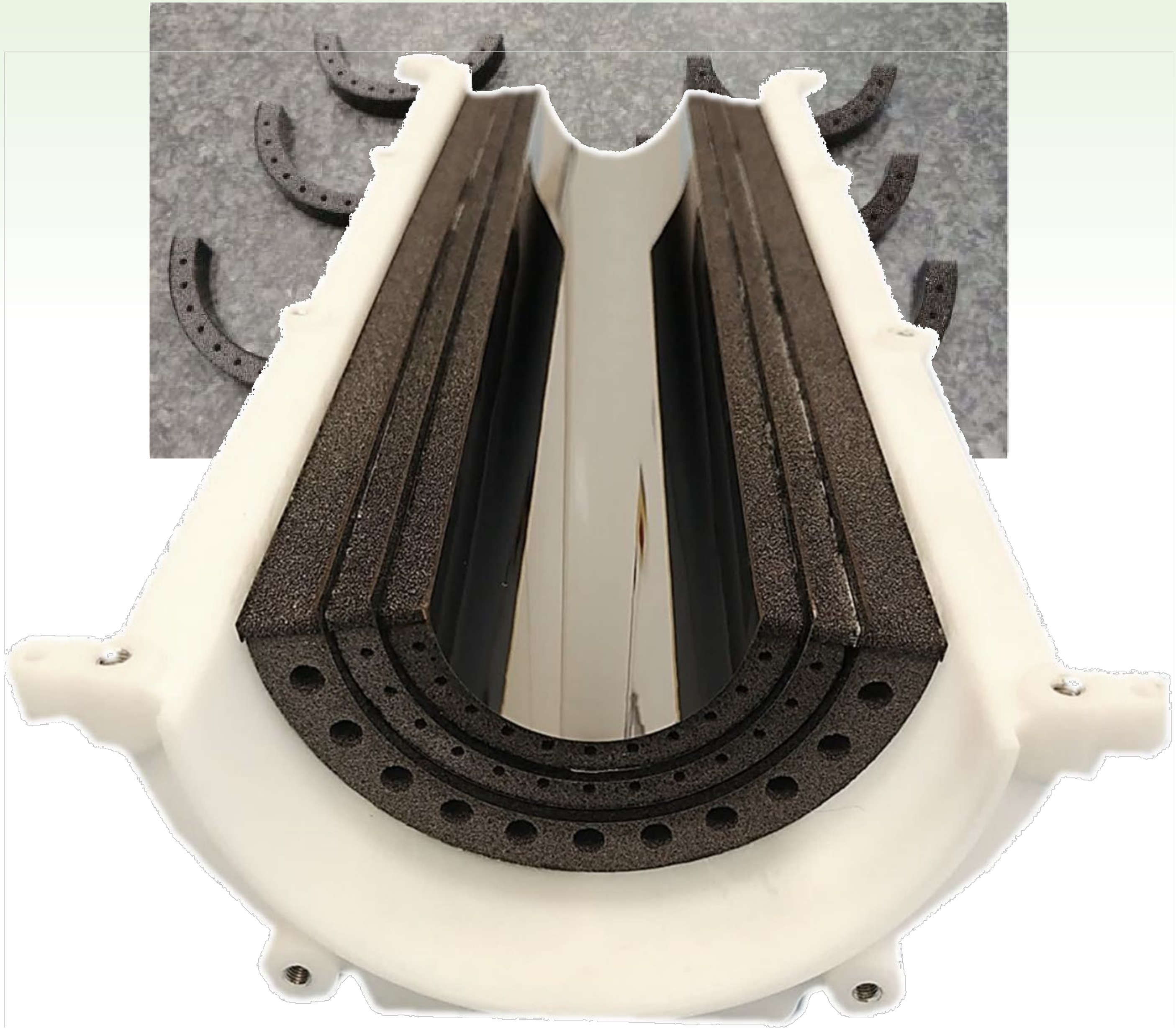
12 inches blank silicon wafer
40-50 micron thick

Carbon foam

- Duocel Foam ERG (longerons)
  - ρ = 70 kg/m^3
  - K = 0.05 W/(m*K)
- ALLCOMP LD Foam (rings)
  - ρ = 200 kg/m^3
  - K = 20 W/(m*K)

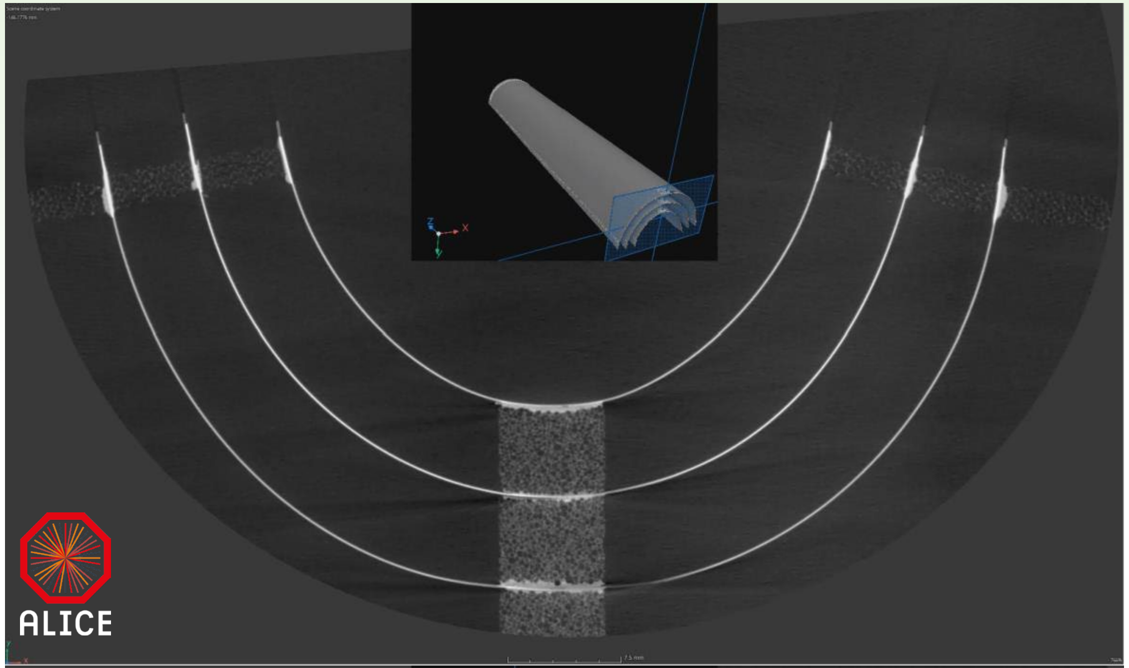
3-layer vertex prototype

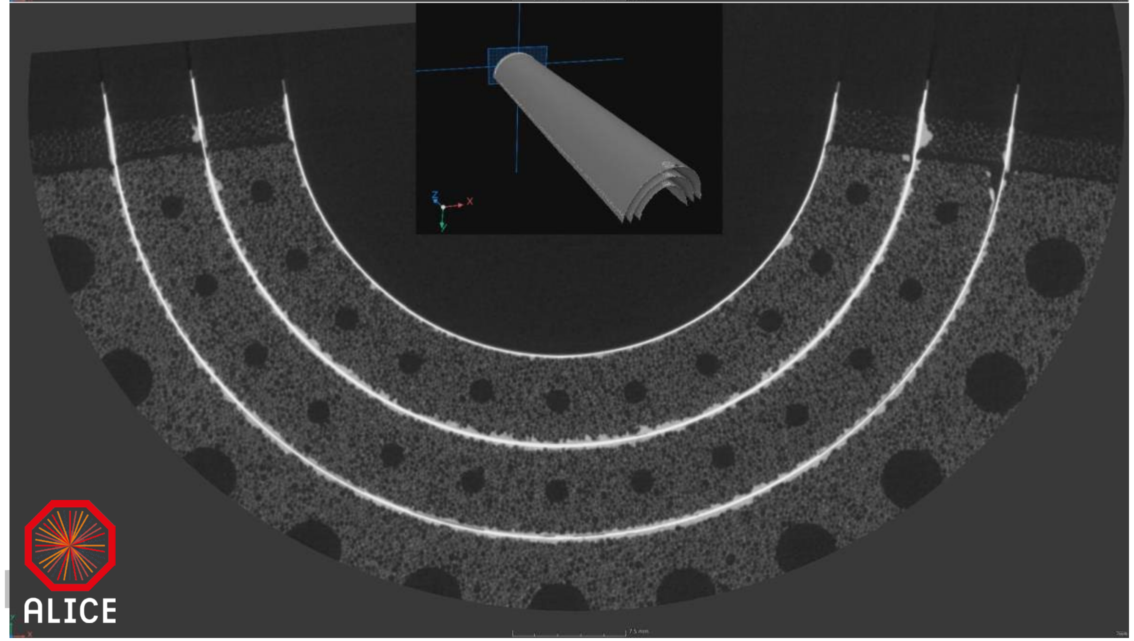
Old prototype

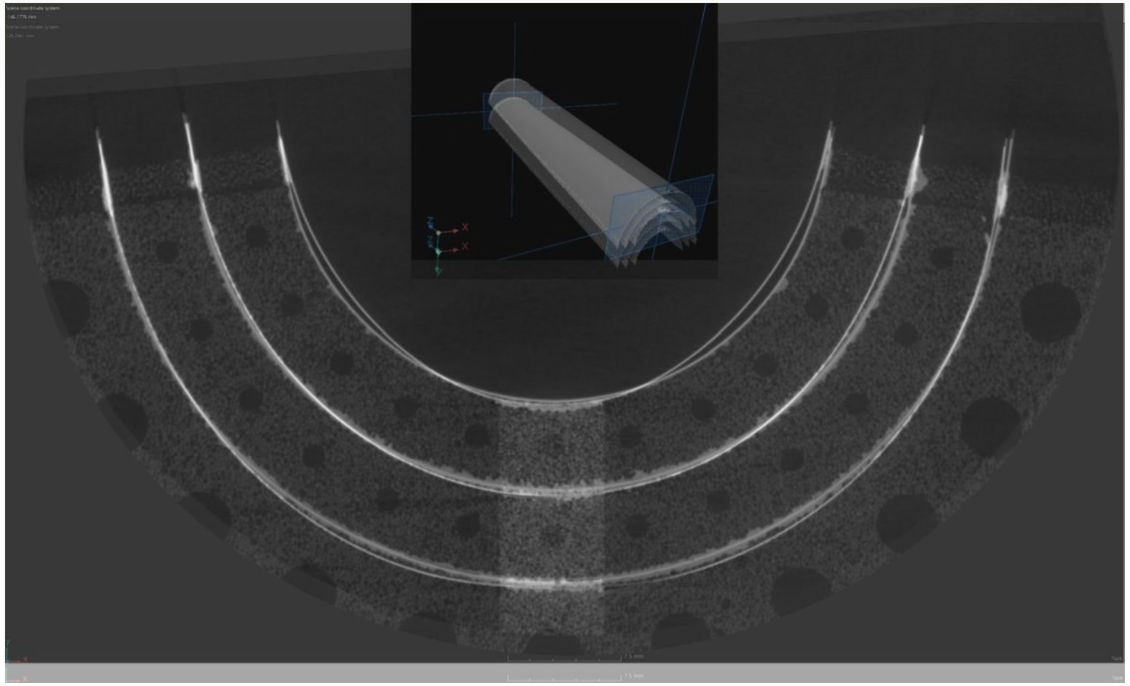


New improved version

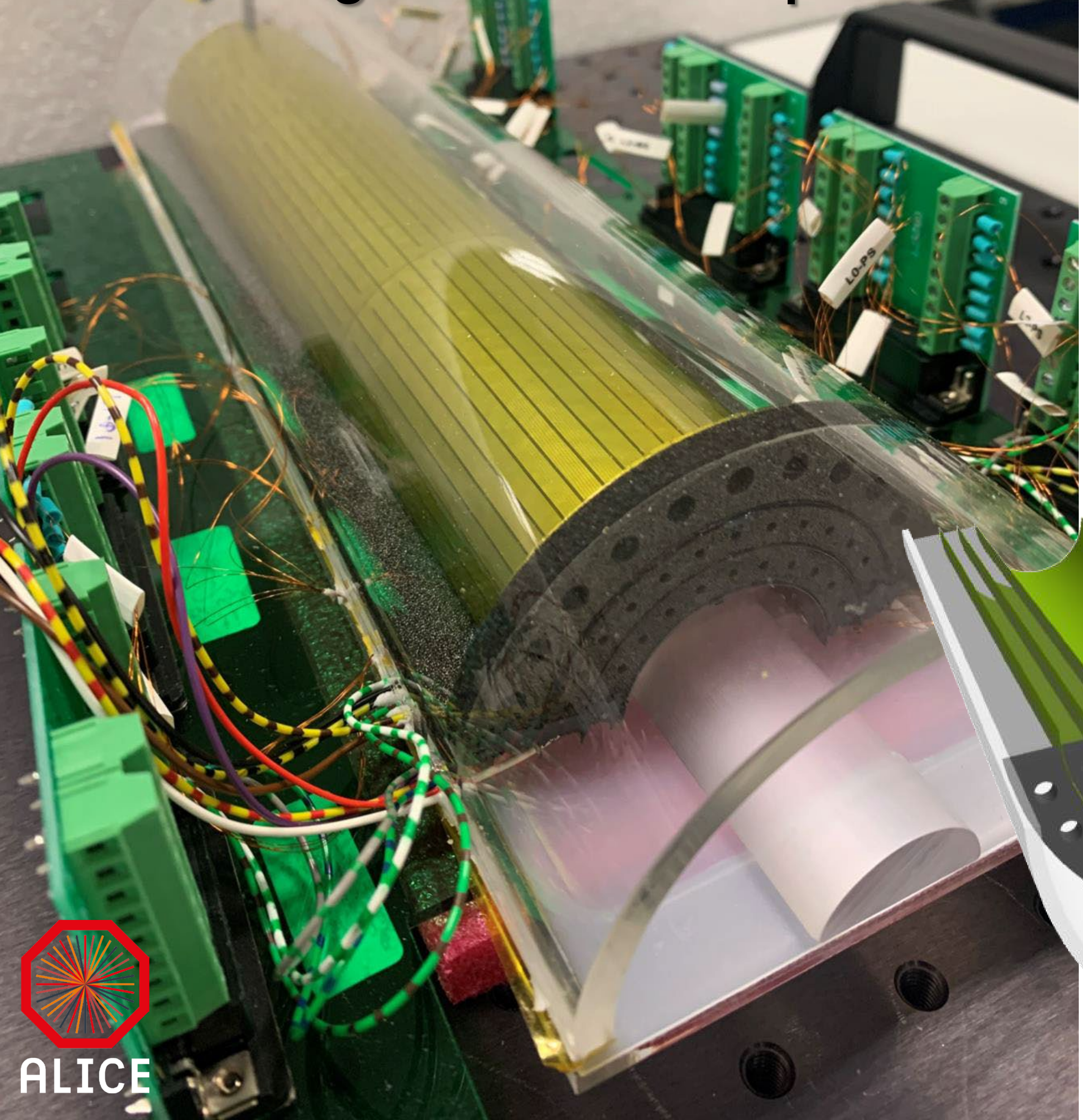
Geometry and stability improvements



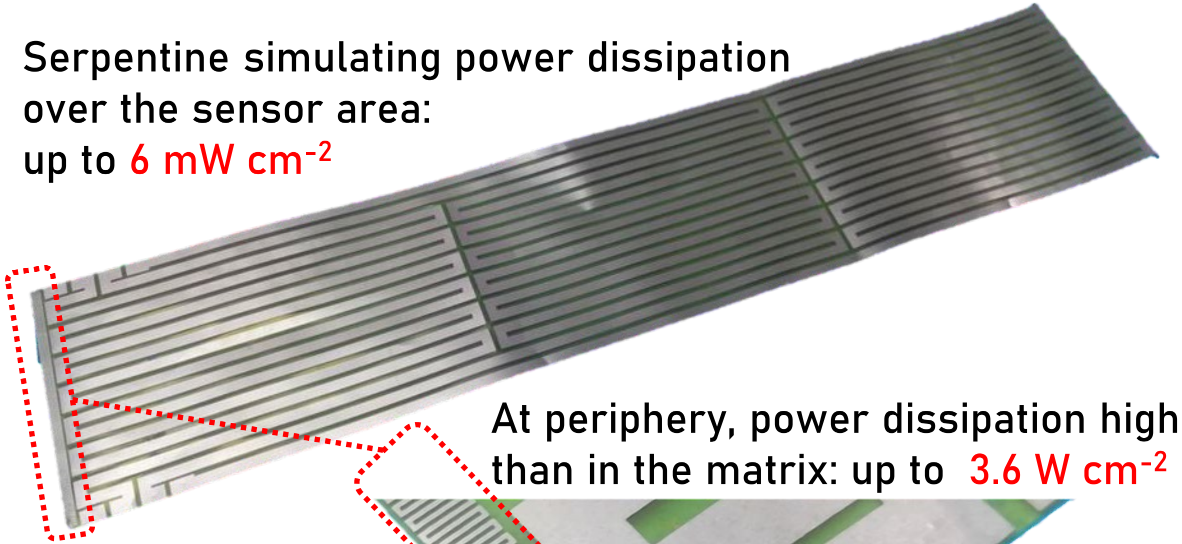




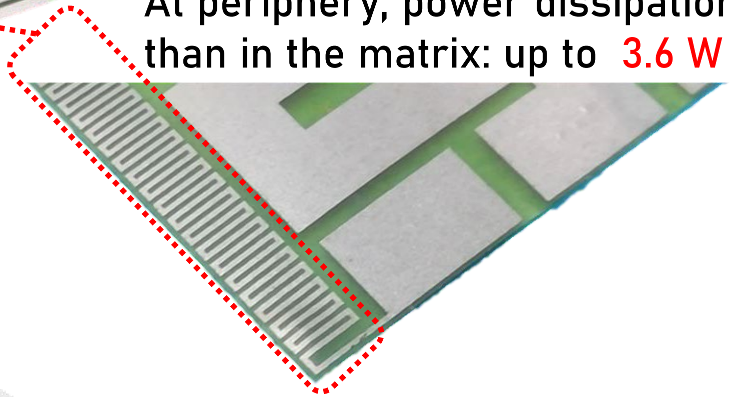
Air cooling test mock-up

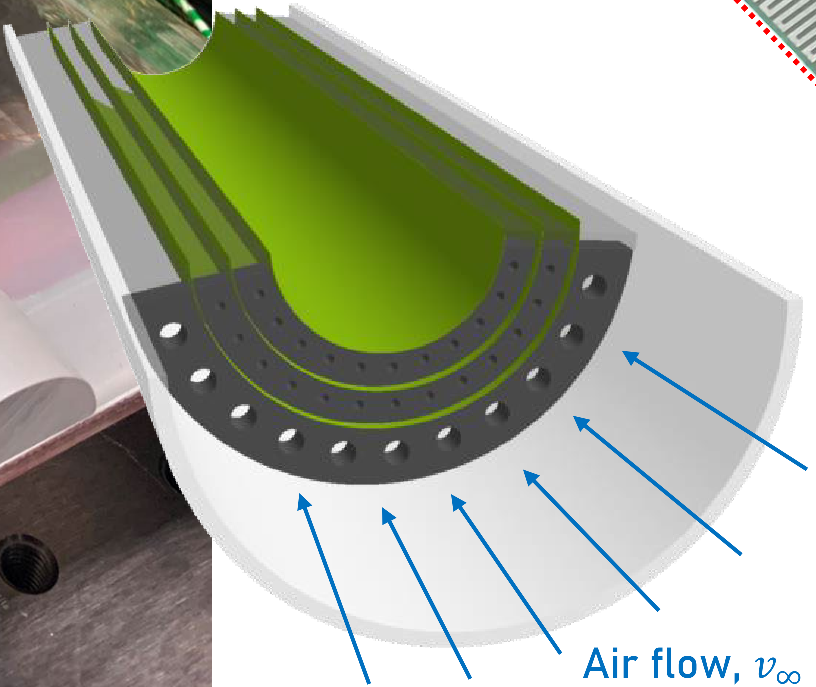


Serpentine simulating power dissipation over the sensor area: up to 6 mW cm^{-2}

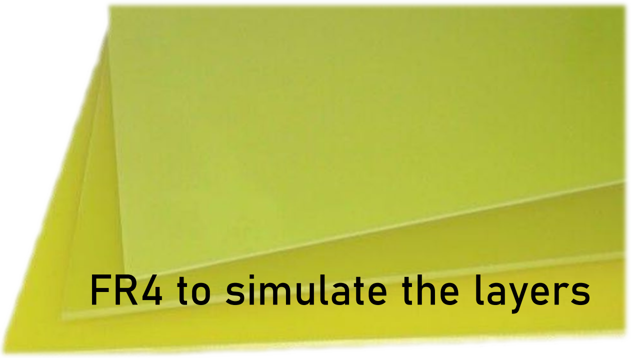


At periphery, power dissipation higher than in the matrix: up to 3.6 W cm^{-2}



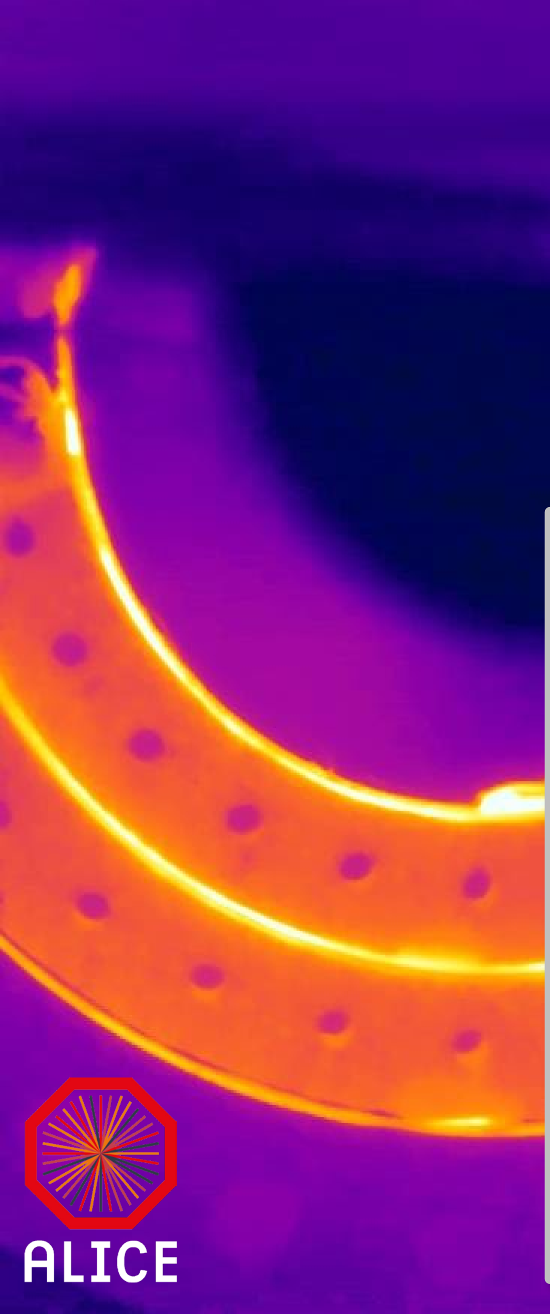


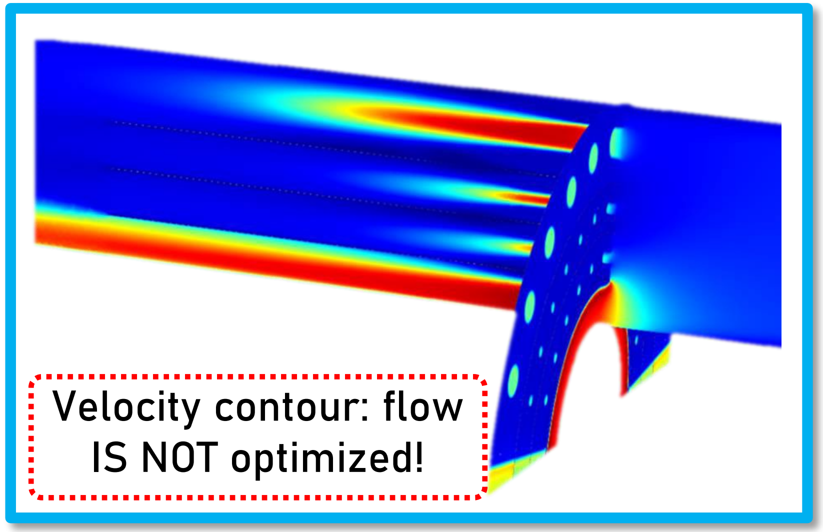
Air flow, $v_\infty = 6m/s$



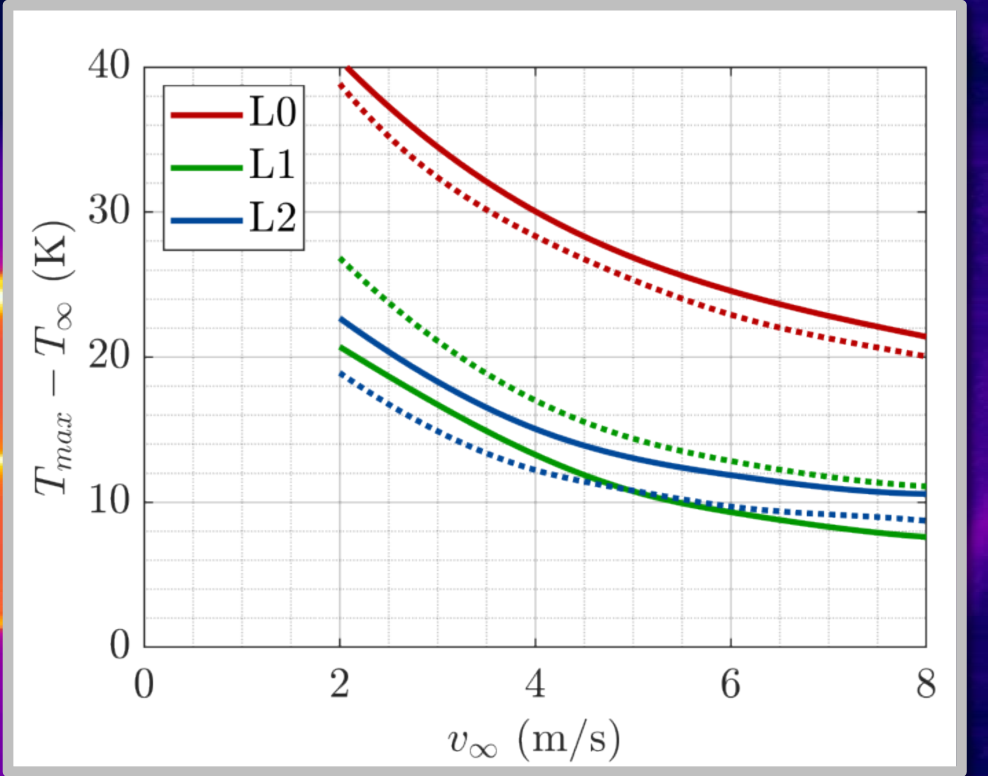
FR4 to simulate the layers

Air cooling measurements

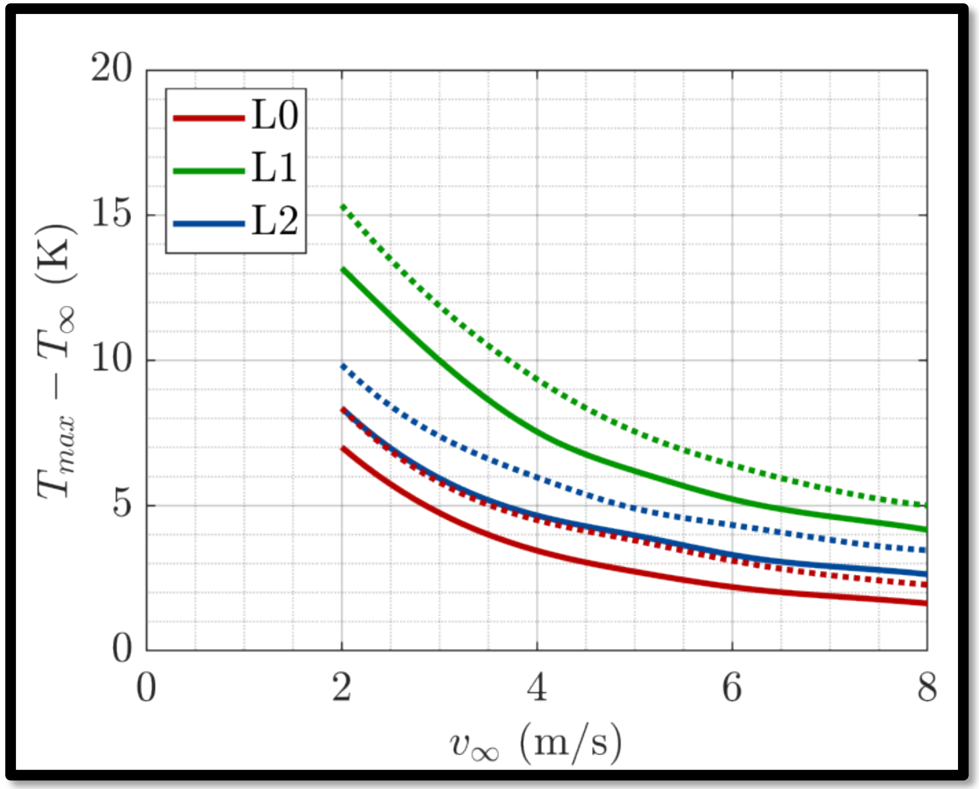




PERIPHERY max temperature variation [C]

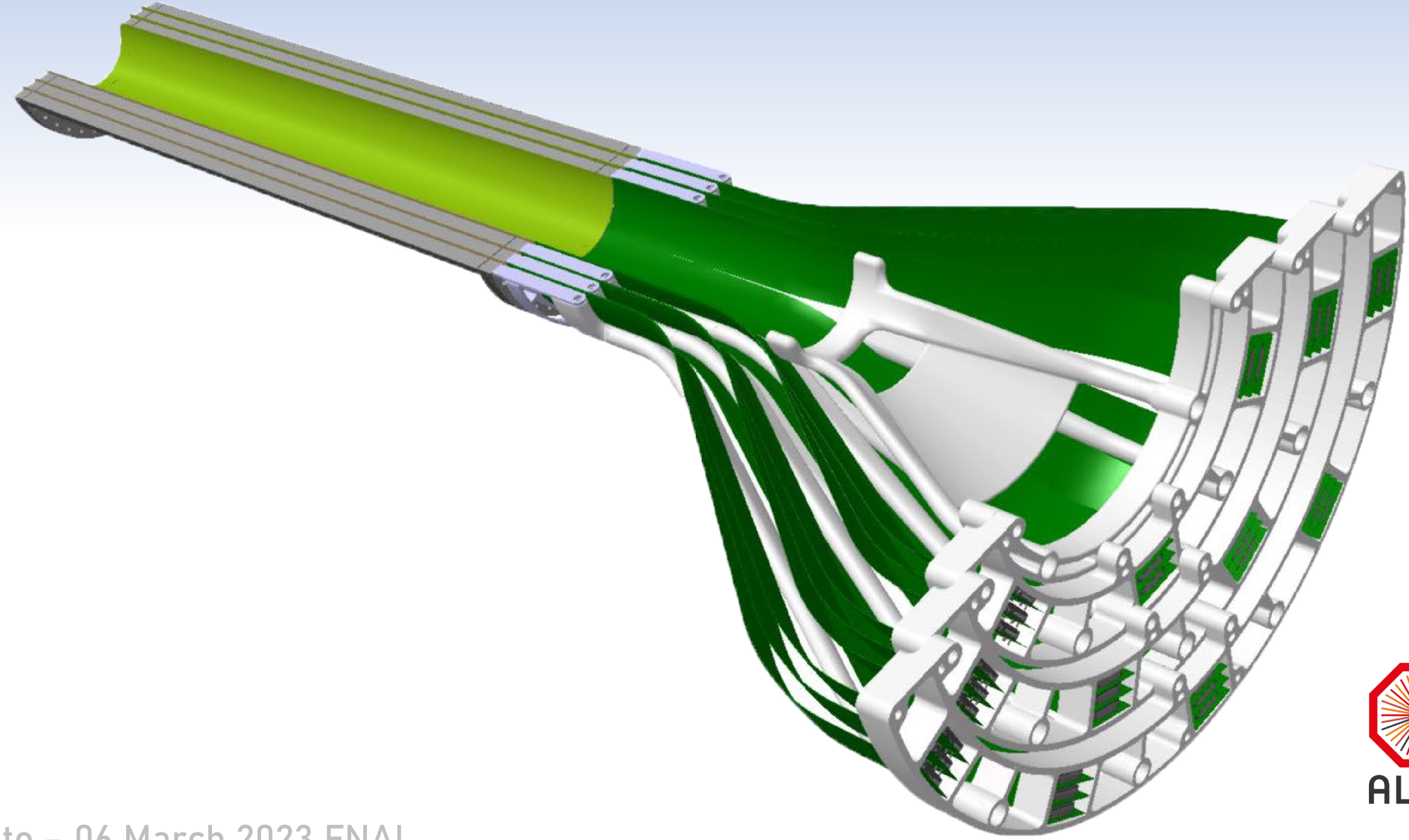


MATRIX max temperature variation [C]



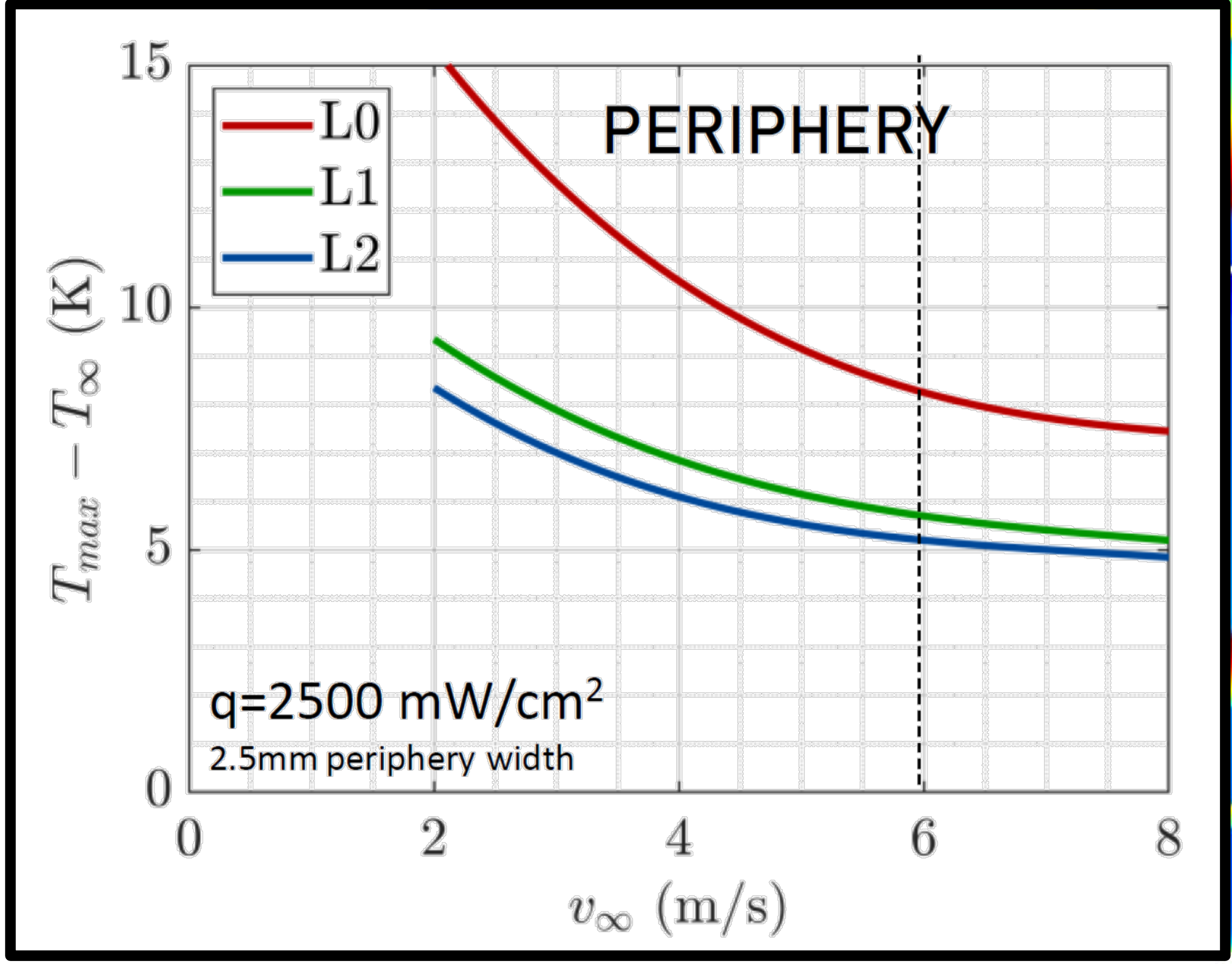
ALICE

Airflow optimization necessary

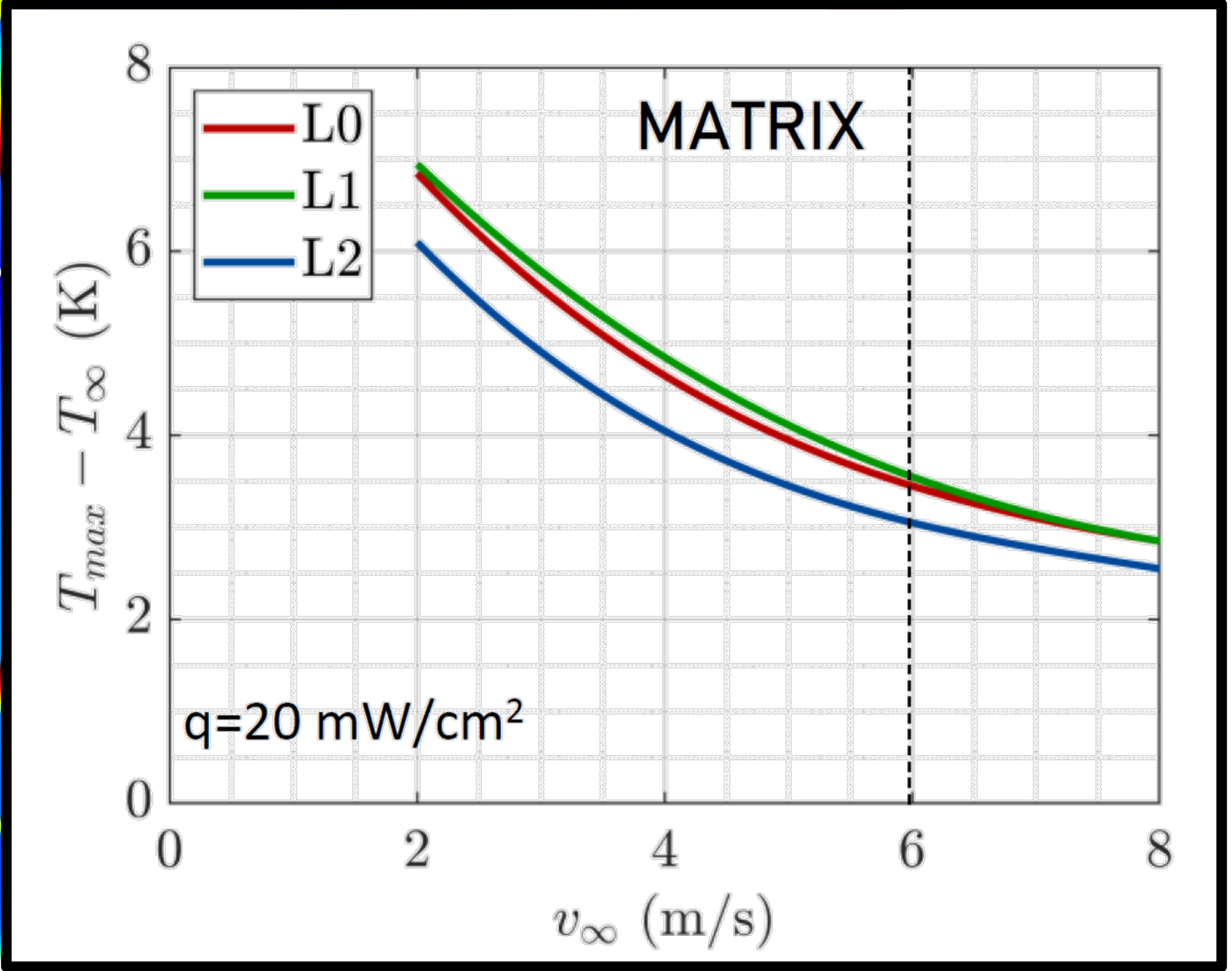


Airflow optimization - results

PERIPHERY max temperature variation [C]

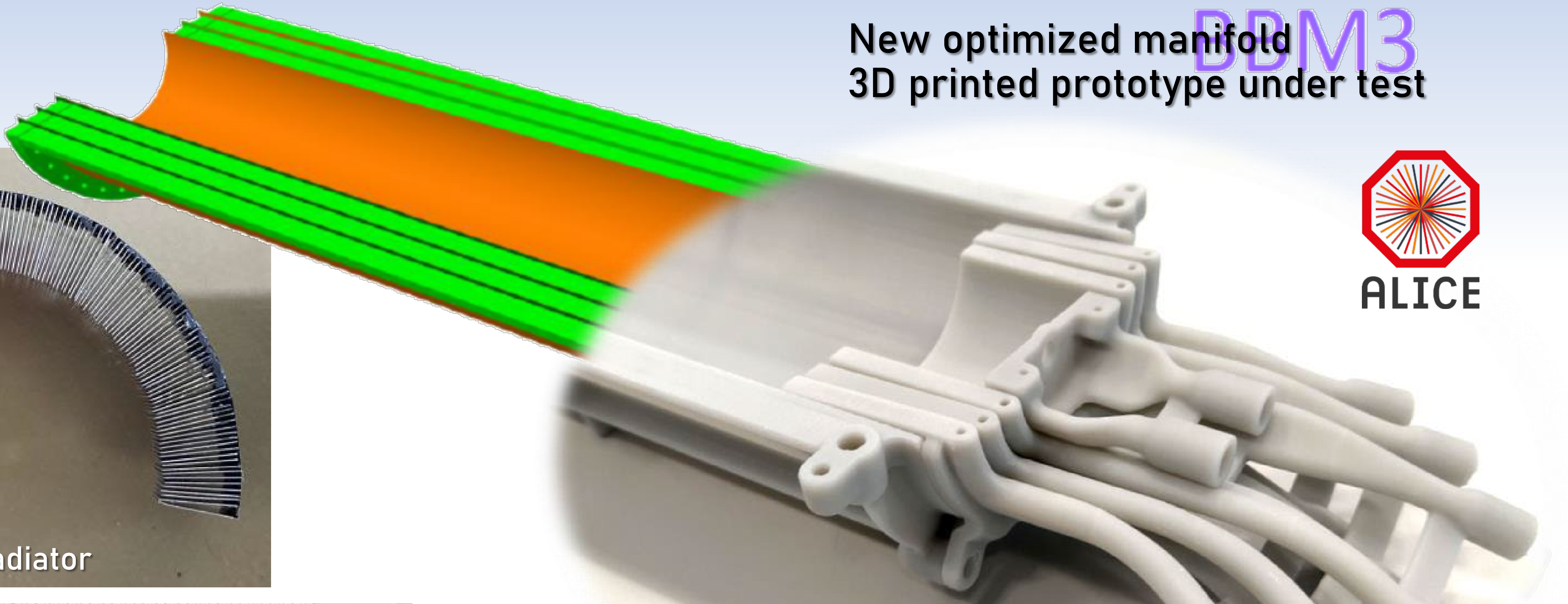


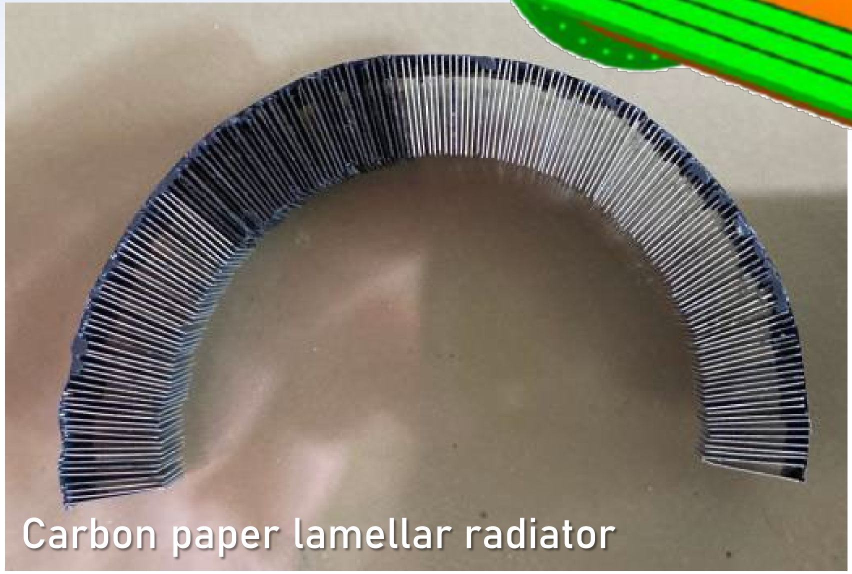
MATRIX max temperature variation [C]



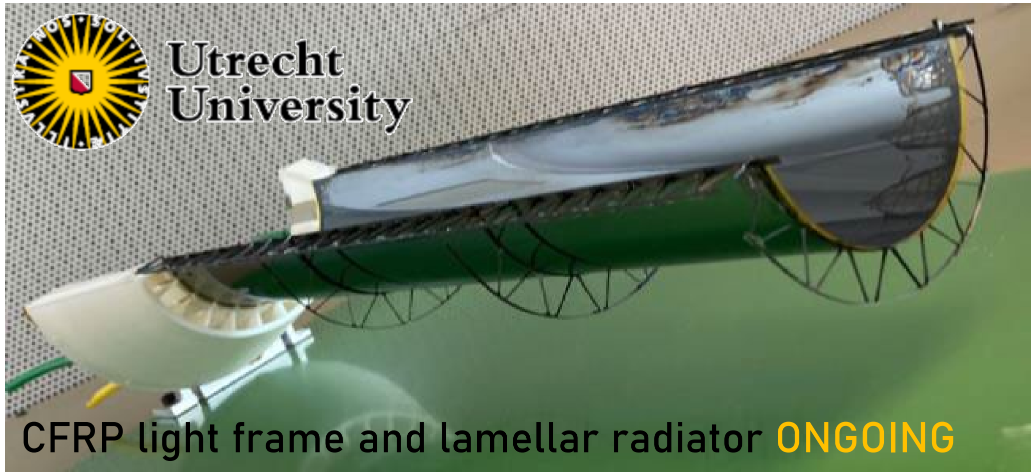
Air cooling – what's next

New optimized manifold BBM3
3D printed prototype under test

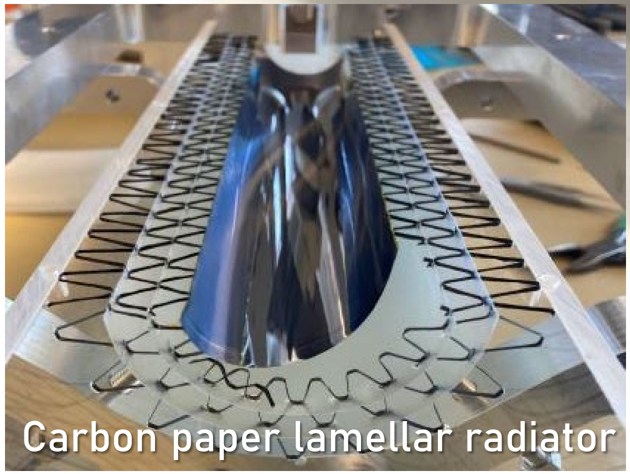




Carbon paper lamellar radiator



CFRP light frame and lamellar radiator ONGOING

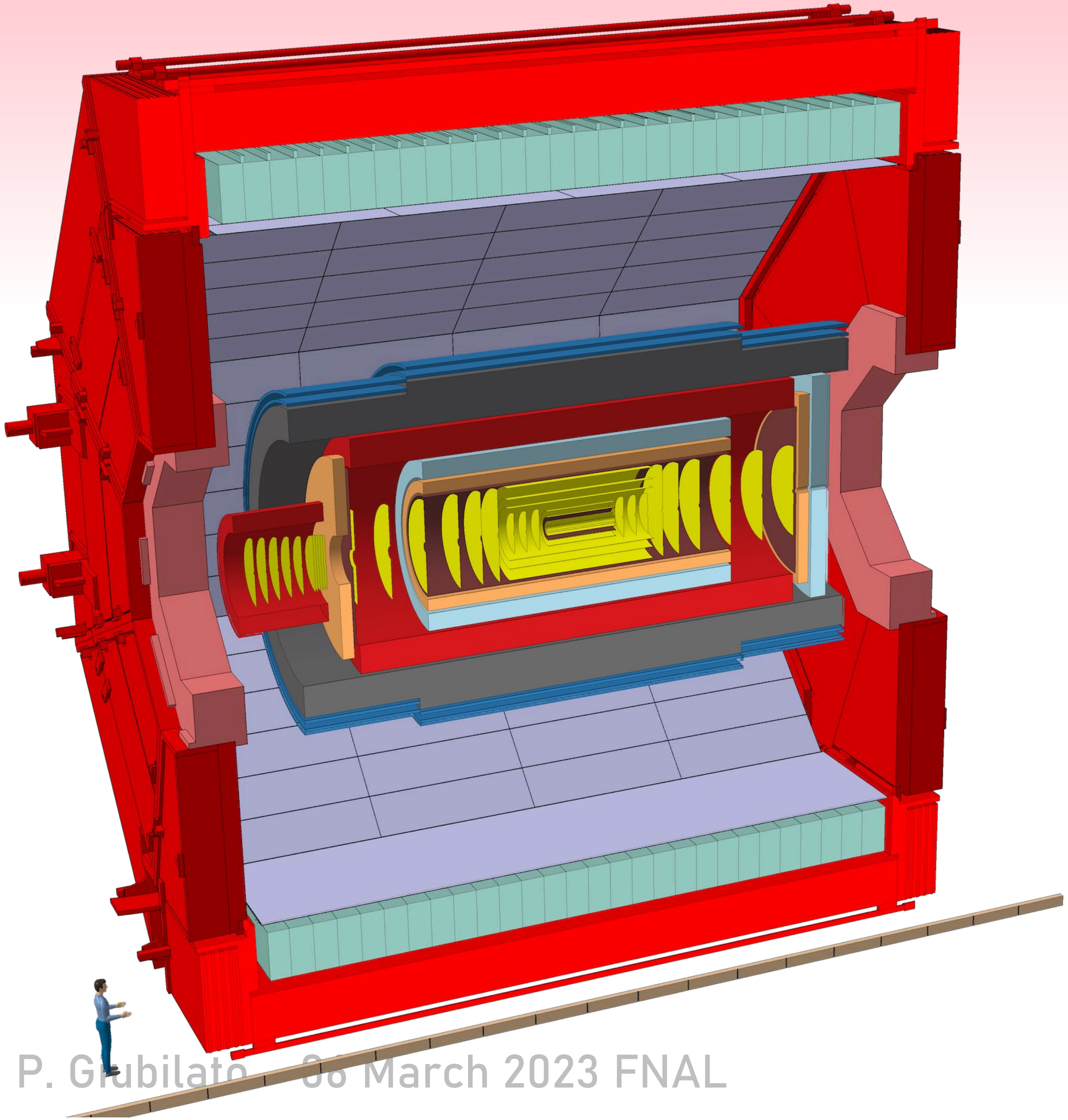


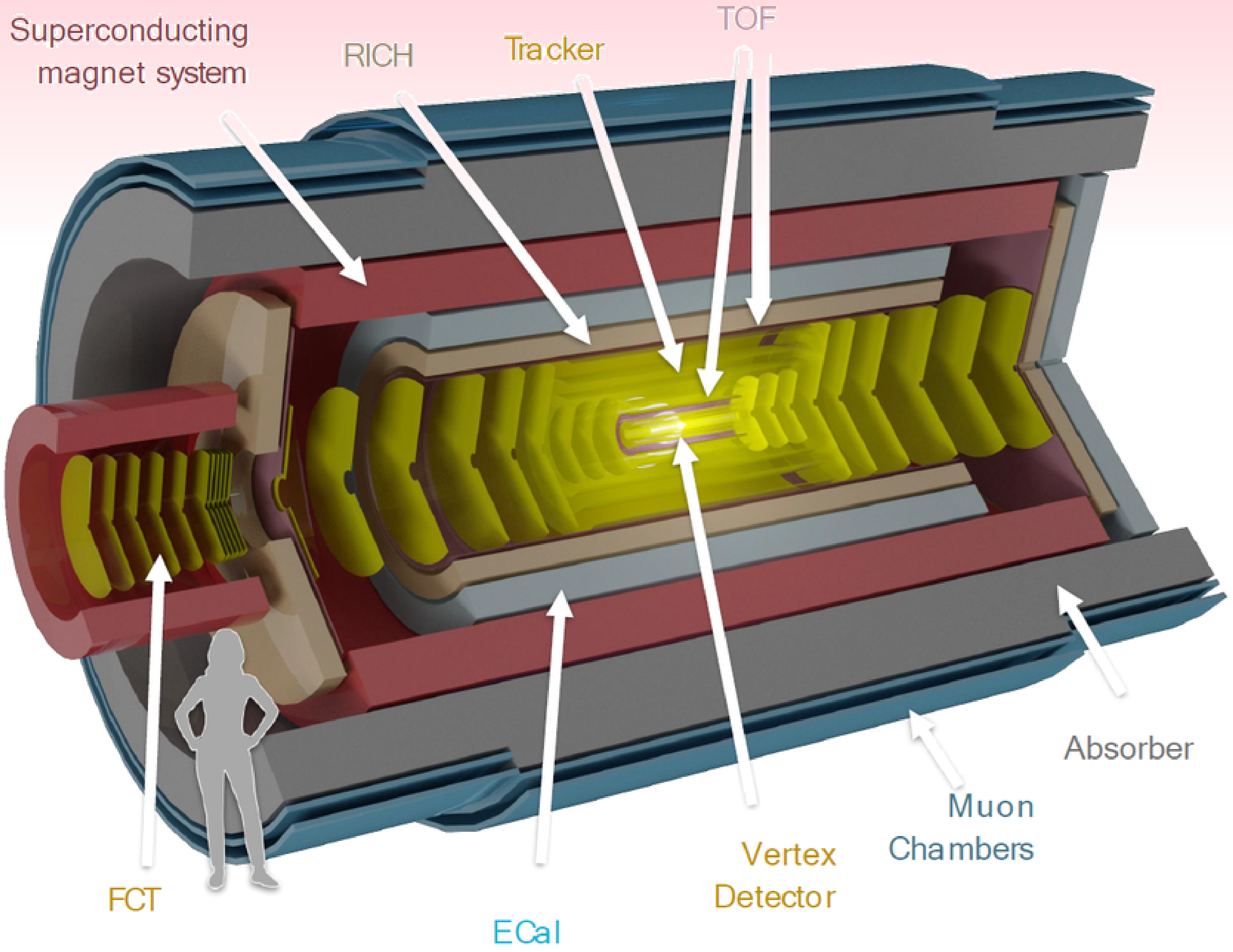
Carbon paper lamellar radiator

Next step

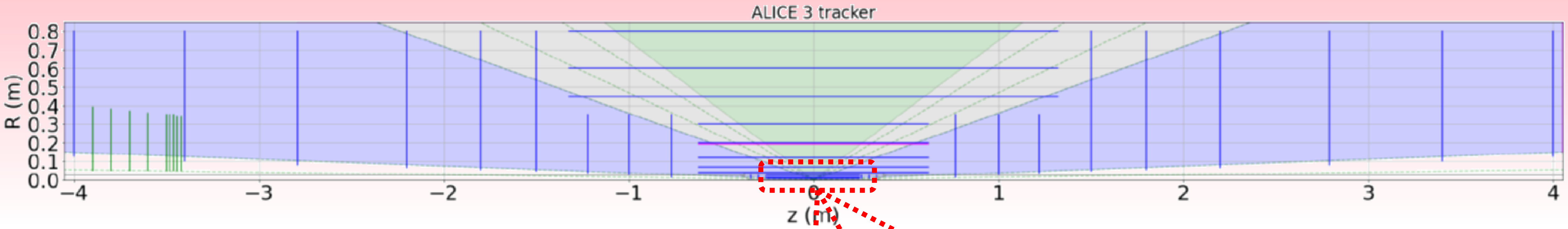
Getting closer

From current ALICE to a VERY compact detector





A large area tracker



10 barrels, 11 discs
inner-most part within beam pipe

- large active area: ~60 m^2
- low material budget: 0.1% X0

inner layer – less than ITS2, while being larger

- high spatial resolution: 2.5 µm

Layer	Material thickness (% X_0)	Intrinsic resolution (µm)	Barrel layers: Length ($\pm z$) (cm)	Barrel layers: Radius (r) (cm)	Forward discs: Position ($\lvert z \rvert$) (cm)	Forward discs: R_{in} (cm)	Forward discs: R_{out} (cm)
0	0.1	2.5	50	0.50	26	0.005	3
1	0.1	2.5	50	1.20	30	0.005	3
2	0.1	2.5	50	2.50	34	0.005	3
3	1	10	124	3.75	77	0.05	35
4	1	10	124	7	100	0.05	35
5	1	10	124	12	122	0.05	35
6	1	10	124	20	150	0.05	80
7	1	10	124	30	180	0.05	80
8	1	10	264	45	220	0.05	80
9	1	10	264	60	279	0.05	80
10	1	10	264	80	340	0.05	80
11	1				400	0.05	80

Improving ITS3 5 µm vertex point resolution to 2.5 µm or better…

Pointing resolution (multiple scattering regime)

$$\sigma_p \propto r_0 \sqrt{\frac{x}{X_0}}$$

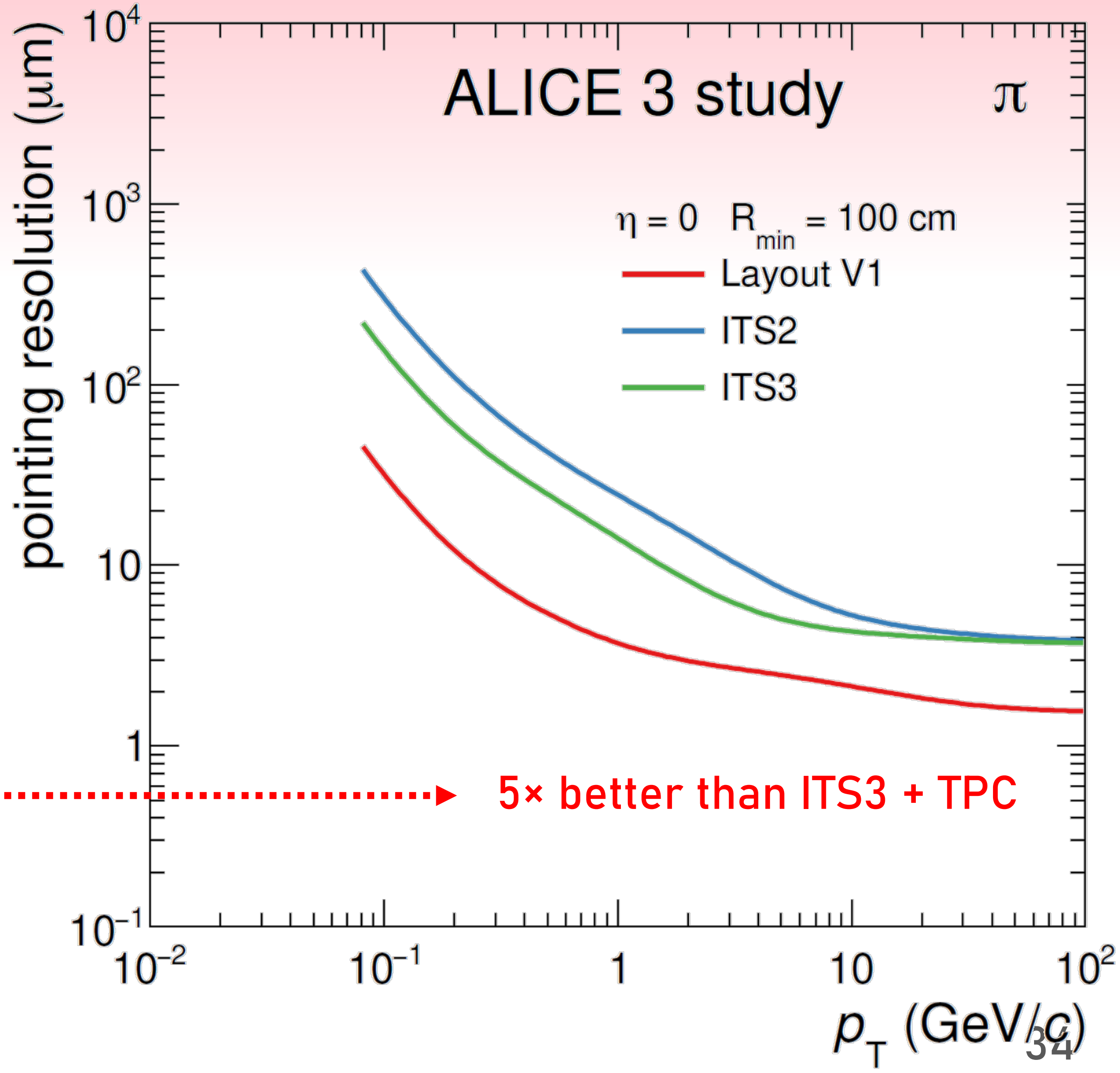
Impossible to improve upon ITS3 here

Necessary to get closer to the beam

to get to 10 µm @ pT = 200 MeV/*c* radius and material of first layer become crucial.

Minimal radius given by required aperture

- R ≈ 5 mm at top energy
- R ≈ 15 mm at injection energy



5× better than ITS3 + TPC

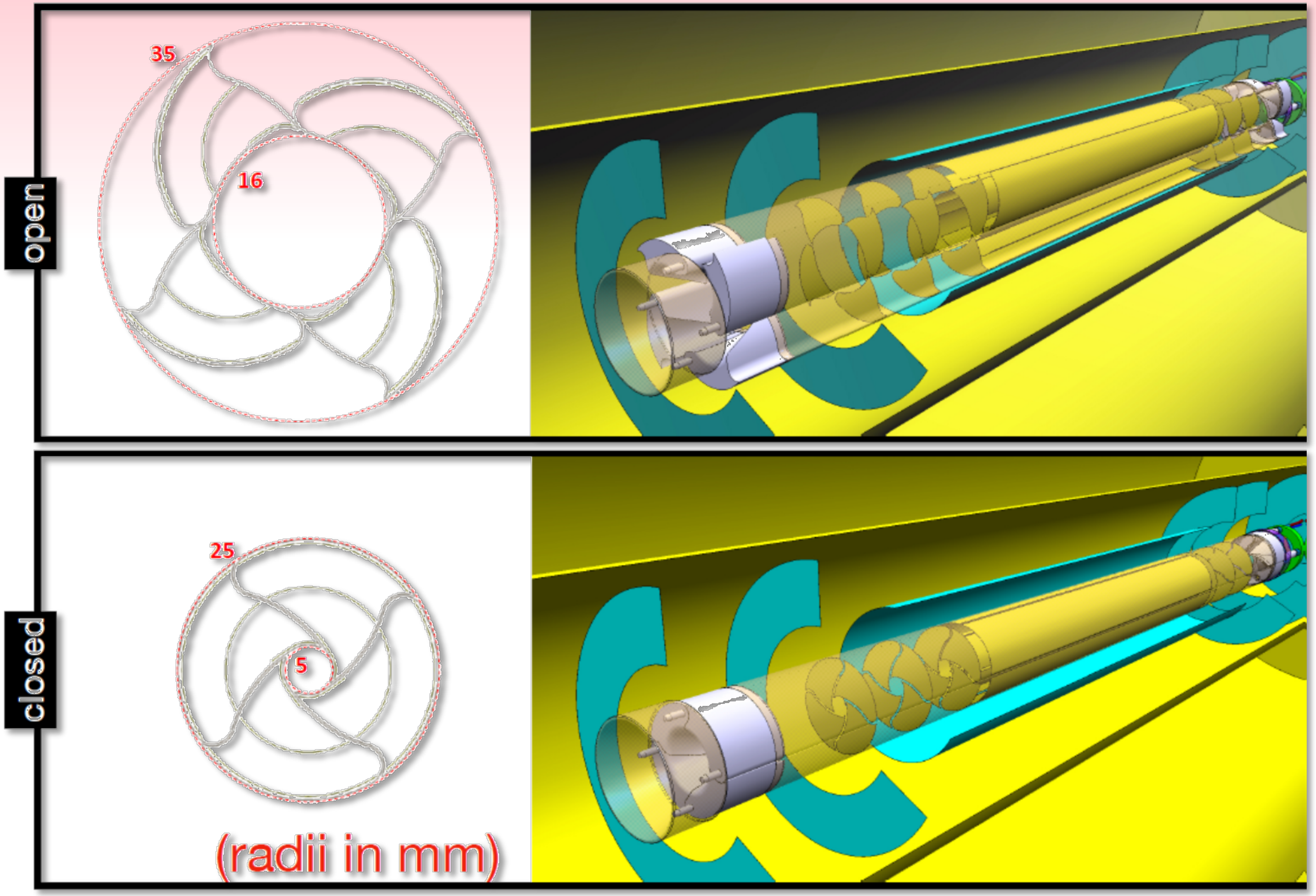
Requires a radical design of the first 3 layers

- 3 layers within beam pipe (in secondary vacuum) radii of 5 - 25 mm, with following specs:

- wafer-sized, bent MAPS
- 1 ‰ X_0 per layer

ITS3 tech

- σ_{pos} ~2.5 µm →
  - 10 µm pixel pitch
  - 100 MHz cm^{-2} rate
  - < 50 mW cm^{-2} power



Foreseen operational figures*

Layer	Radii	Flux		Bandwidth [Gb s^{-1}]			Power	Radiation	
	Cm	[MHz cm^{-2}]	[GHz lyr^{-1}]	Hits	Noise	Total	[W]	NIEL [1 Mev $n_{eq}cm^{-2}$]	TID [Mrad]
0	0.5	96	17	274	1.0	275	13	9×10^{15}	288
1	1.2	16	7.3	117	2.4	119	32	1.6×10^{15}	50
2	2.5	3.8	3.6	57	5.0	62	66	3.6×10^{14}	12
3	3.8	1,7	1.8	28	0.7	79	175	1.6×10^{14}	5
4	7	0.48	1.2	18	1.4	43	131	4.6×10^{13}	1.5
5	12	0.16	0.8	13	2.4	27	224	1.6×10^{13}	0.5
6	20	0.058	0.6	9.9	4.0	19	374	5.6×10^{12}	0.2
7	30	0.026	0.5	7.9	6.0	16	561	2.5×10^{12}	0.08
8	45	0.012	0.6	9.6	19.1	33	1792	1.1×10^{12}	0.04
9	60	6.5×10^{-3}	0.5	8.2	25.5	36	2389	6.3×10^{11}	0.02
10	80	3.7×10^{-3}	0.4	6.8	34.0	42	3185	3.5×10^{11}	0.01

*
- bandwidth: 16 bit/hit, single pixel clusters
- radiation load: 50 months of 24 MHz pp interactions
- Fake-hit rate: 10^{-8} px^{-1} $event^{-1}$ @ 40 MHz readout rate

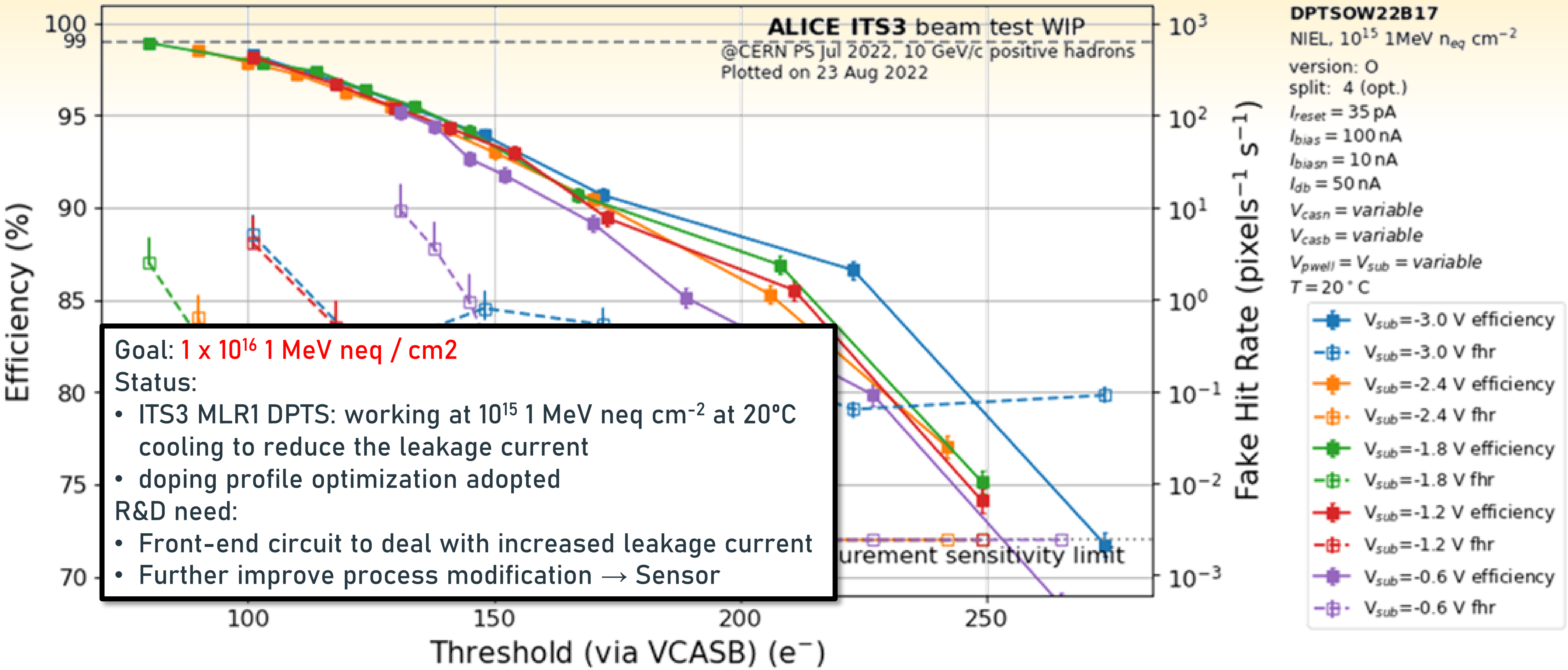
Foreseen operational figures*

Item	Unit	Next ITS		ITS3	ITS2
	Cm	Vertex	Tracker		
Pixel pitch [µm]	[µm]	9 ÷ O(10×10)	28 ÷ O(50×50)	O(20×20)	28
Spatial resolution [µm]	[µm]	2 ÷ 2.5	2 ÷ 10	5	5
Time resolution [ns]	[ns]	10 ÷ 100	10 ÷ 100	100 ÷ O(1000)	O(1000)
Shaping time [ns]	[ns]	25 ÷ 200	25 ÷ 200	200 ÷ O(5000)	O(5000)
Fake hit rate	[px^{-1} $event^{-1}$]	$< 10^{-8}$	$< 10^{-8}$	$< 10^{-7}$	$<< 10^{-6}$
Power consumption	[mW cm^{-2}]	70 (+75%)	20	20 (matrix)	30 ÷ 40
Hit flux	[MHz cm^{-2}]	20 ÷ 94		8.5	5
NIEL	[1 MeV n_{eq} cm^{-2}]	1×10^{16}		3×10^{12}	3×10^{12}
TID	[Mrad]	300 ÷ 1000	5	0.3	0.3

- In red: likely not achievable (no idea at the moment)
- In yellow: not strictly necessary, more a goal
- In blue: more realistic, expected goal

65 nm proven technology – 10^{15} 1 MeV n_{eq} cm^{-2} measureents

- Proven by R&D53 (ATLAS – CMS)
- Comparable results in Tower-Jazz 65 nm



Goal: 1 x 10^{16} 1 MeV neq / cm2

Status:

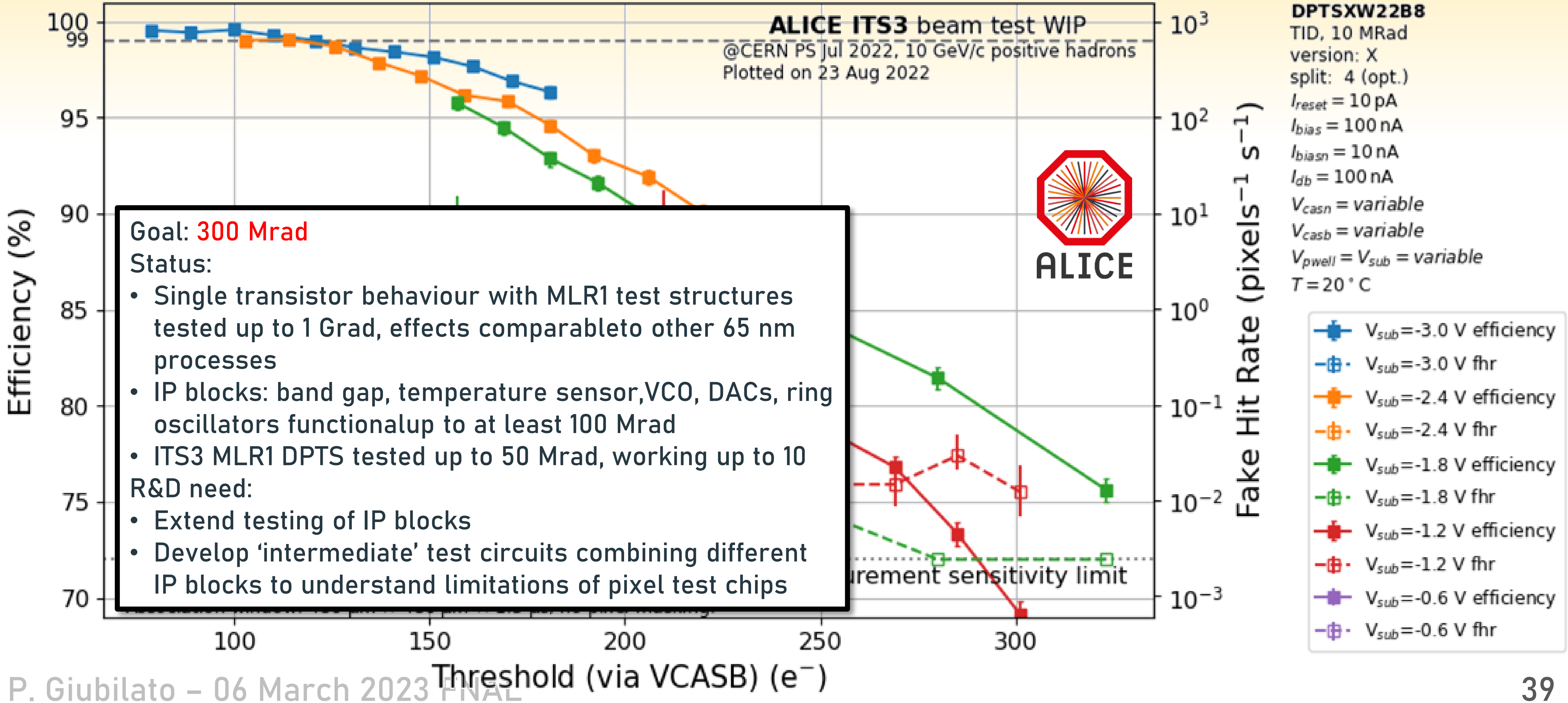
- ITS3 MLR1 DPTS: working at 10^{15} 1 MeV neq cm^{-2} at 20°C cooling to reduce the leakage current
- doping profile optimization adopted

R&D need:

- Front-end circuit to deal with increased leakage current
- Further improve process modification → Sensor

65 nm proven technology – 10 Mrad measurements

- Proven by R&D53 (ATLAS – CMS)
- Comparable results in Tower-Jazz 65 nm



Goal: 300 Mrad

Status:
- Single transistor behaviour with MLR1 test structures tested up to 1 Grad, effects comparableto other 65 nm processes
- IP blocks: band gap, temperature sensor,VCO, DACs, ring oscillators functionalup to at least 100 Mrad
- ITS3 MLR1 DPTS tested up to 50 Mrad, working up to 10

R&D need:
- Extend testing of IP blocks
- Develop ‘intermediate’ test circuits combining different IP blocks to understand limitations of pixel test chips

Power consumption and distribution likely the BIGGEST issues

Consumption

Biggest contributors:

- Front-end circuits: use maximum possible pixel size (enters quadratically)
  - optimise the charge collection carefully
  - optimisation of the time resolution
- On-chip data transmission (see dedicated slide)

▪ Status: – No comparable chip available, differ in terms of pixel size, hit rate capabilities, time resolution,…

Distribution

Vertex Detector

- Stitched chip of 25 cm length (chip split in *z*-direction) and 1 cm width*
- 70 mW cm^{-2} power consumption
- On-chip metal layers for power distribution
- Aluminium, O(1µm) thick
- 20% / 2 mm width used for supply 0.5 Ω/cm * 25 cm = 13 Ω
- Chip operating at 1 V – Average current along a 1 cm wide, 25 cm long chip: 0.9 A
- 3 V voltage drop

Power consumption multiplied!

Outer Tracker

- Parallel powering of chips low voltages, high currents
- sub-optimal in terms of material budget and space

Power distribution alternatives

Serial powering
- Current reduction of roughly a factor of 10
- Complicated to realize with stitching: substrate is acting as common reference (unless depletion zones separate the domains)
- safer option use separate chips instead of stitching

Status:
- in use for ATLAS and CMS LS3 tracker upgrades

R&D need:
- LDO shunt regulator
- Prototyping of a module using existing MAPS

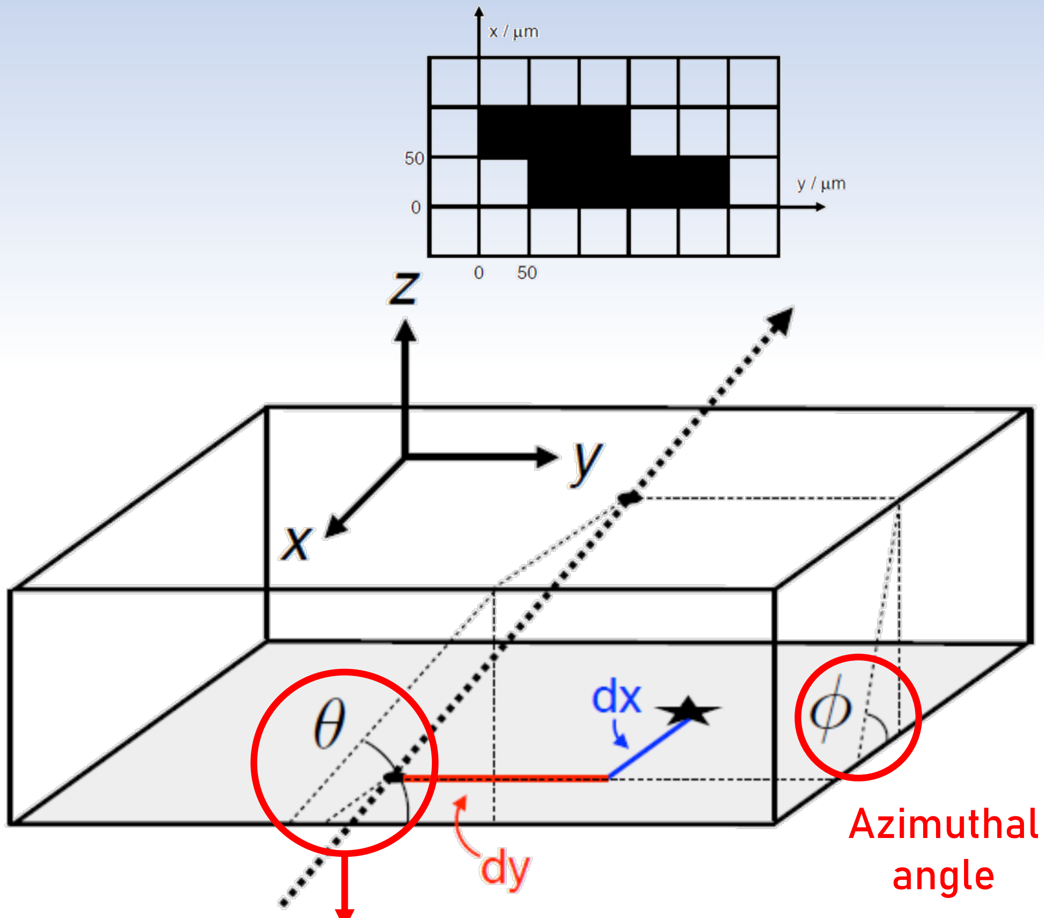
Redistribution Layer (RDL)
- Additional copper and polyamide layer(s) added to the wafer
- Trade off between resistance and material budget
- Impacts the flexibility

R&D need:
- Prototyping of RDL assemblies
- Study of the mechanical properties (i.e. bending and thermal cycles) of RDL assemblies

Do not get crazy on small pixels

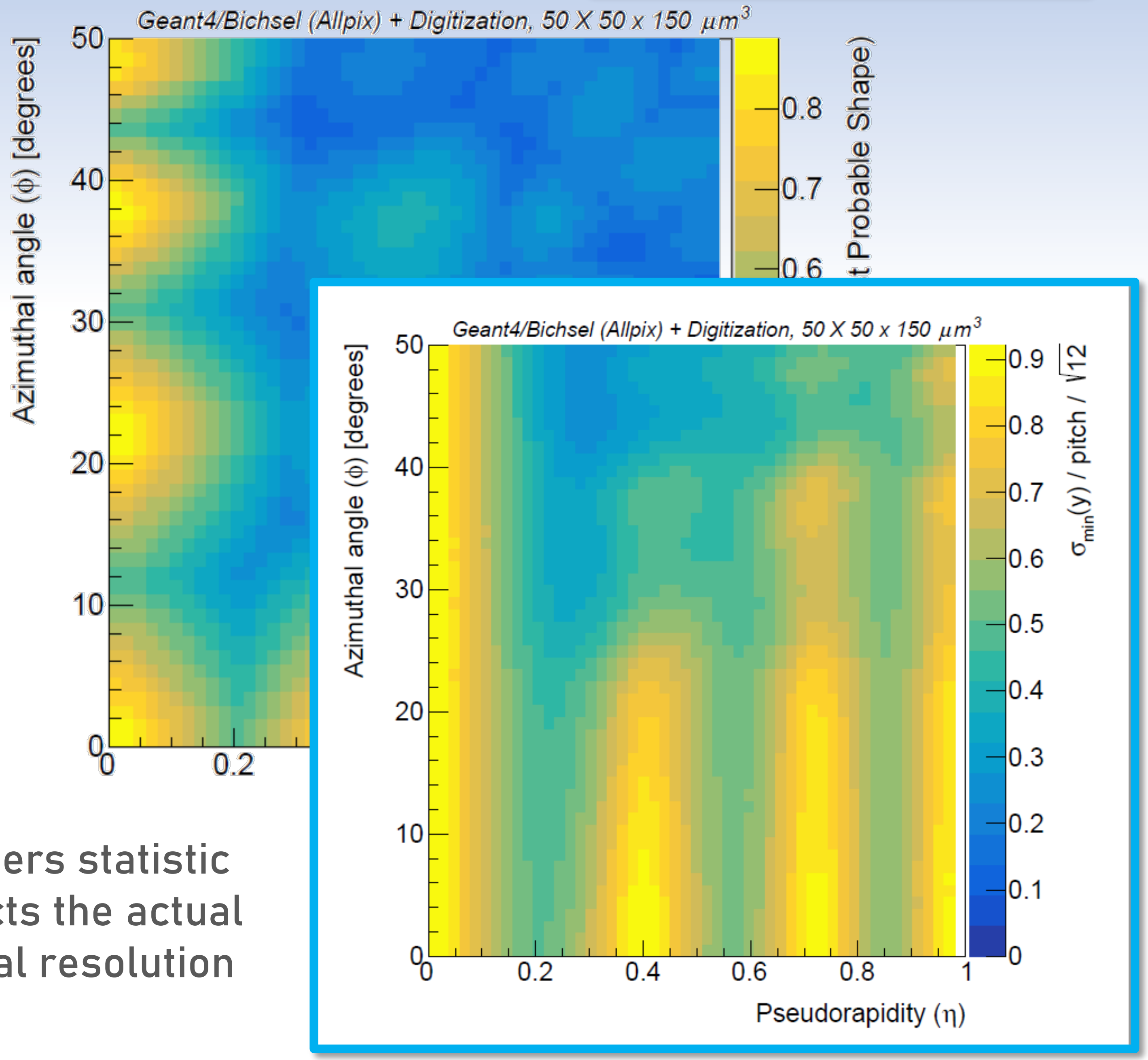
An insight on actual binary pixel resolution

DOI: 10.48550/arXiv.1711.00590



Polar angle

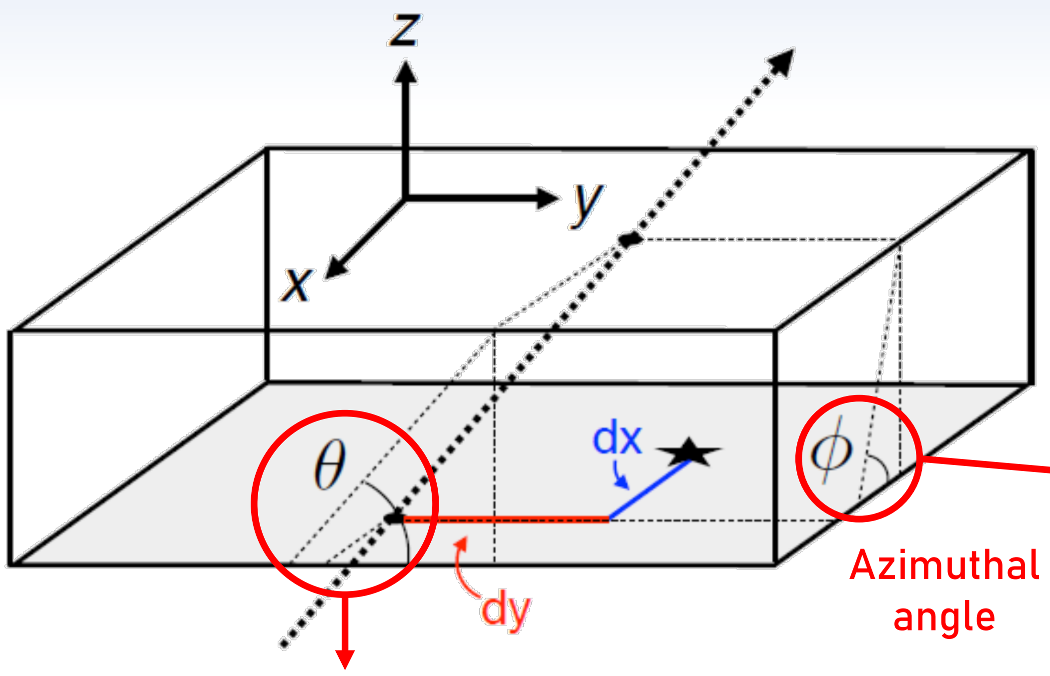
$$\eta = -\ln\left(\tan\frac{\theta}{2}\right)$$



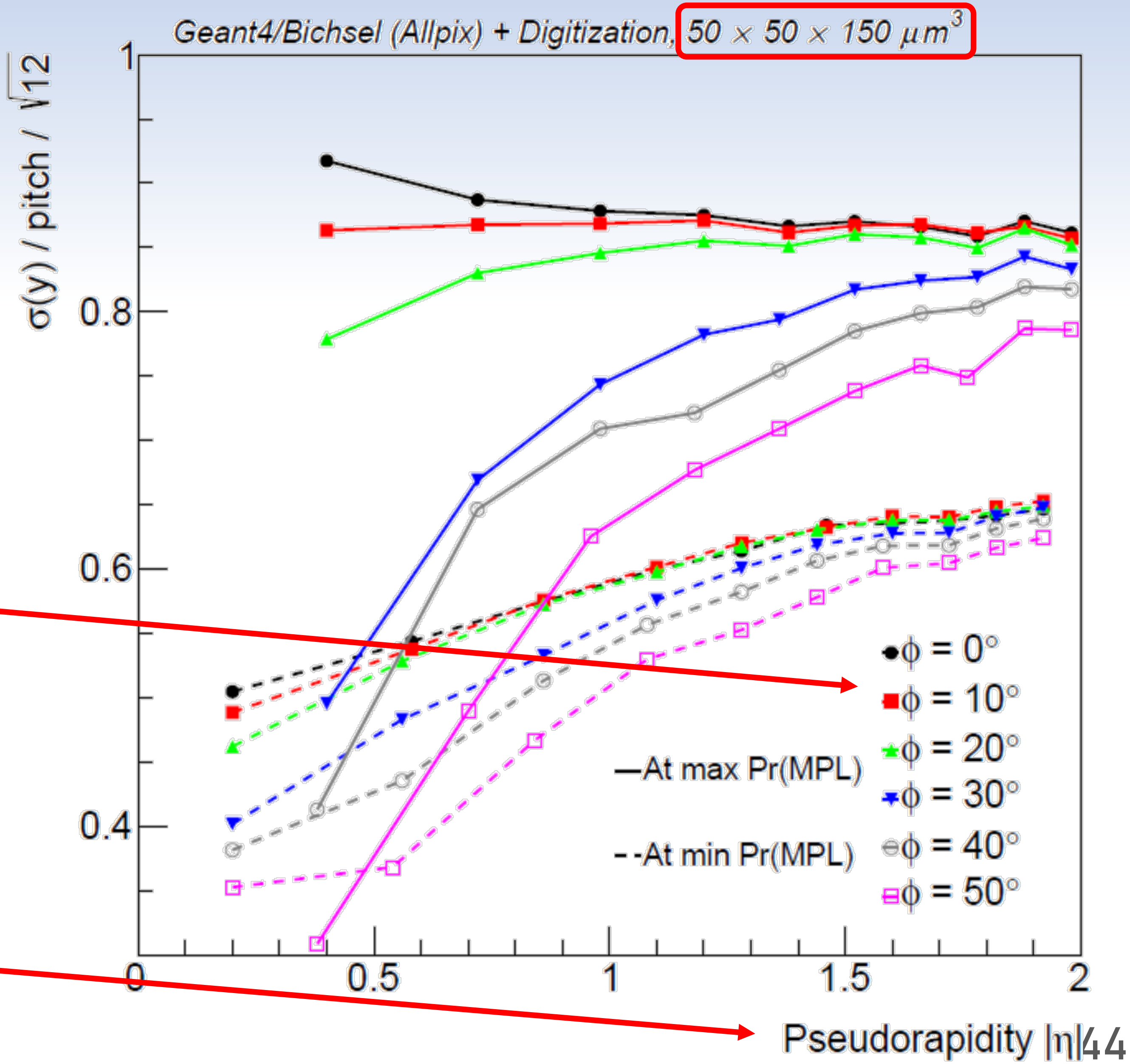
Clusters statistic impacts the actual spatial resolution

An insight on actual binary pixel resolution

DOI: 10.48550/arXiv.1711.00590



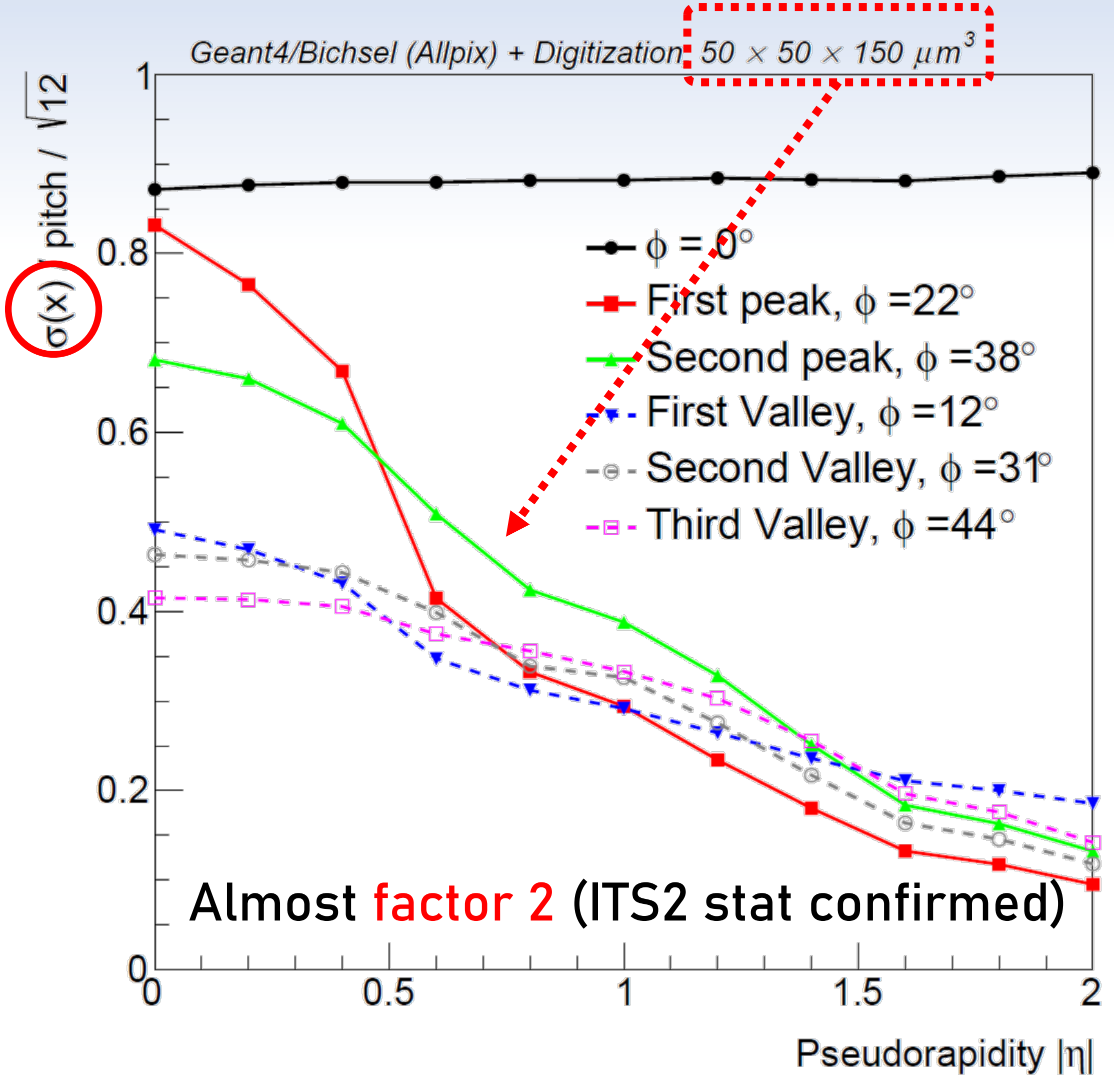
$$\eta = -\ln\left(\tan\frac{\theta}{2}\right)$$

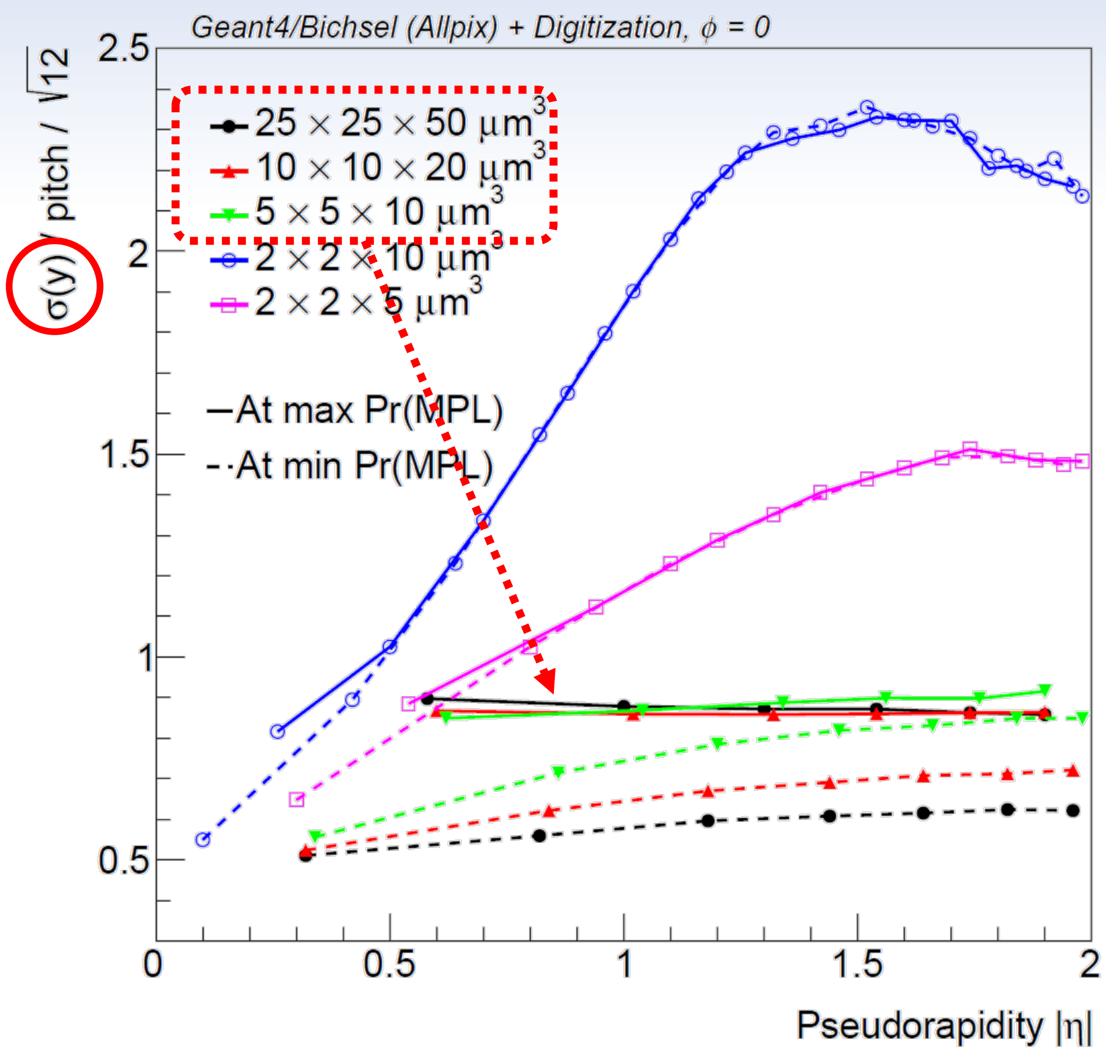


An insight on actual binary pixel resolution

DOI: 10.48550/arXiv.1711.00590

Bot x and y position resolution are actually better than the classical $1/\sqrt{12}$ assumption



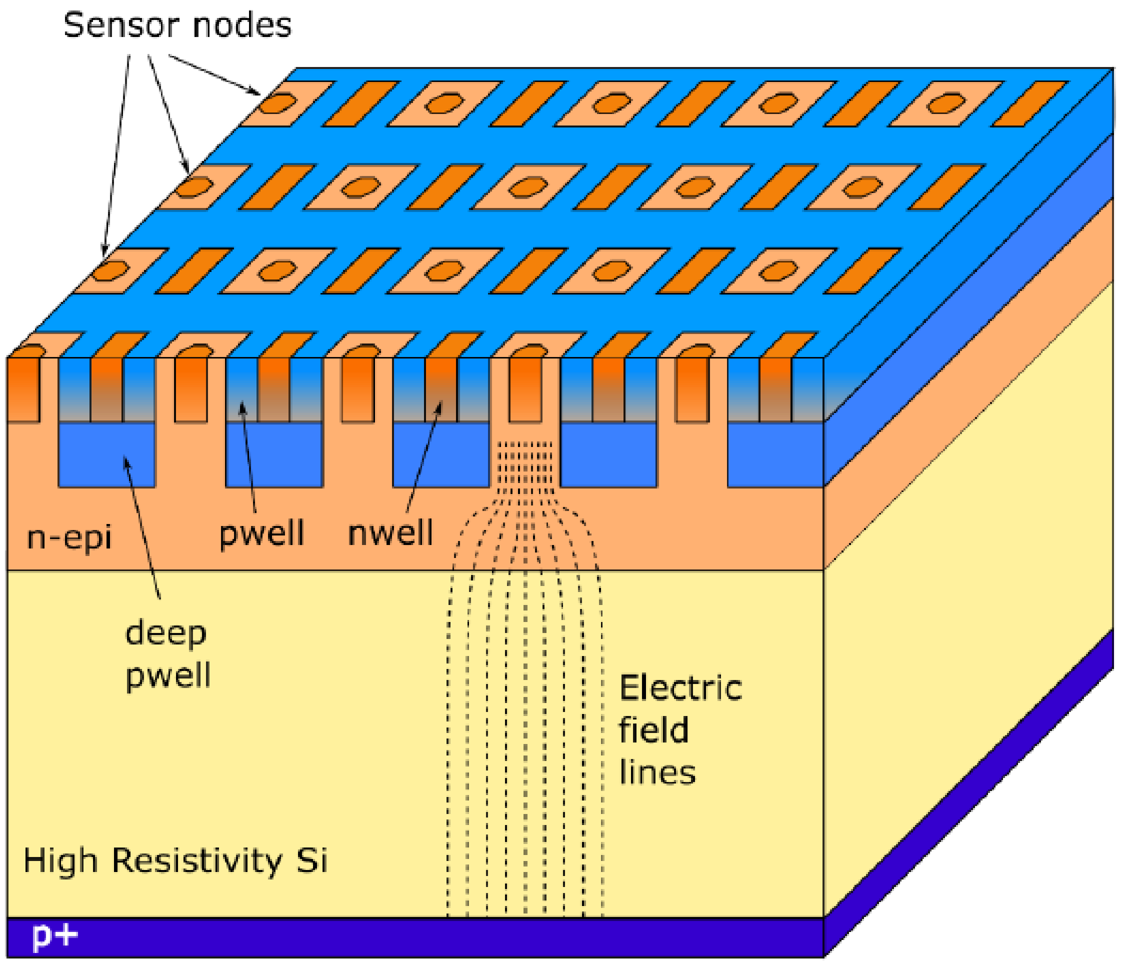


Timing also possible

ARCADIA sensor for timing R&D

Fully Depleted CMOS Sensors:

- Monolithic sensors
- Charge collected mainly by drift:
  - Fast collection time (≃ ns)
  - Better collection efficiency
  - Higher radiation tolerance
- n-on-n sensor concept
- A p+ boron-doped region at the backside of the n-substrate
- n-doped and p-doped wells for CMOS electronics
- 110 nm Technology (Lfoundry), 6 metal layers
- Only deep pwell as a custom implant
- Vback , negative bias, to the p+ contact to start full depletion
- Thickness from 50 µm to about 400 µm



ARCADIA sensor for timing – expected performance

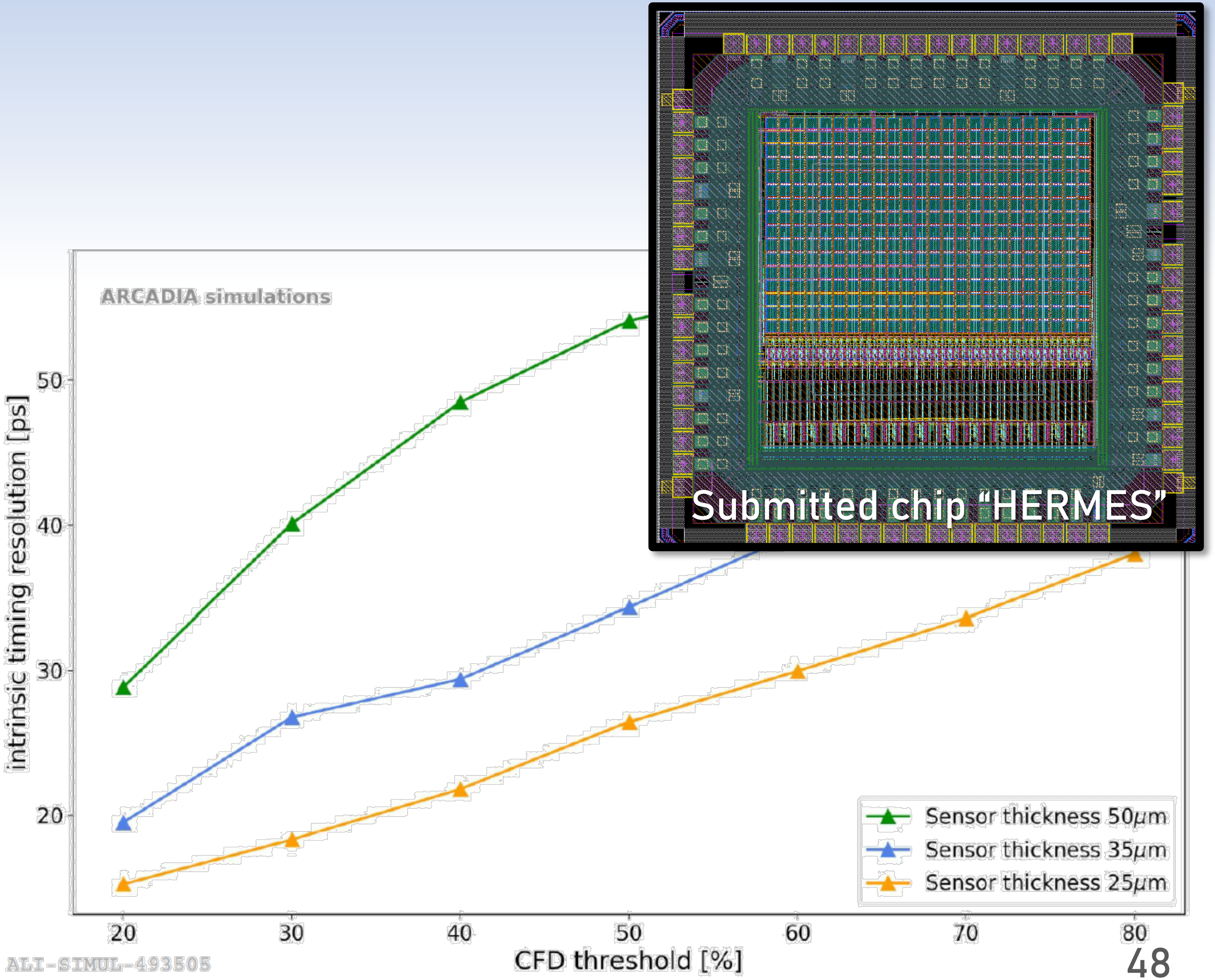
Stefano Durando

Sensor simulations:
▪ TCAD, Electric Field & Weighting Potential evaluation, ALLPix2, Pixels

Monte Carlo analysis
- Pitches: 50 - 10 µm
- Thicknesses: 25 - 35 - 50 µm

→ Resolution is 20÷30 ps for the 50 µm pitch

- Larger PAD sizes allow for a better field uniformity and better area efficiency
- Thinner sensors have a better time resolution
- Still, less charge is generated
- Increase in the electronics jitter
- Gain into the monolithic sensor?

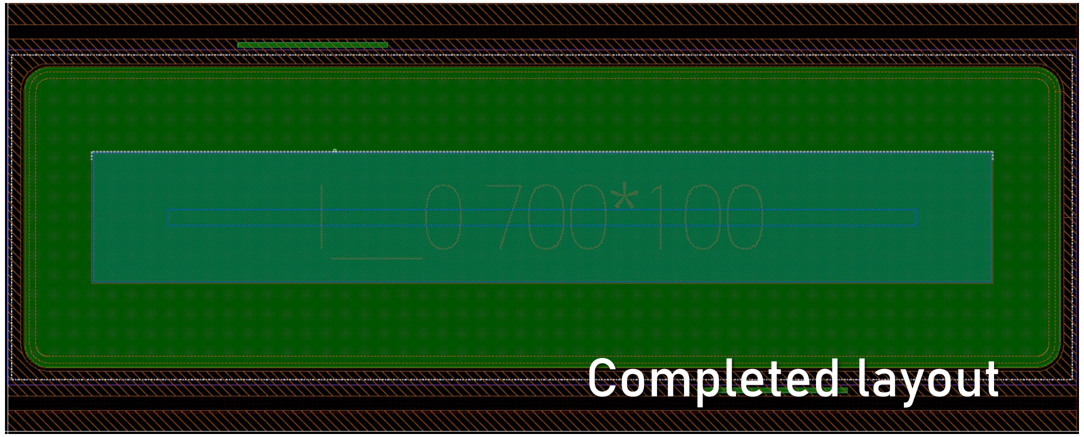


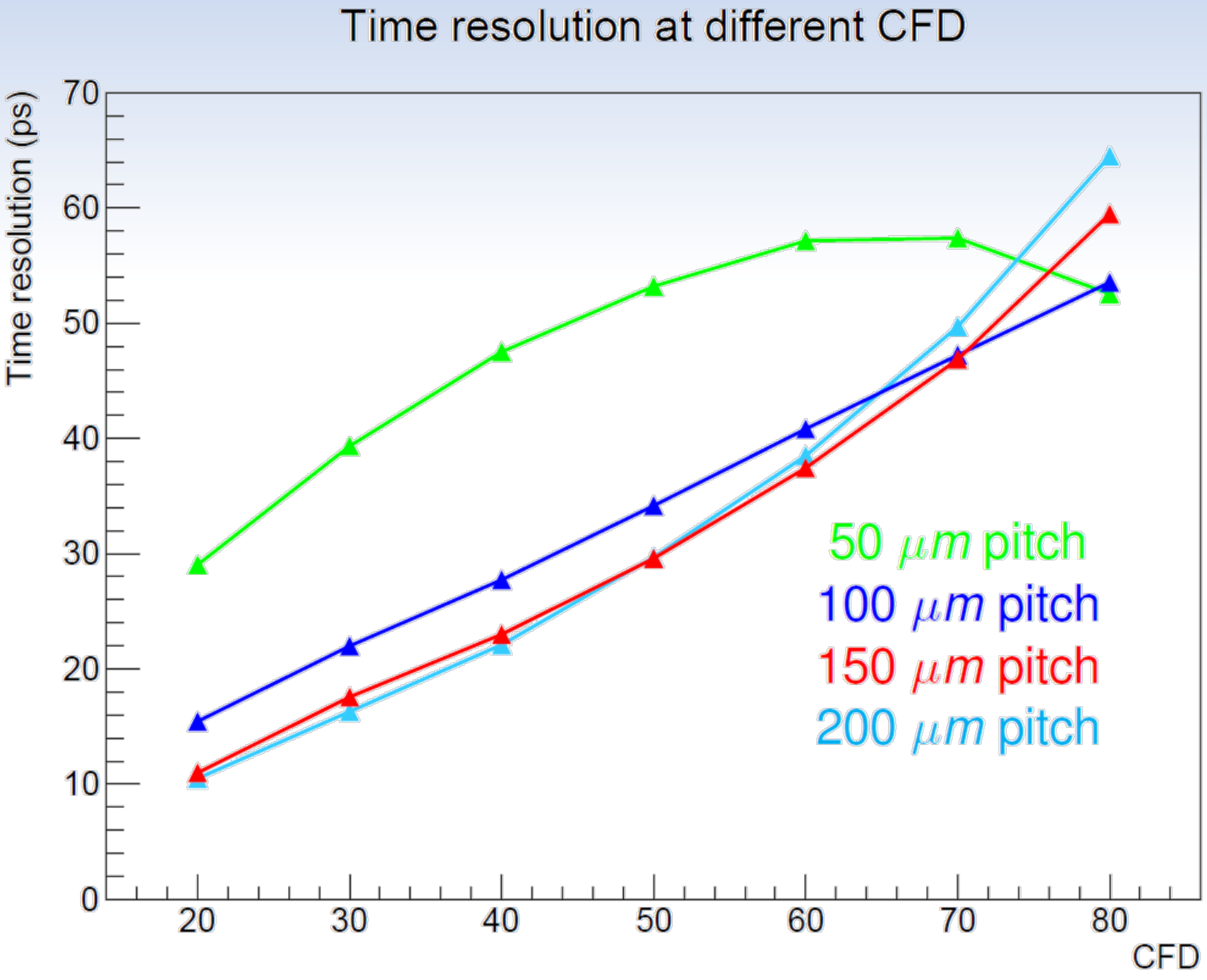
ARCADIA sensor for timing – optimal pixel size

Stefano Durando

Increasing the pixel pitch for better time resolution

- 150 µm and 200 µm pixel pitches show very close time resolution values
- Can achieve < 20 ps





50 µm thick sensor - G. Andrini, C. Ferrero

ARCADIA sensor for timing – process modification

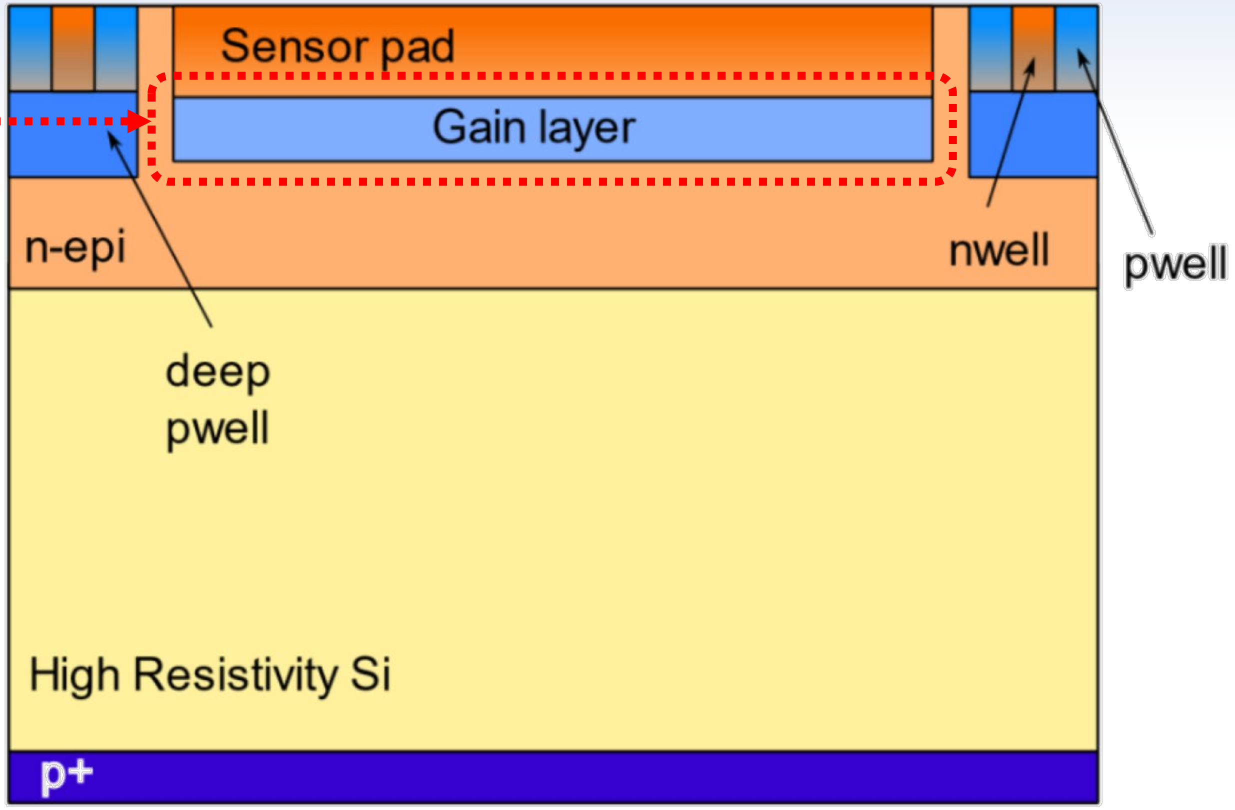
Stefano Durando

A gain layer can be added with minimal modifications to the process

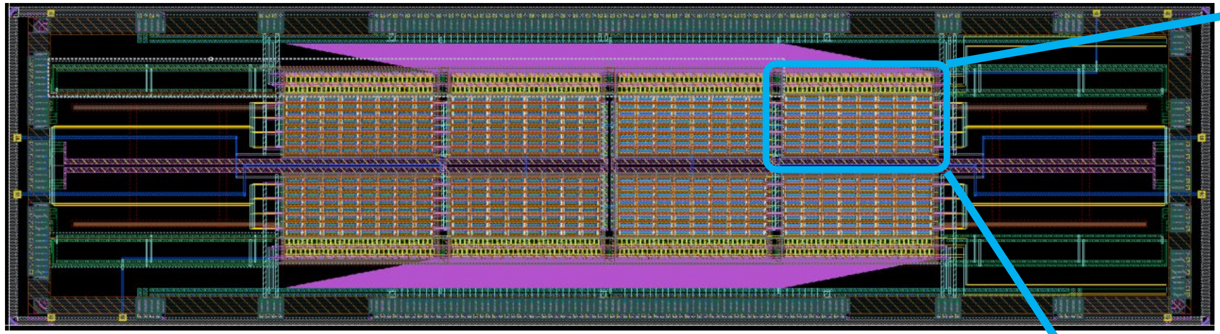
- With this approach, the sensor should be biased at **HV positive bias on the top side of the sensor to increase the gain**

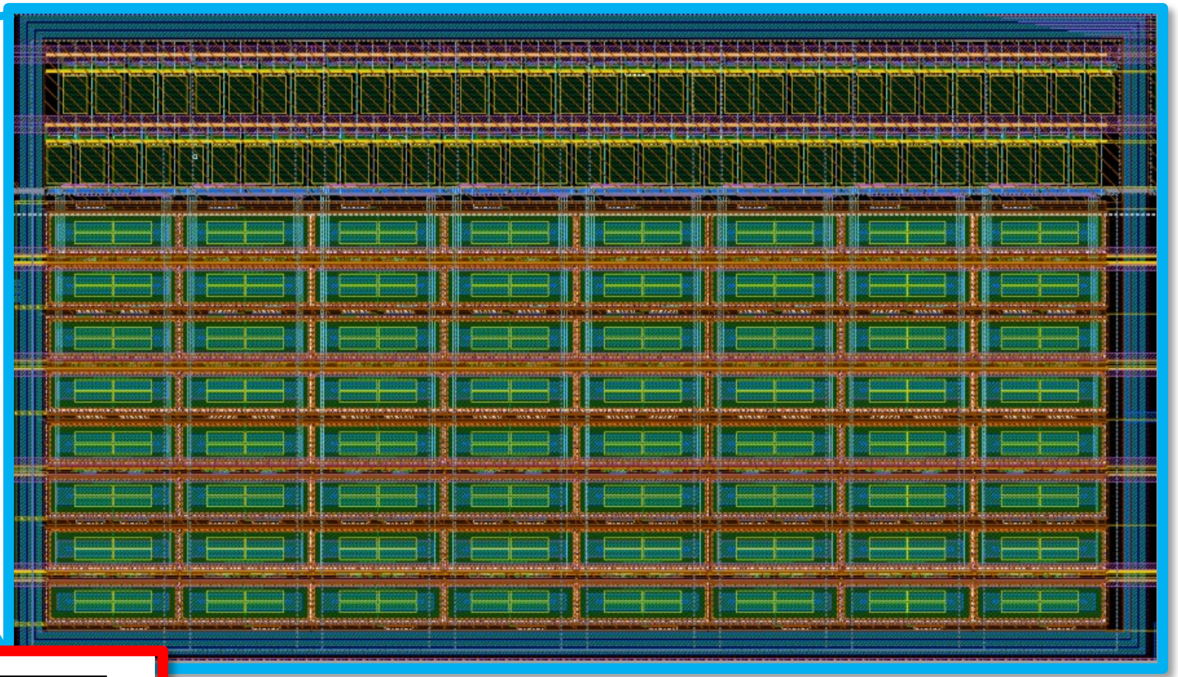
Drawbacks:
- Sensor biasing
- AC coupling with the electronics

Simulations :
- Estimation of the dose profile
- Prediction of the impact ionization



ARCADIA sensor for timing – process modification submitted





First demonstrator submitted in July 2022
- 16.4 x 4.4 mm2, 256 x 2 channels
- 110 nm technology node, 6 metal layers
- ARCADIA sensors + additional gain layer
- **Silicon just arrived**, waiting first measurements

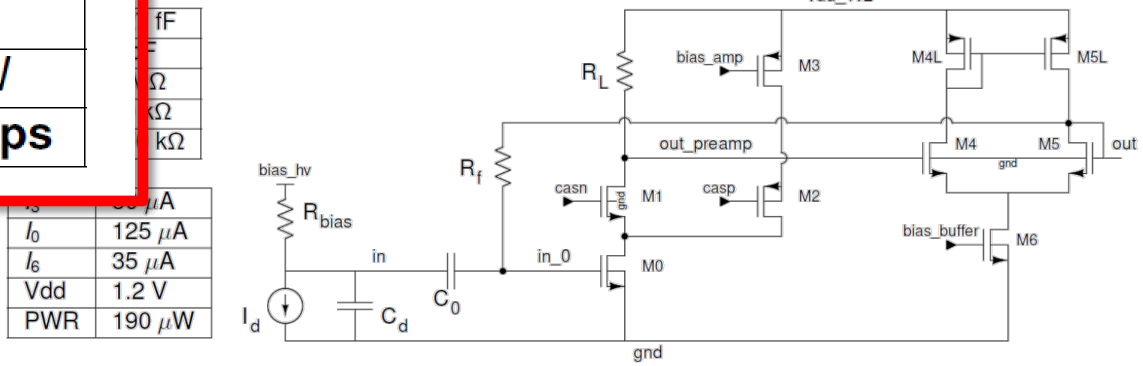
Post layout simulation →

Gain	35 mV/fC
BW	460 MHz
rms_{noise}	150 e-
PWR	190 uW
$jitter_{10-15-20}$	**10-7-6 ps**

- Pixel size = 250 x 100 μm²
- Diode area ≃ 220 x 70 μm²
- Sensor cap : Cd ≃ 127 fF
- Electronics area = 250 x 8 μm² on the pixel side
- 2 Pixel flavors (different guardrings)
- Minimum active thickness available is 50 μm

spired by LGADs front-end electronics [1]

300 mW cm^{-2}



[1] ALCOR, Agapopoulo et al 2020 JINST 15 P07007

Outlook

MAPS (or D-MAPS) work, but

commercial solution
single production step
cost-effective for large area

If taken together, a factor 100+ beyond state of the art

Few more extreme ideas and R&D necessary (scaling not enough)

Especially on power and data density:
- Analogue front end, digital architectures
- Data compression, and much more…

0.1% X_0 material budget

10^{16} NIEL, 500 Mrad TID

10 µm pitch

100 MHz cm^{-2} flux

≤ 100 ns time resolution

≤ 100 mW cm^{-2} power

10 ps timing at 300 mW cm^{-2}