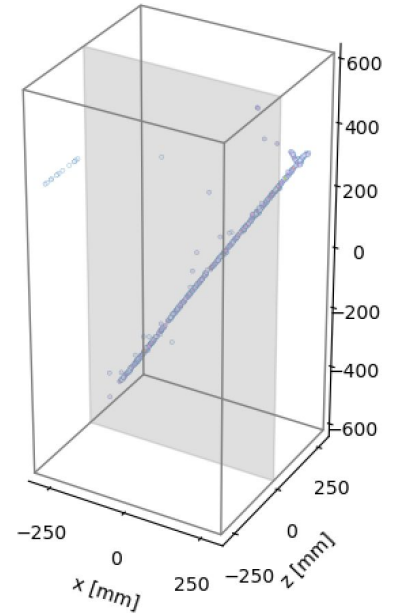
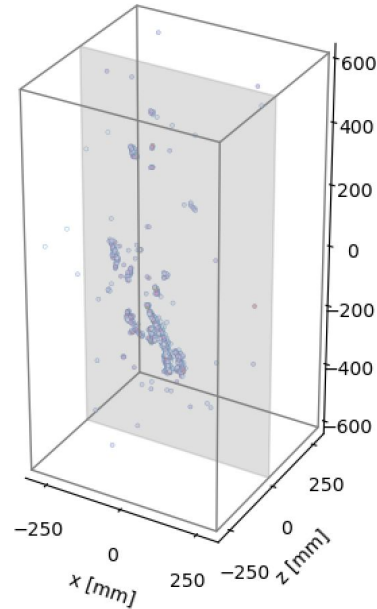
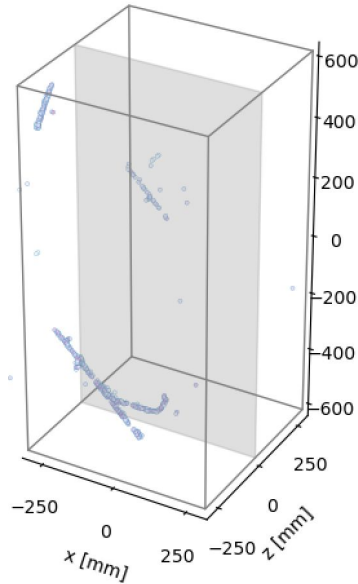
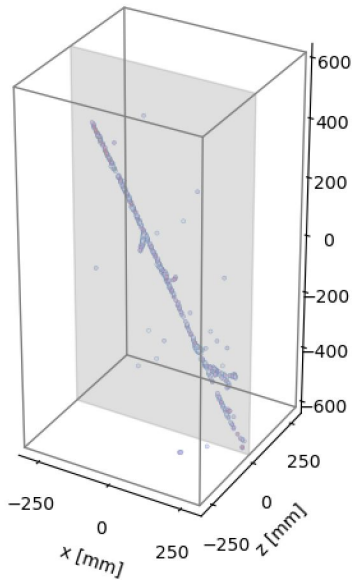


# **Module 3 Run 2 Operation Summary: Charge Readout**

Stephen Greenberg, March 2, 2023

# Overview

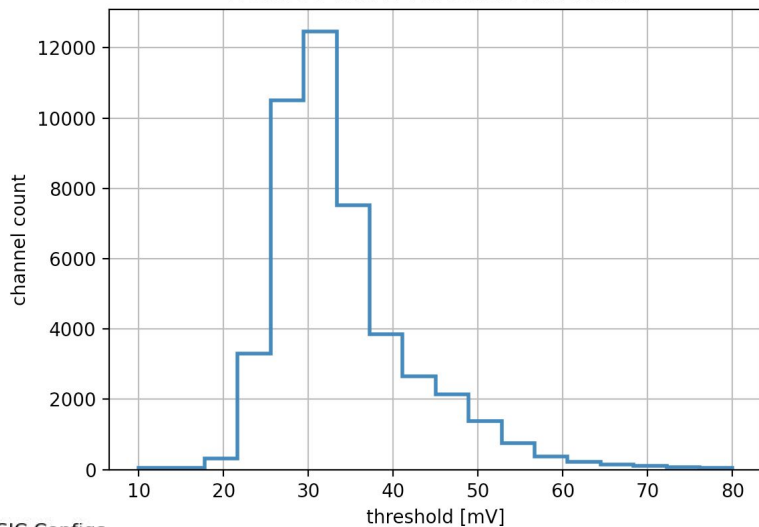
- All 1600 ASICs initially configured at cold
- Later failures to communicate with TPC 1 Tile 7 emerged (more later)
- 2.65% disabled channels, median threshold  $\sim 30$  mV



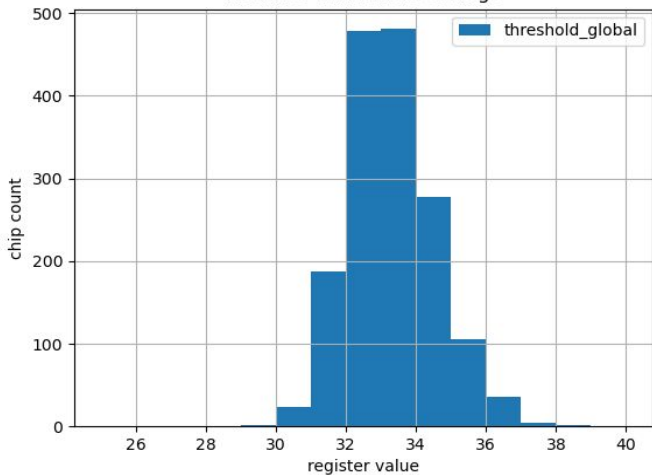
# Thresholds

- Uniform rate-based thresholding algorithm used
- Dedicated run with no periodic reset+no HV for threshold extraction
- Still room for optimization of thresholding
  - Additional range in pixel trim not used

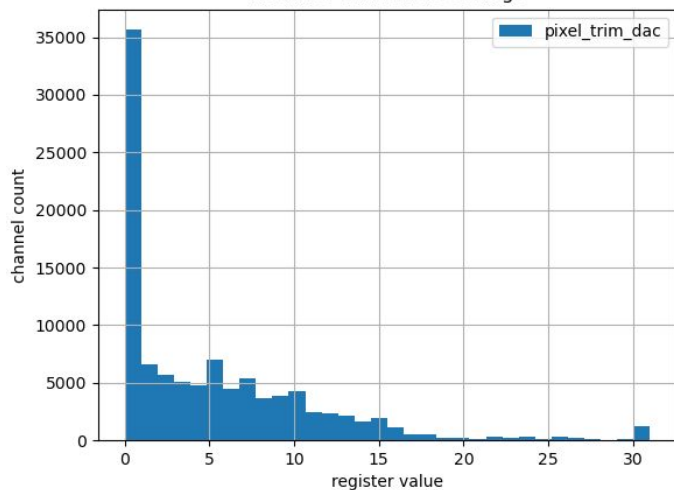
Module 3 Run 2 Threshold Extraction



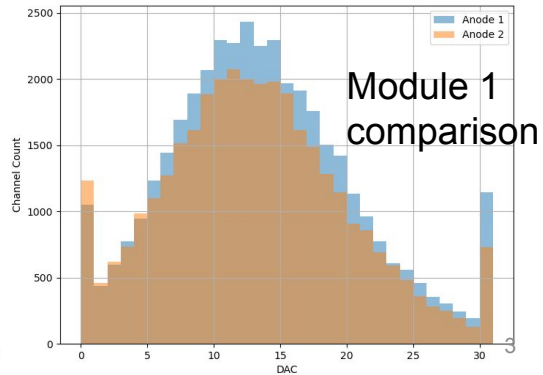
Module3 Run 2 ASIC Configs



Module3 Run 2 ASIC Configs

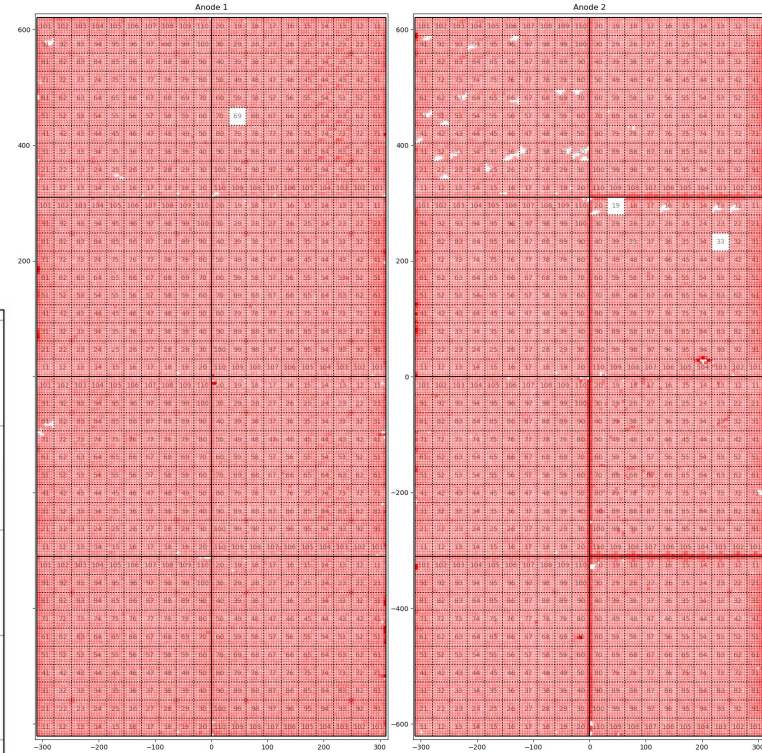
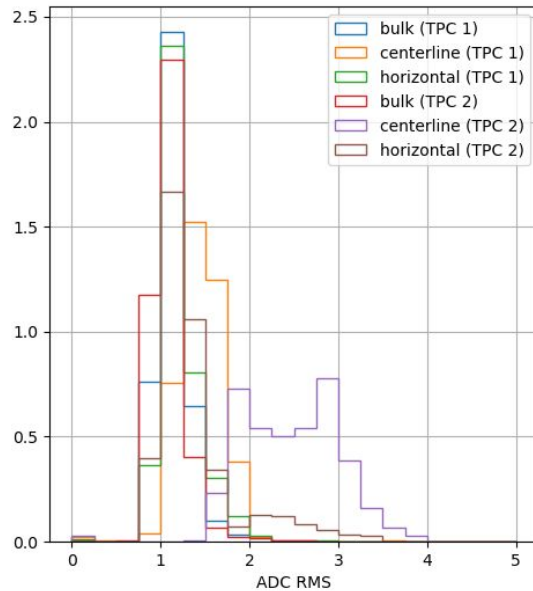
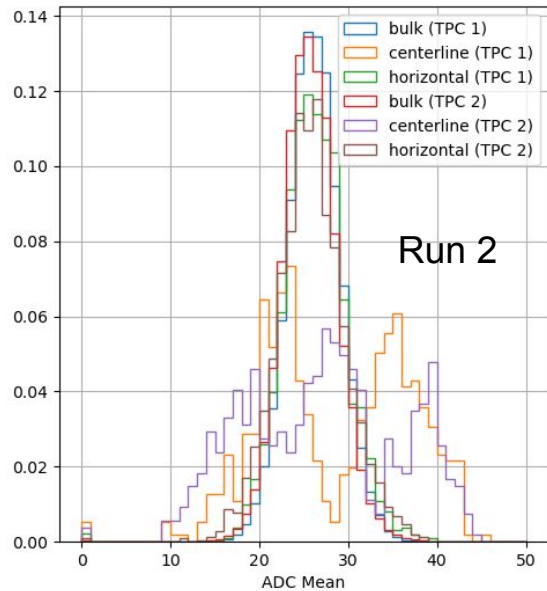


pixel\_trim\_dac



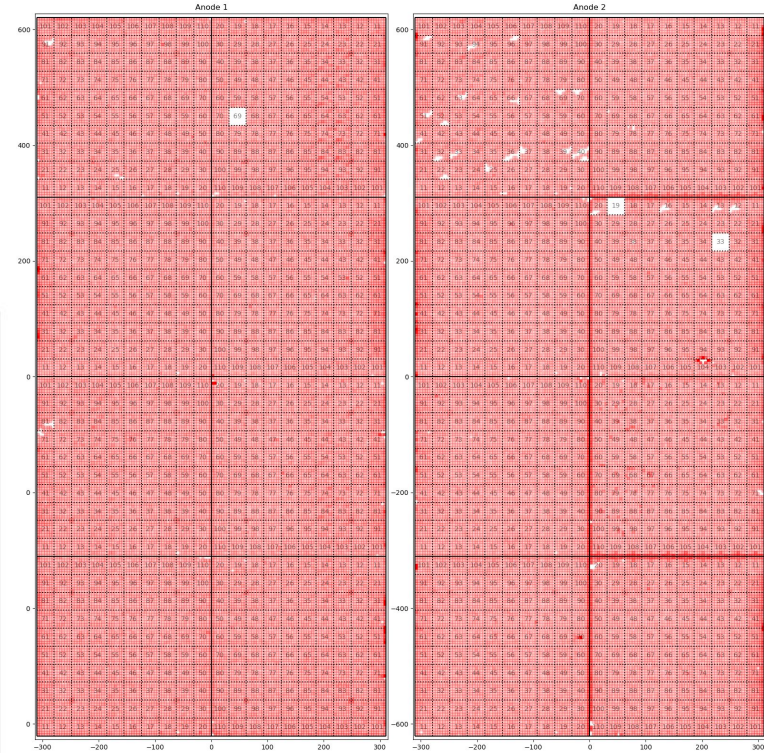
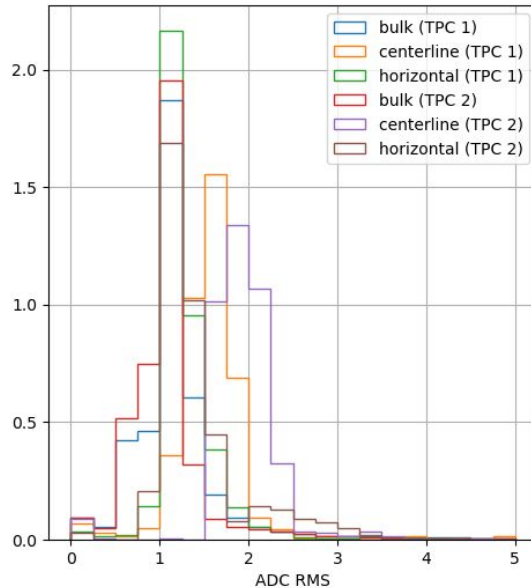
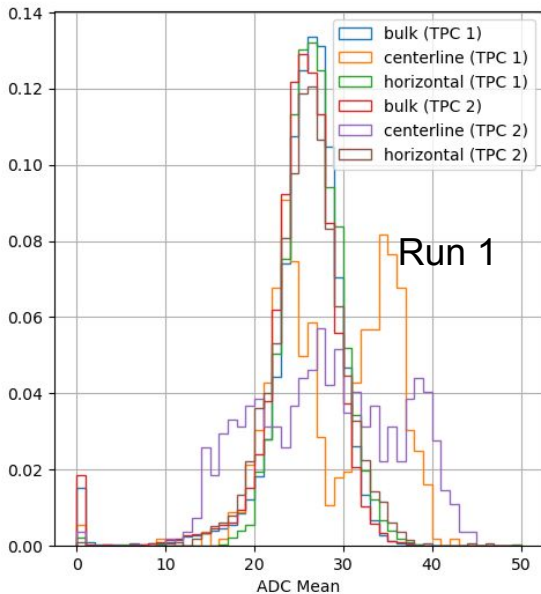
# Tile Edge Effects

- DC Pedestal shift for centerline pixels on both TPCs
- Increased pedestal RMS on some TPC2 tile boundaries
- Observed warm/cold in both run 1 and run 2.
- Same grounding scheme for TPC1 and TPC2



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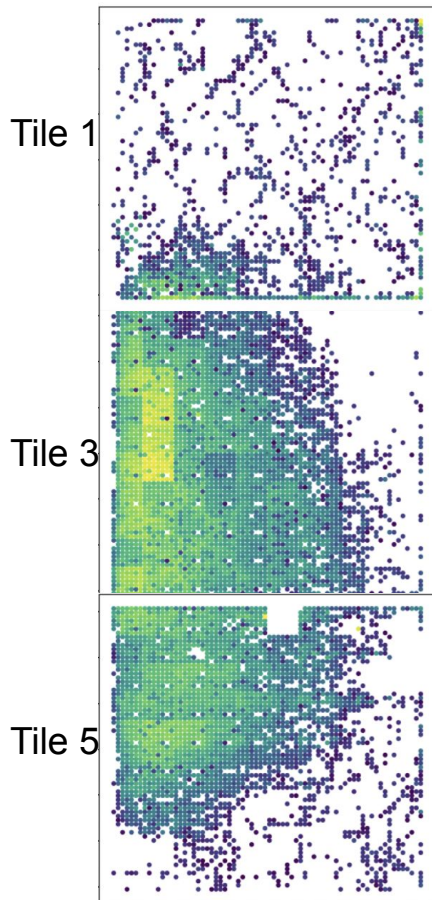


# Tile 7 Configuration Issues

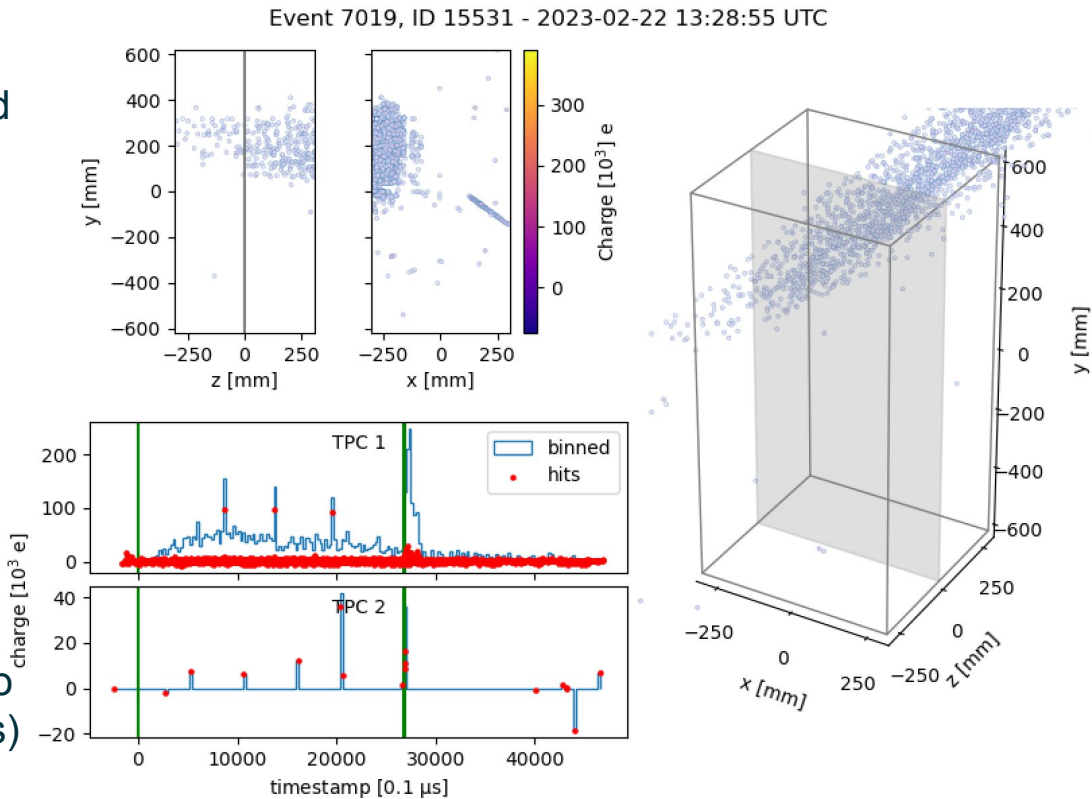
'DATA'	26	4276355	'0xa3a01fc03cfd3feL'
'DATA'	26	4276627	'0xa3a01fc03cfd3feL'
'DATA'	26	4276899	'0xa3a01fc03cfd3feL'
'DATA'	26	4277171	'0xa3a01fc03cfd3feL'
'DATA'	26	4277443	'0xa3a01fc03cfd3feL'
'DATA'	26	4277715	'0xa3a01fc03cfd3feL'
'DATA'	26	4277987	'0xa3a01fc03cfd3feL'
'DATA'	26	4278259	'0xa3a01fc03cfd3feL'

- Inability to communicate with tile 7 on TPC 1 at cold starting around 11 PM PT Tuesday (2/21)
- Floods of identical packets observed on all IO channels
  - Packet content: broadcast write to enable MISO upstream
  - Source of packets unknown
  - Persists through hard resets and power cycles
  - Tile depowered overnight—issues continued at next attempt 2/22 morning
  - Communication with tile restored during warmup (after draining)
- Tile failure due to broadcast write reproducible in lab
  - Single packet causes packet flood on all io channels
  - Persists through power cycles (at least 10-20 minutes depowered)
  - Can regain communication by writing broadcast disable upstream packets and hard reset(s)
- Possibly related to reproducible bit flips from certain ASICs?

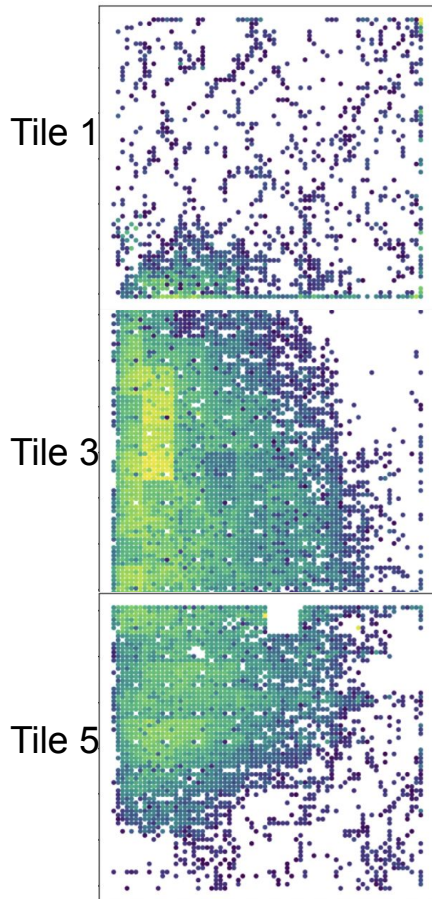
# Additional Noise Features



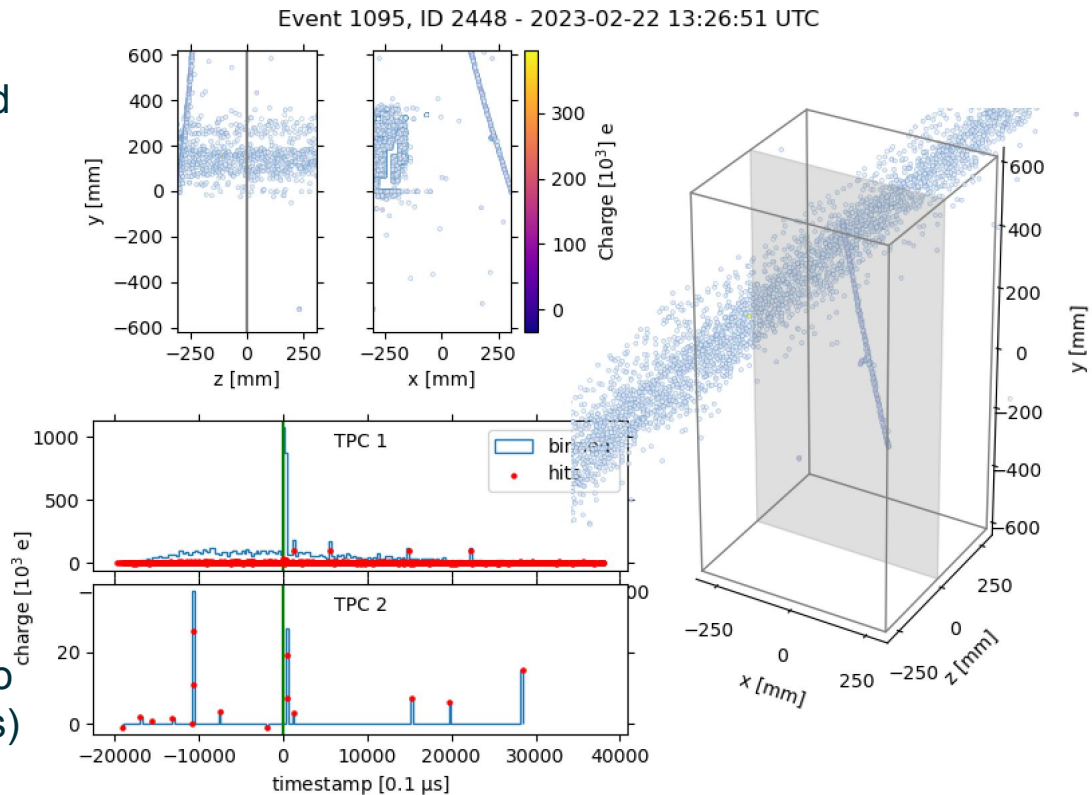
- Started with HV ramp up, stopped after ramp-down
- Visible only on TPC 1
- Spatially correlated with sparking on field cage panel and impacted ARCLight
- Not visible in run 1 (possibly due to higher thresholds)



# Additional Noise Features

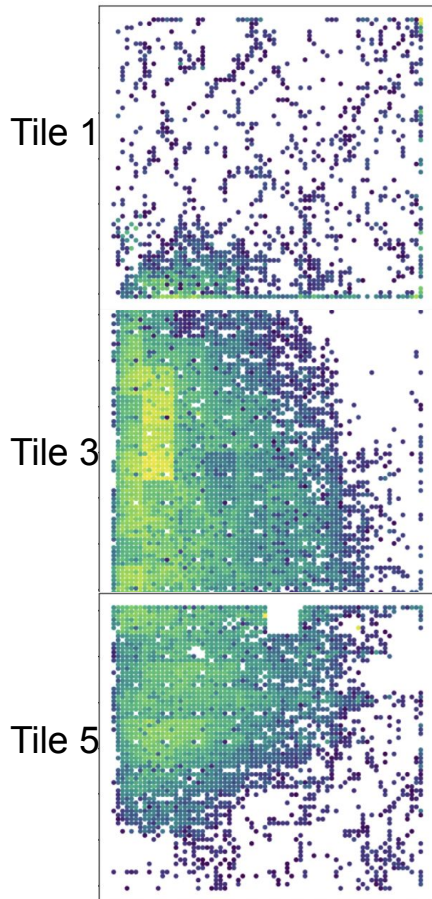


- Started with HV ramp up, stopped after ramp-down
- Visible only on TPC 1
- Spatially correlated with sparking on field cage panel and impacted ARCLight
- Not visible in run 1 (possibly due to higher thresholds)

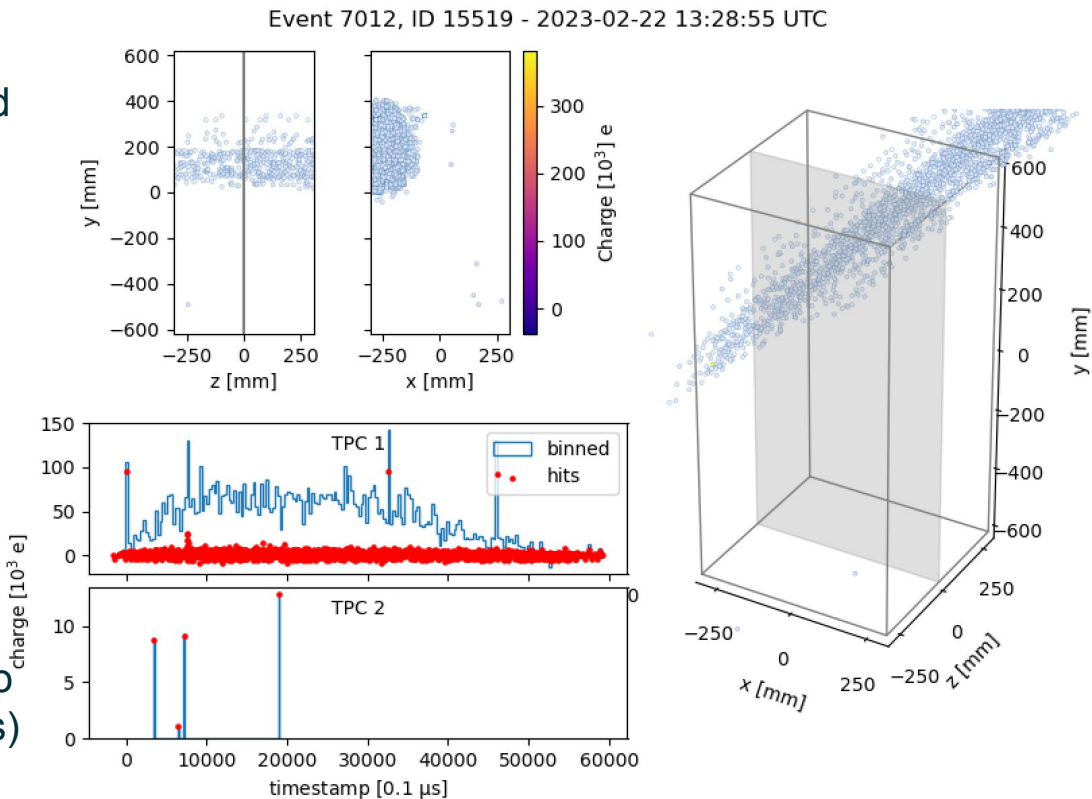




# Additional Noise Features

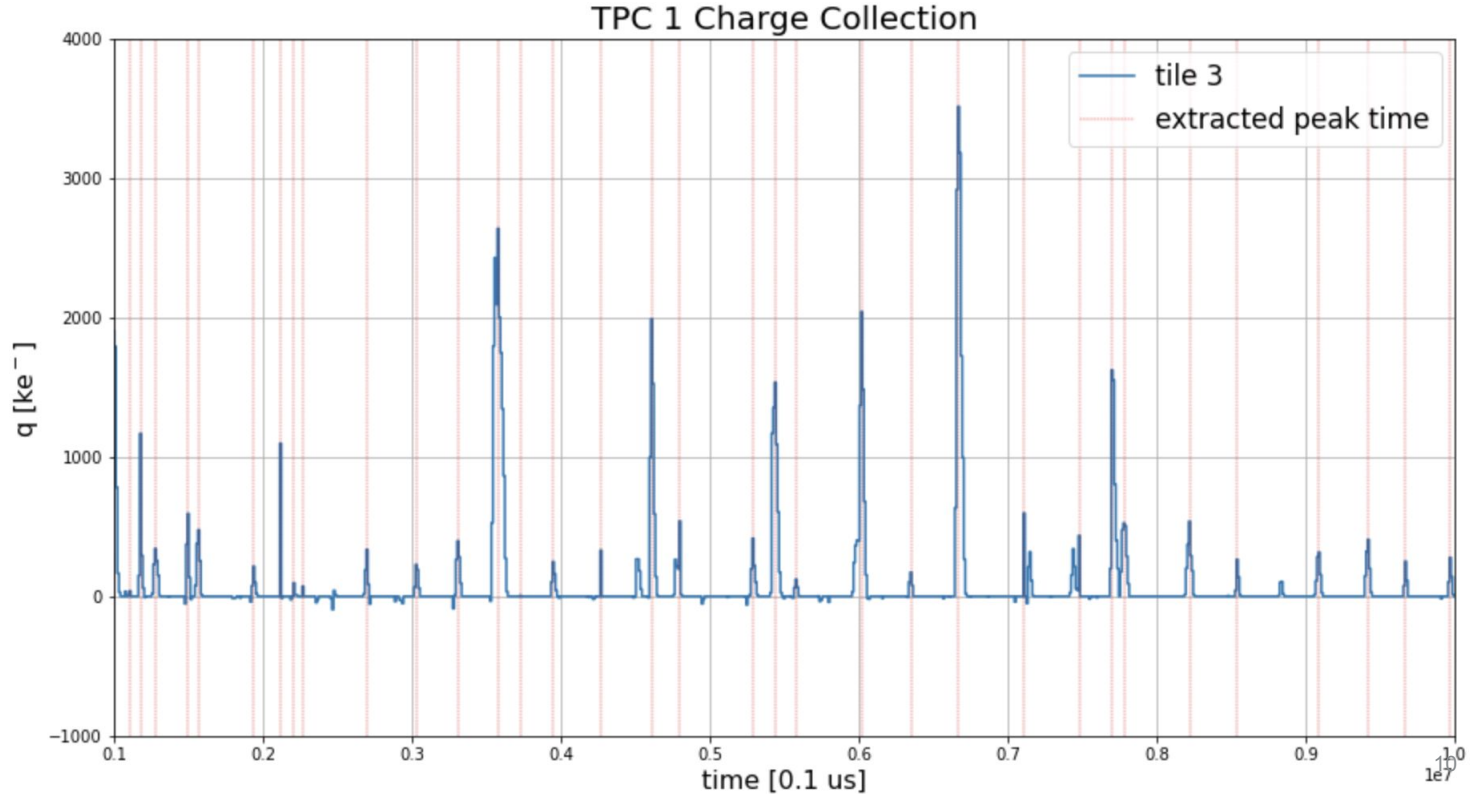


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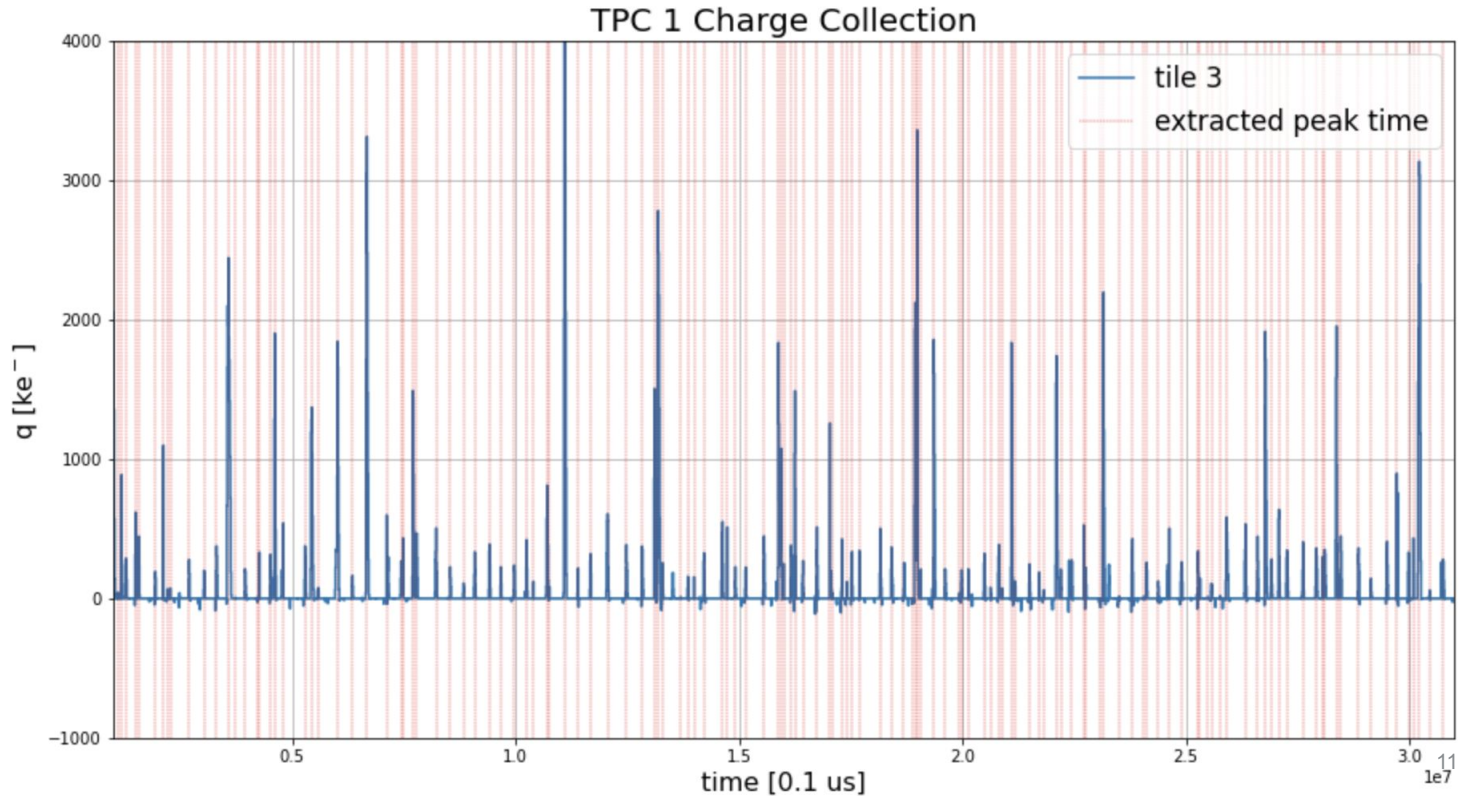
# Additional Noise Features

- Typical duration 3-8 ms
- (right) Charge collected vs. time on single tile



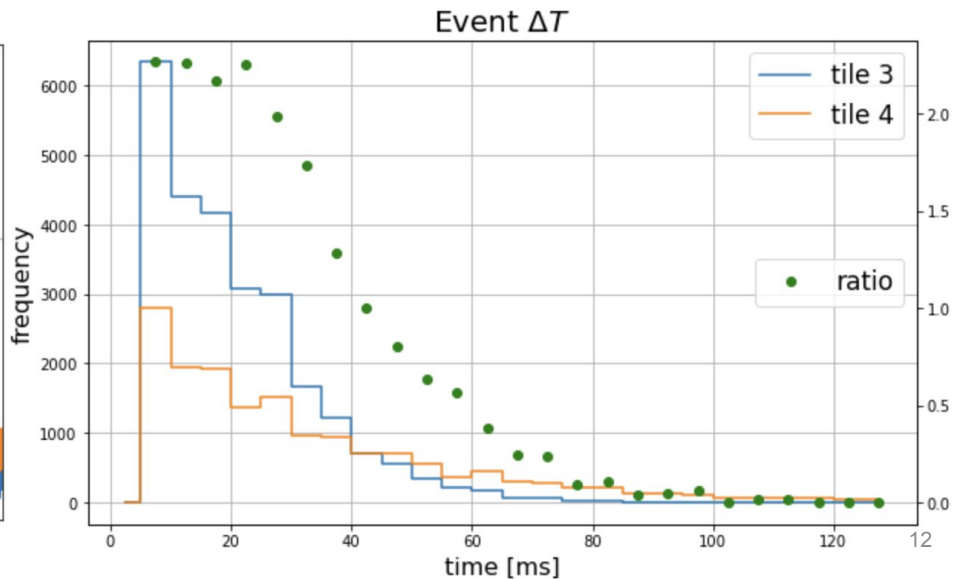
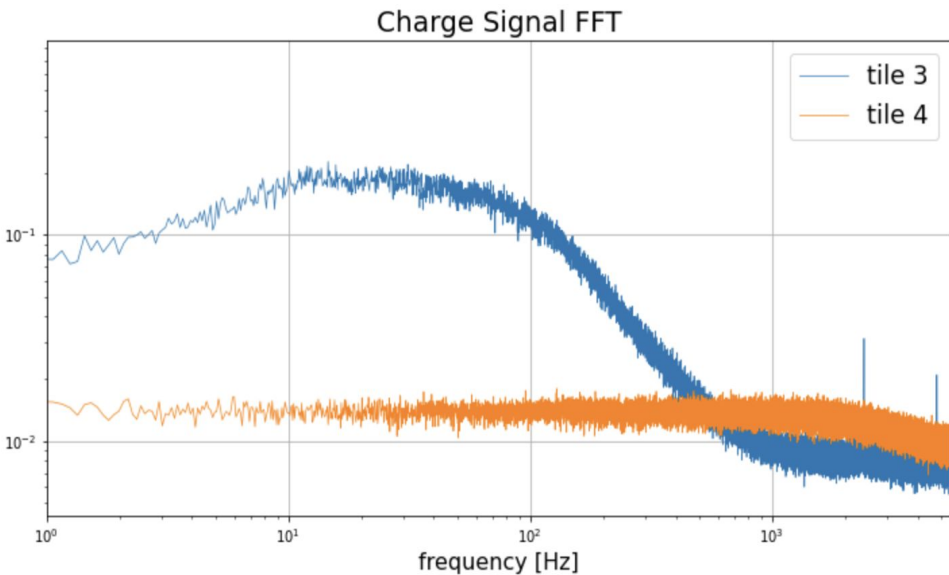
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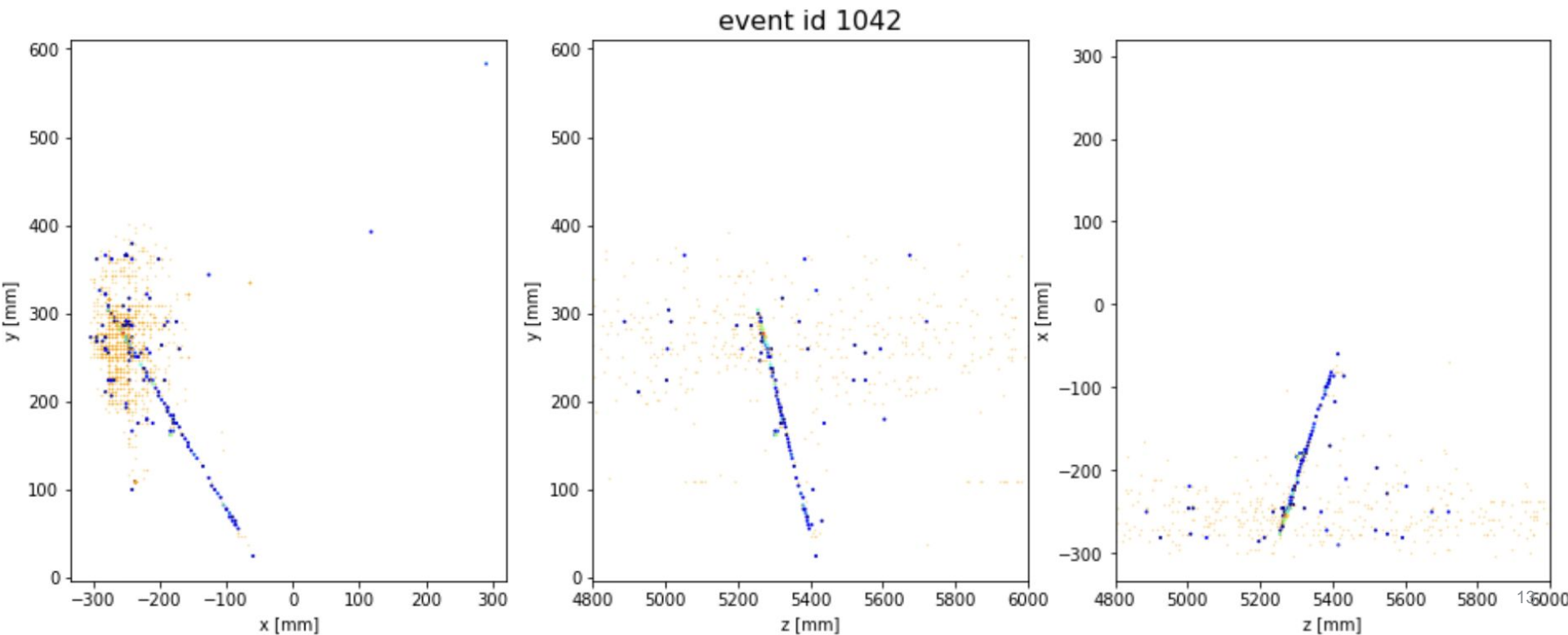
# Additional Noise Features

- (right) Time between extracted peaks,  $\sim 10\text{-}30$  ms
- (left) full charge collected vs. time signal FFT



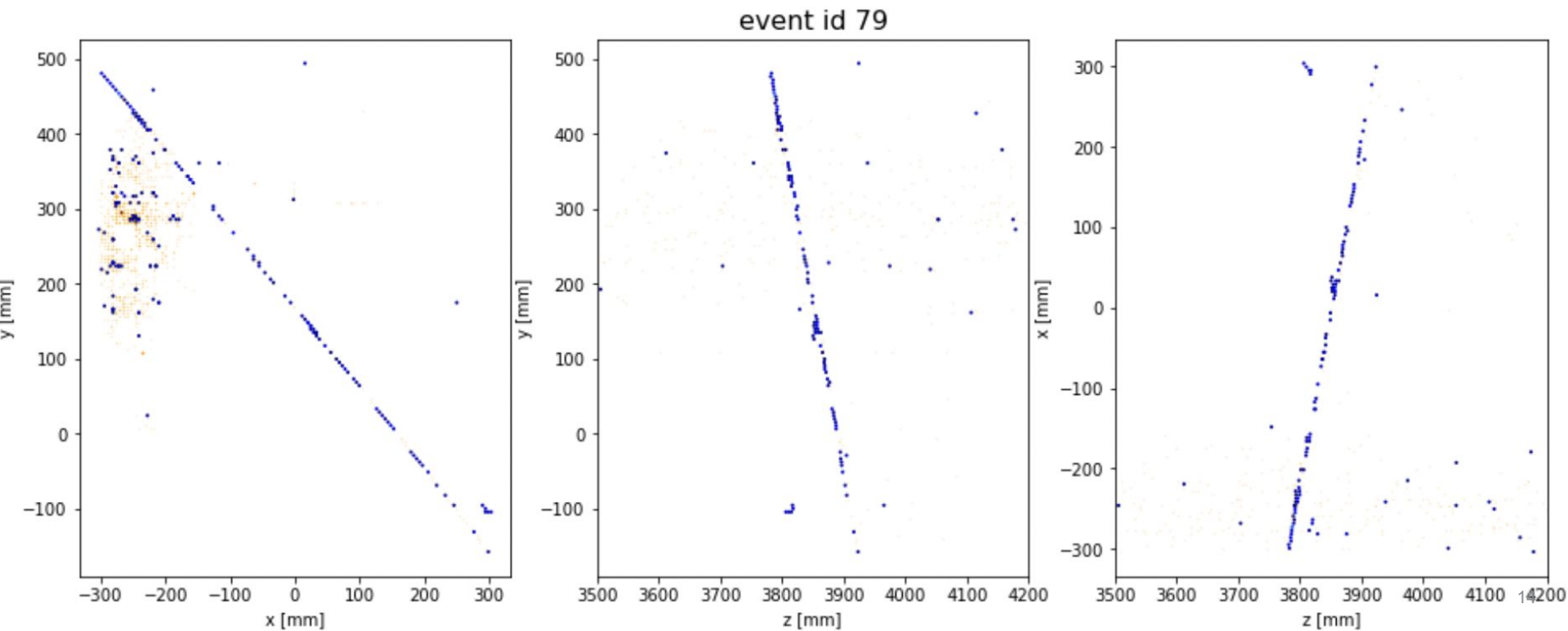
# Additional Noise Features

- Sample events with track passing through noise



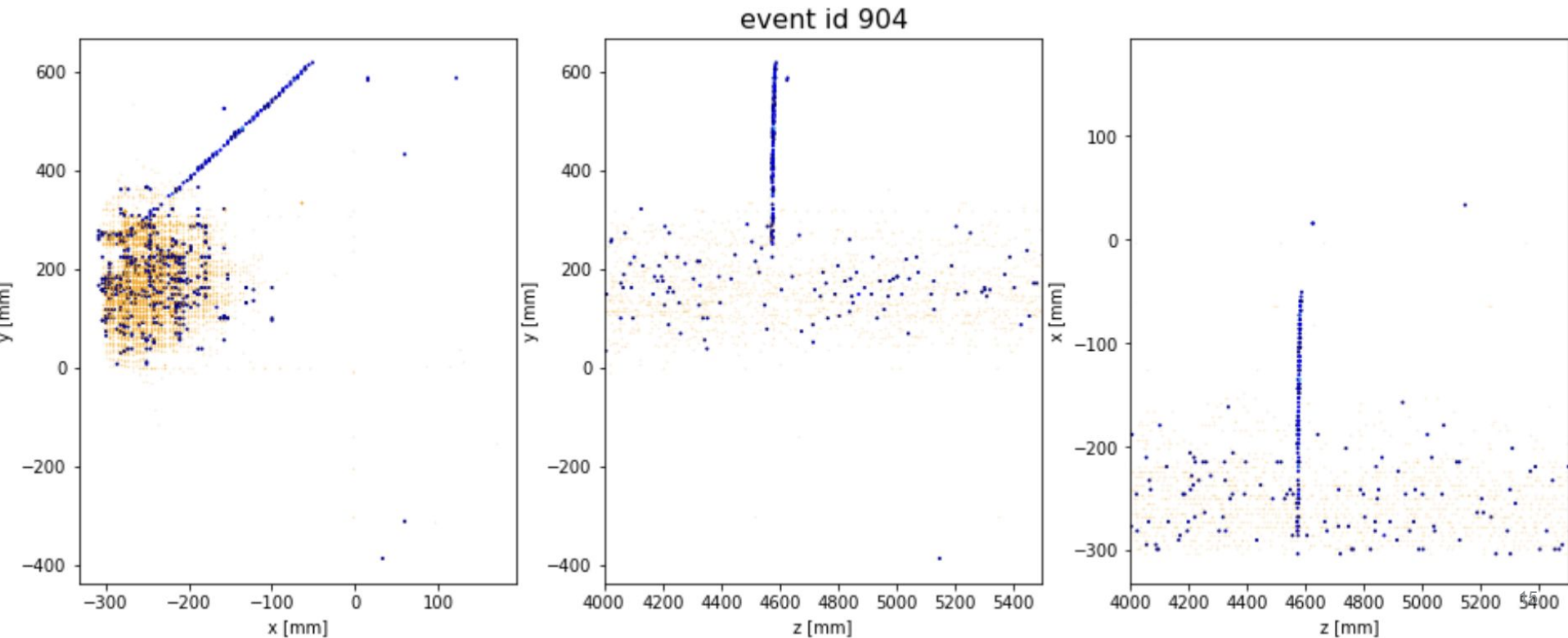
# Additional Noise Features

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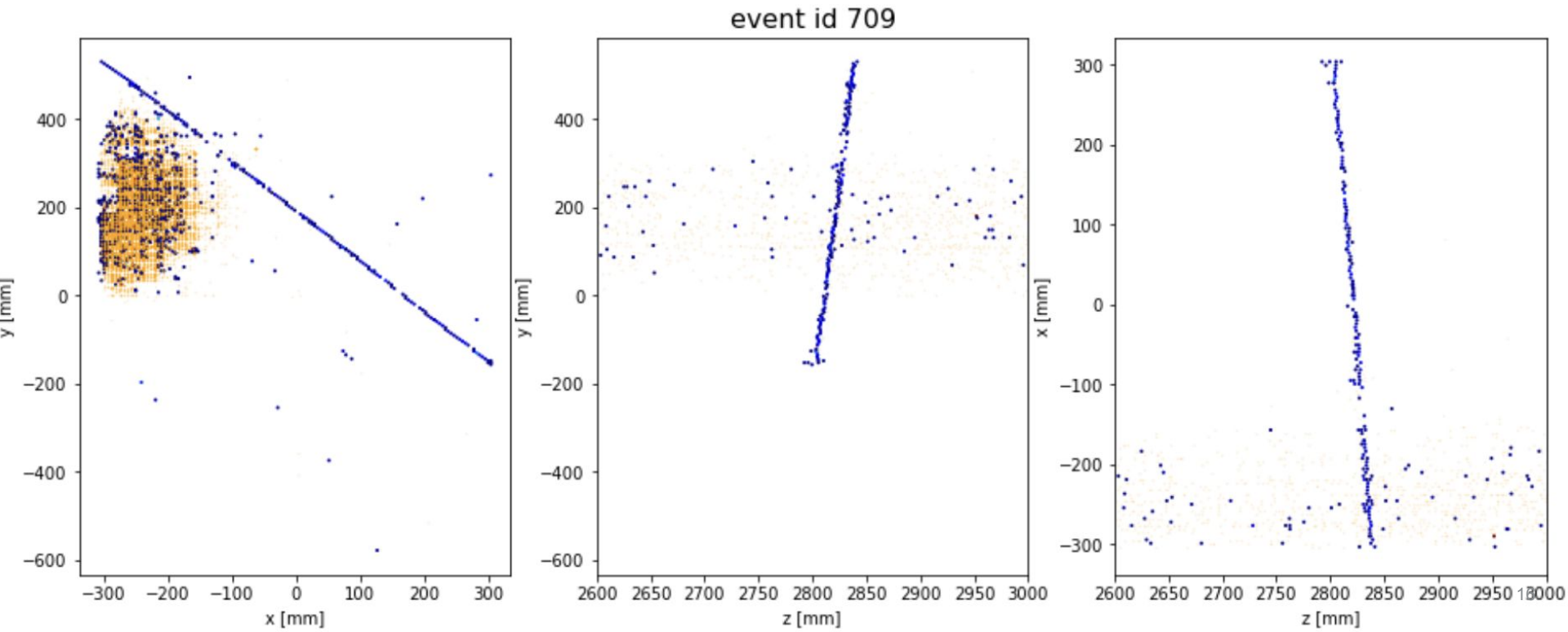
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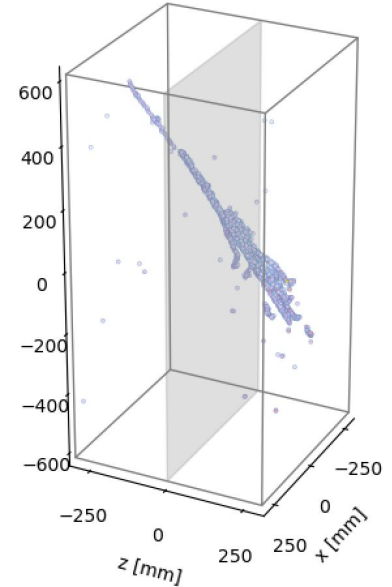
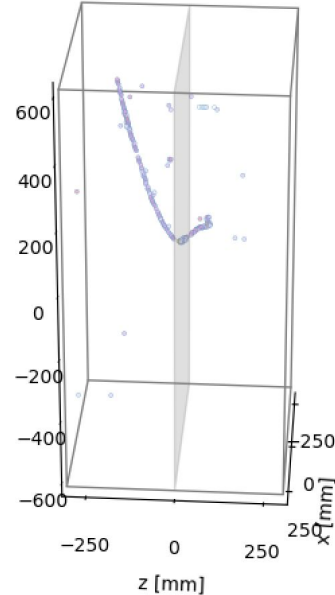
- Sample events with track passing through noise





# Next Steps

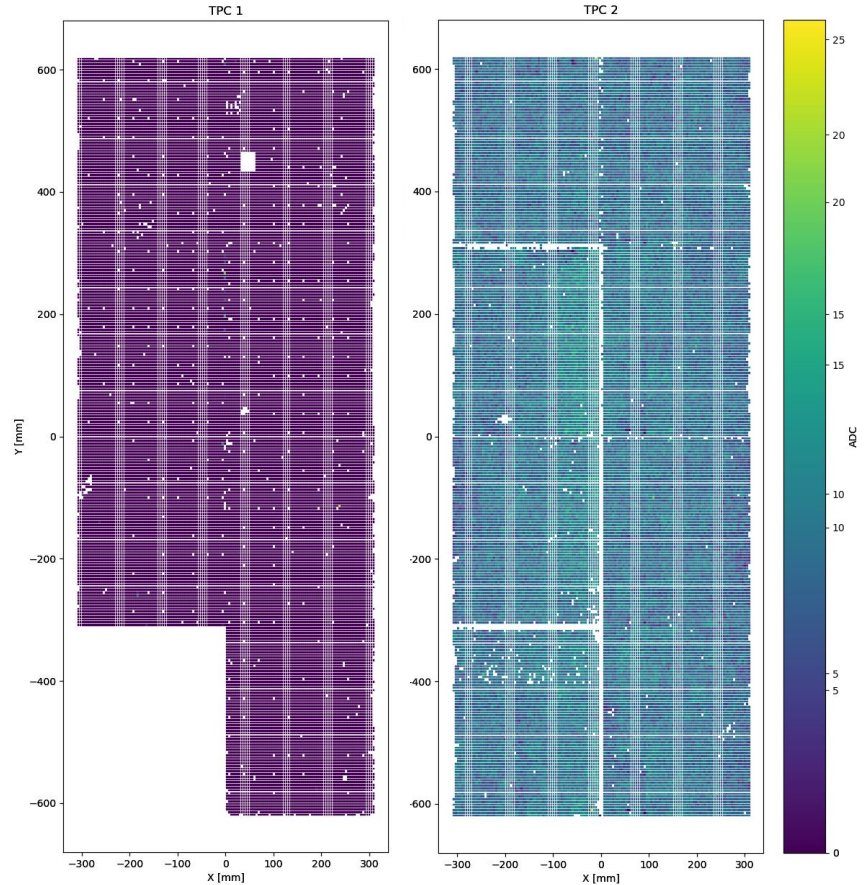
- Suitable charge thresholds obtained, although further optimization is possible
- Overall charge system is healthy, pending further investigation of Tile 7 failure
  - Pedestal shift edge effects also warrant investigation
- **Several high priority items still on the table for evaluating module**
  - Correlation of light and charge data around noise from sparking
  - Searching for culprit(s) of Tile 7 failure
    - Minor holdup: access to DAQ machine at Bern



# Backup

# Disabled Channels

- 2.56% disabled total
  - Includes channels disabled on tile 7 prior to failure
- Edge effects result is significant disabling



# Purity

- Relatively poor purity seen in TPC1
  - Run started quickly after filling
- Plot from end of run around 02/22 17:00 CET

