Precision Timing System
MiniWorkshop

HEP LLRF

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Juan Fernández
juan.fernandez@nav-timing.safrangroup.com

Pilar Gil
pilar.gil@nav-timing.safrangroup.com

SAFRAN

High Energy Physics (HEP) department

Team areas of expertise:

- Ultra-stable low-noise RF electronics
- Customized or standard crates (Compact PCI-e Serial, uTCA or standalone solutions).
- Real-time embedded system based on the latest FPGAs and SoCs.
- Individualized Control system Solutions based on EPICS frameworks (EPICS, TANGO).
- RF distribution.
- High reliable and real-time diagnosis and post-mortem analysis.
- Fast data acquisition systems. Adaptive Fast-control systems.

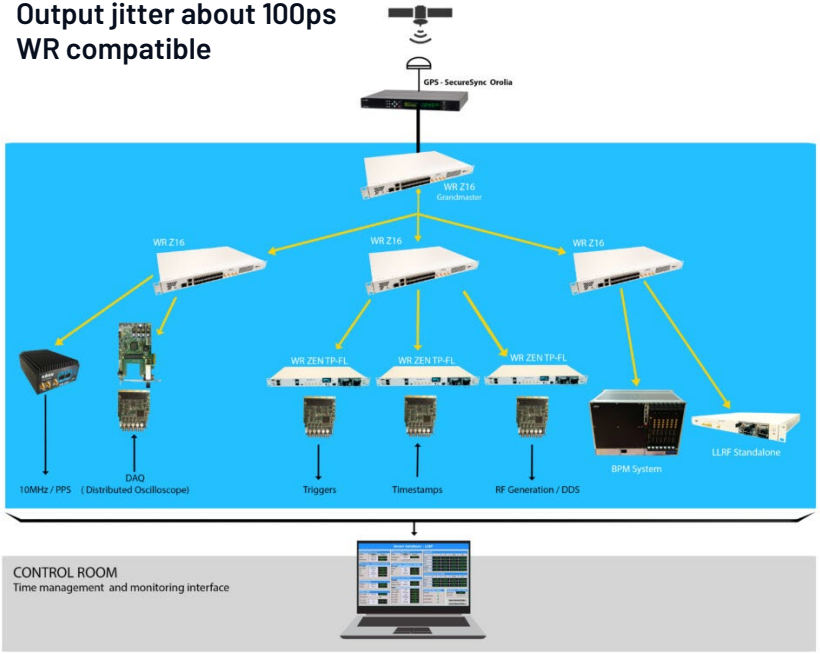
Radiofrequency control, monitoring, timing system and services

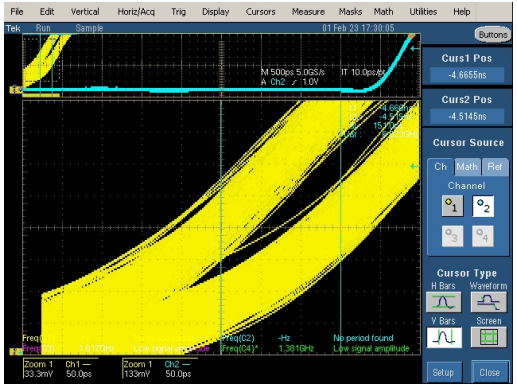
Products:

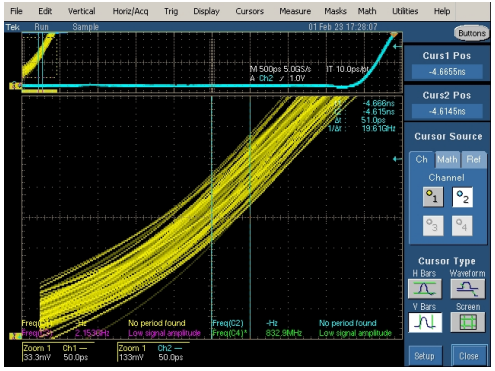
- LLRF – Precise Low Level RF generators
- BPMs – Beam Position Monitors
- Timing systems – Precise triggers generation
- RF generation and distribution
- Software & Services

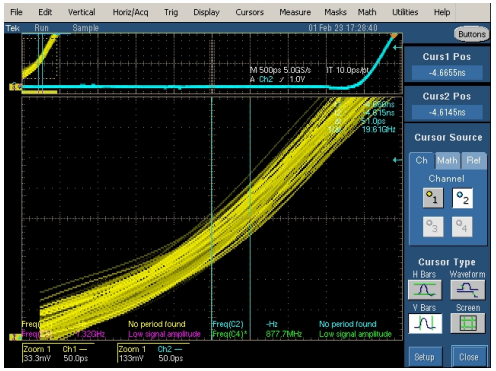
Timing System

Generation of synchronized triggers and gate signals
Configurable rates, widths and periods
Resolution below 10ps
Output jitter about 100ps
WR compatible









Goal:
15ps output jitter
5ps resolution

Safran´s LLRF capabilities

Chassis and backplanes:
CPCI, UTCA, standalone

Frequency range:
up to 1.5 GHz

Master Reference:
External (MO) & White Rabbit (10MHz)

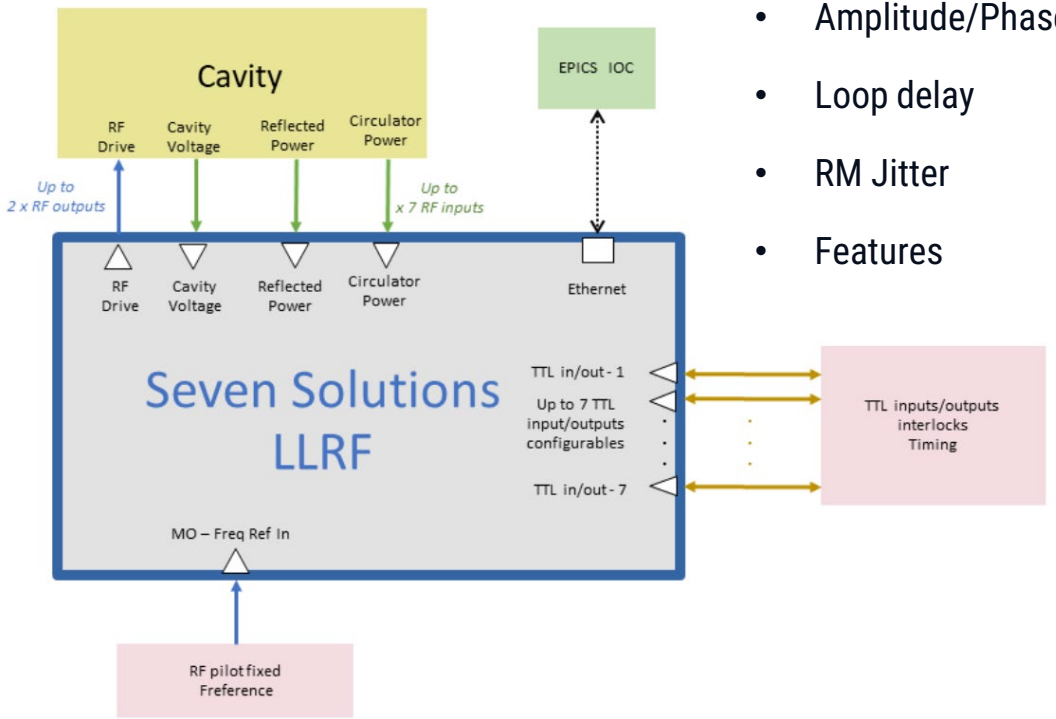
FPGA families:
From Virtex 6 to Zynq Ultrascale (MPSoc)

CPU:
External CPU & System on Chip (SoC)

Data acquisition architecture:
Direct sampling & intermediate frequency

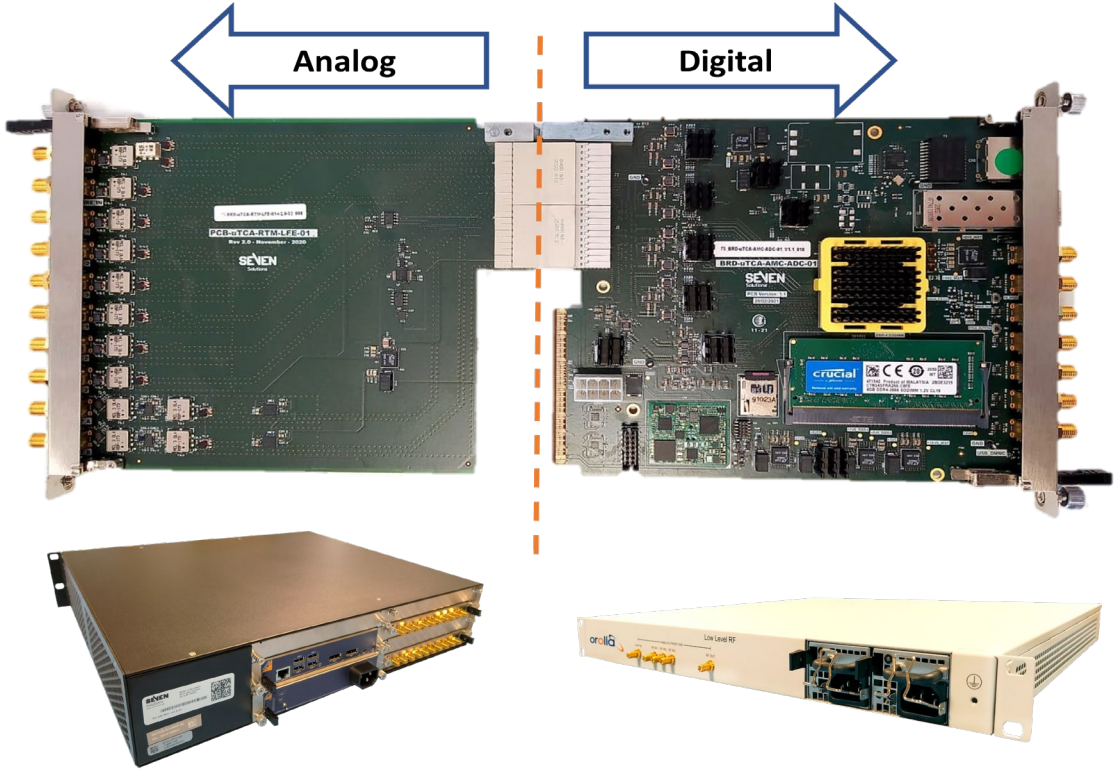
Control system:
EPICS & TANGO

Standard uTCA LLRF solution



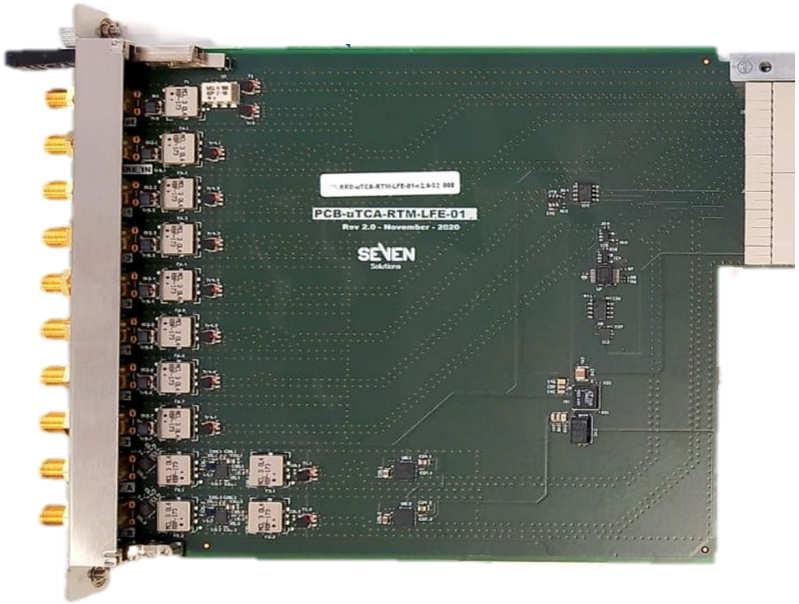
- Amplitude/Phase Stability **0.3% - 0.3 degree**
- Amplitude/Phase precision **0.03% - 0.03 degree**
- Loop delay **< 1us**
- RM Jitter **182fs**
- Features **Continuous and Pulse mode**
  Feedforward
  Frequency shifting
  Frequency tracking (digital PLL)
  Fast output interlock system (Machine protection)

Standard uTCA LLRF solution



- NATIVE-R2 uTCA.4 from N.A.T. **(up to 5 LLRF boards - AMC + RTM)**
- NAT-MCH-**PHYS80**
- NAT-MCH-**RTMCOMex-E3**
- Timing gating and triggers:
  - 4 x **shared bidirectional backplane lines**
  - 4 x **point-to-point backplane lines**

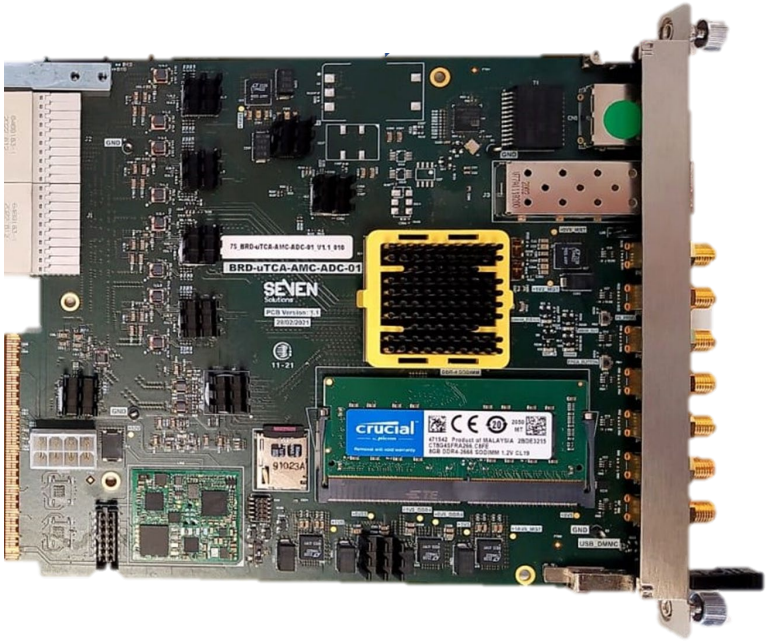
Standard uTCA LLRF solution



LLRF Front-End (LFE) board

- RTM with double height and mid-size form factor **uTCA.4**
- **1 x RF MO Ref.**: 176 MHz sine wave for LLRF reference
- **7 x RF inputs** to monitor up to two cavities
- **2 x RF outputs** to drive up to two cavities
- **Direct sampling** architecture
- RF input power dynamic range: **[-60,+10] dBm**
- Maximum RF output power: **+10dBm**
- **Fail-safe for overheating** mode
- EEPROM memory

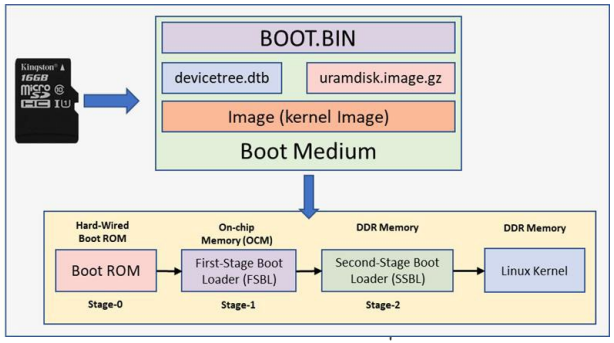
Standard uTCA LLRF solution



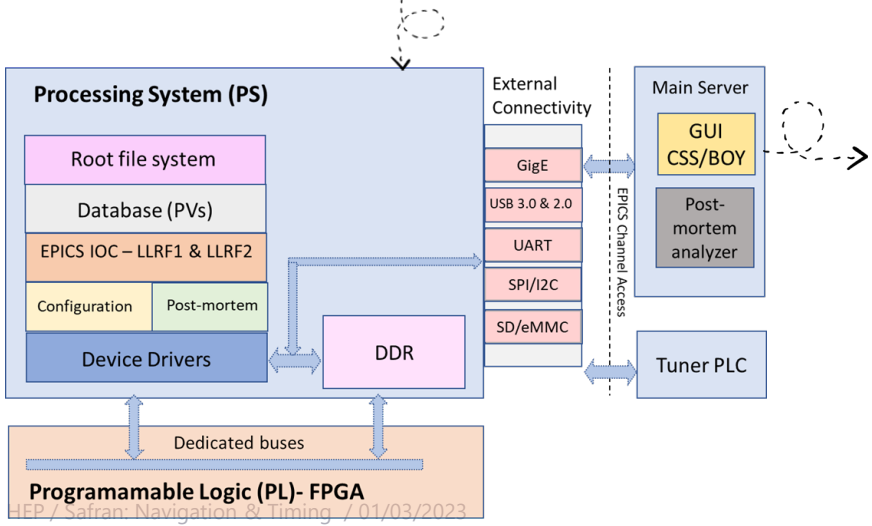
LLRF AMC board

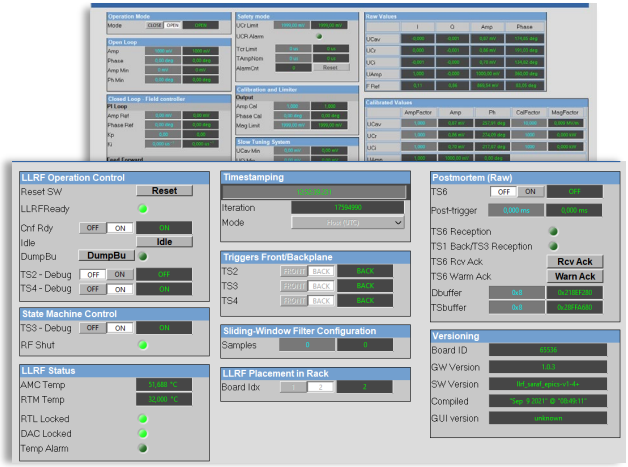
- **8 x ADC** channels
- **2 x DAC** channels
- **16 bits, 250MSPS ADCs - QDR LVDS** interface
- **16 bits, 1.5 GSPS DACs – DDR LVDS** interface
- **Zynq UltraScale+ FPGA** from Xilinx
- **PLL** for low phase noise distribution clocks
- **8GB DDR4** for processor and data storage (postmortem analysis)
- ETH & SFP port (**White Rabbit compatible**)
- uTCA MMC controller
- **Fail-safe for overheating** mode
- uSD socket, uUSB port

Software/Gateware integration



- Buildroot for OS Image:
  - BOOT.bin: FPGA image
  - Uboot: instructions to boot the devices
  - Devicetree: mapping of devices of the system
  - Image: Linux kernel image





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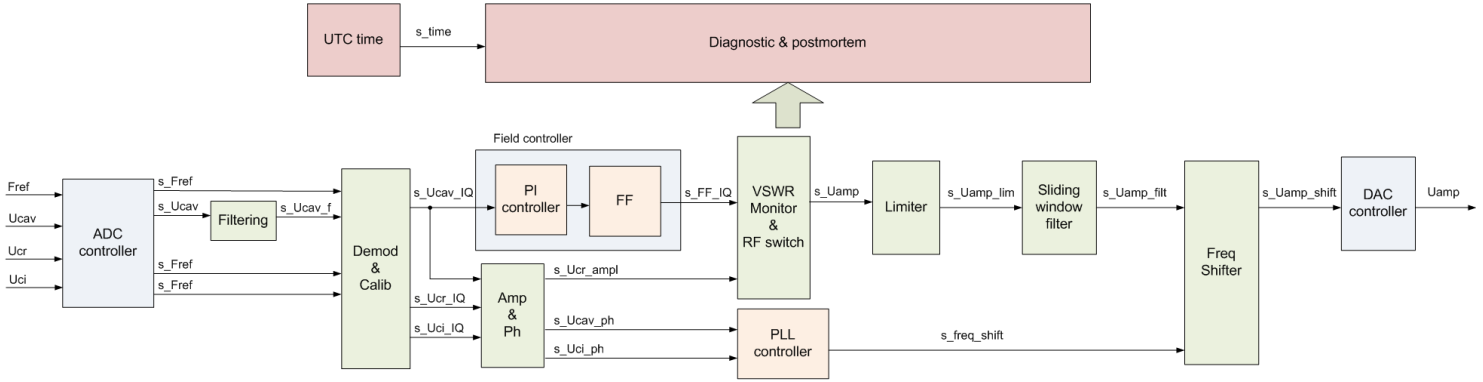
LLRF gateware architecture

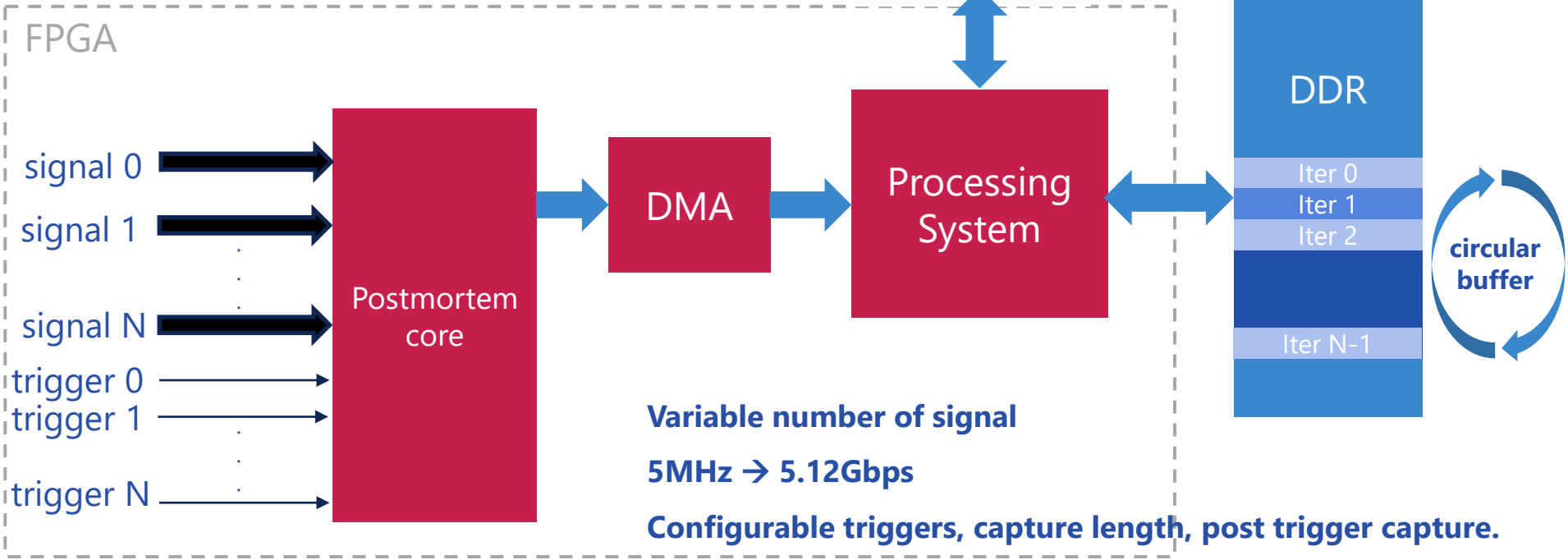


- **Direct sampling** architecture
- **Amplitude and phase loop controller** in pulsed and continuous wave
- **Feedforward** for beam loading compensation
- **VSWR** (arcing/reflection) detection and handling events
- **Pulse shaping** feature for smoothing RF pulses
- Provides information for **step tuner motors**

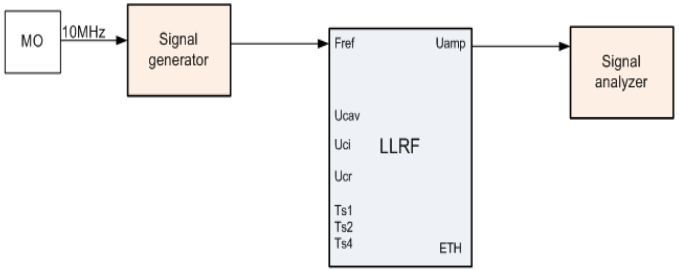
- **Fast output interlock** system (Machine protection)
- **Real time monitoring of RF signals** (incident, reflected, cavity field…)
- **Postmortem up to 0.2 us resolution** with selectable event triggers and configurable capture parameters. MATLAB, python, CSS/BOY libraries for post processing
- **RF output frequency shift +/- 1MHz**
- **Digital PLL** for tracking resonance frequency
- **EPICS** control system support and easy user interface
- **White-Rabbit** and IEEE-1588 protocols.

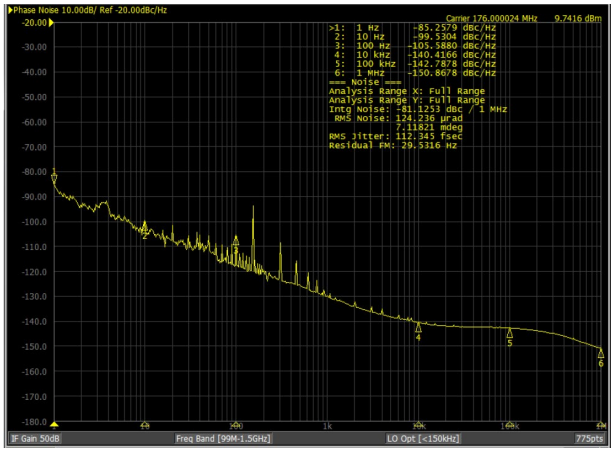
LLRF Postmortem feature

- Analize postmortem files (Excel, Matlab, Python)
- Display data in the GUI

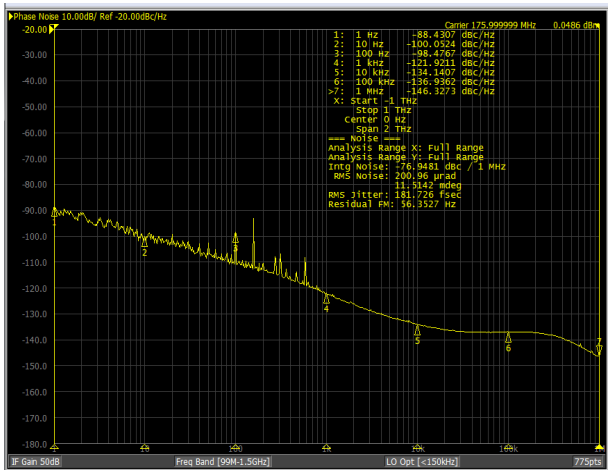


LLRF Performance results – Low jitter addition at the outputs





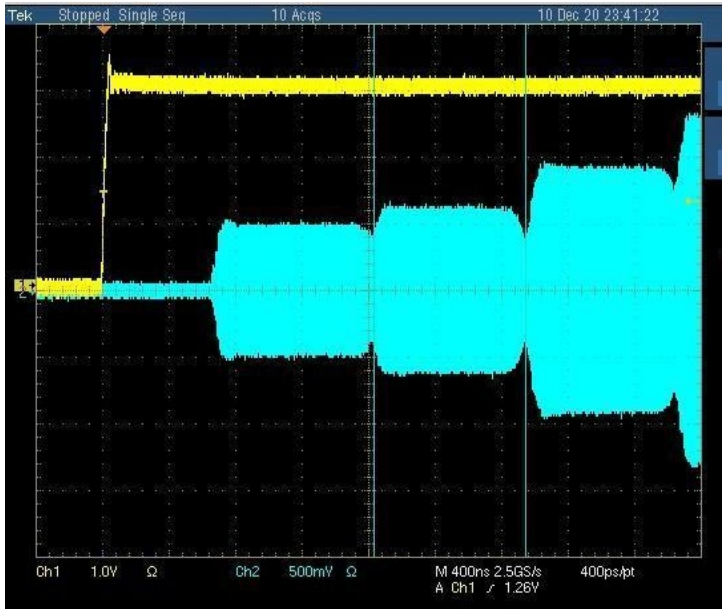
Jitter signal generator: RMS 112 fsec

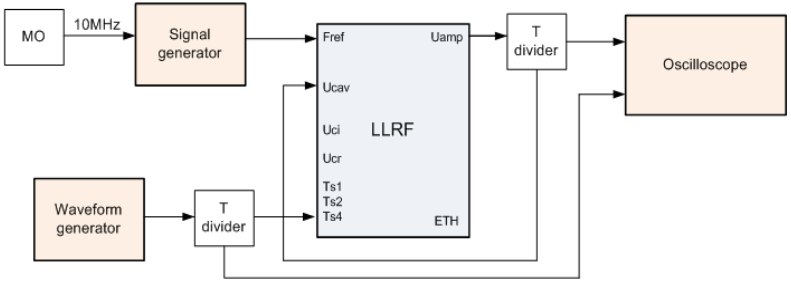


Jitter signal generator: RMS 182 fsec

Additive Jitter: RMS 70 fsec
Integration band: 1Hz - 1MHz

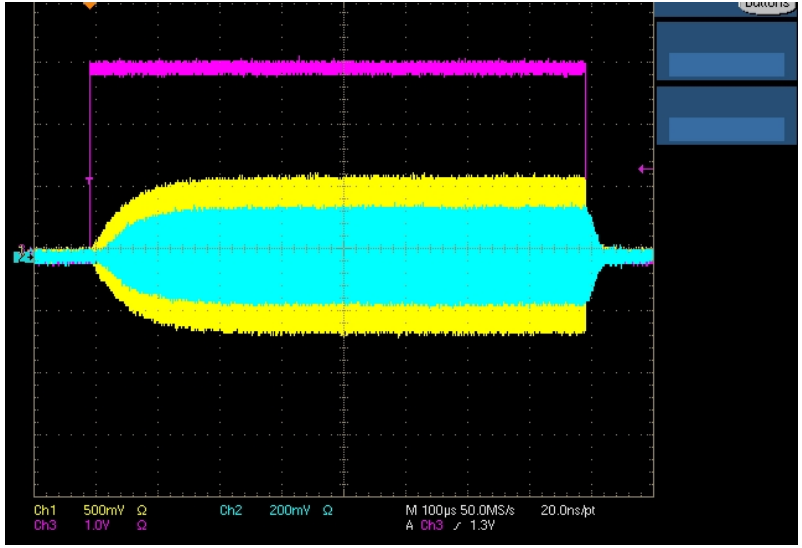
LLRF Performance results – PI delay

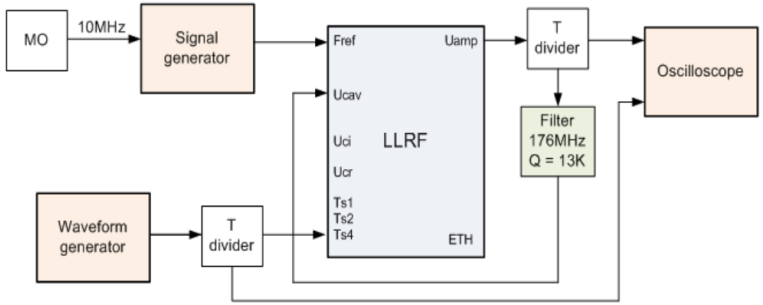




The duration of the steps produced by the effect of Kp determine the **total loop delay** of the system from RF-in to RF-out (**delay < 1us**)

LLRF Performance results – PI for amplitude and phase regulation

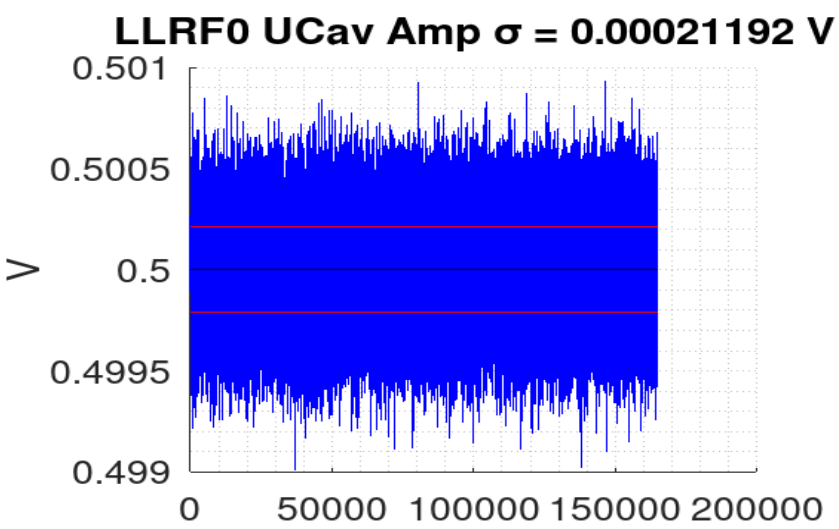


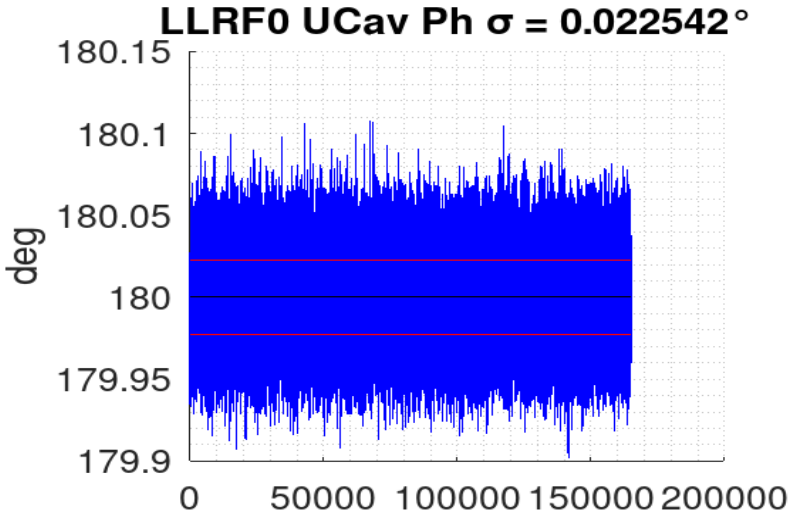


In pink, RF gate signal
In yellow RF output
In blue UCav

A high Q filter is used to emulate the cavity behaviour.
The PI controller keep constant the cavity field

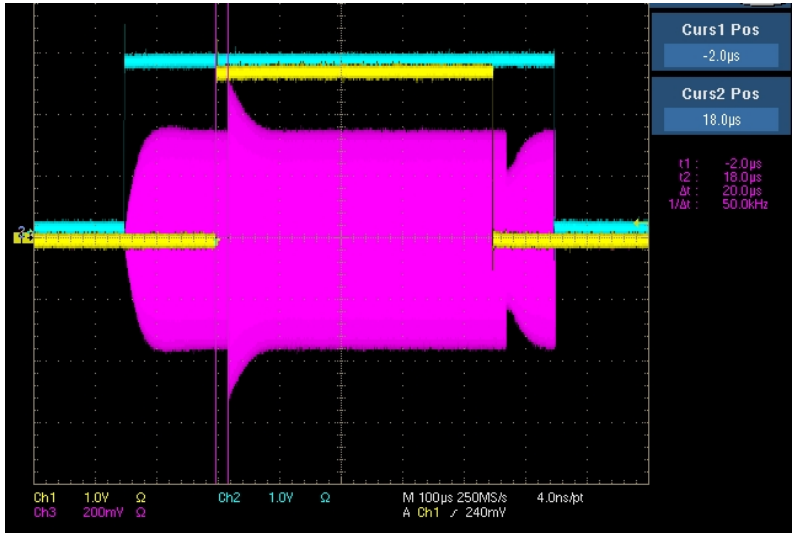
LLRF Performance results – PI for amplitude and phase regulation

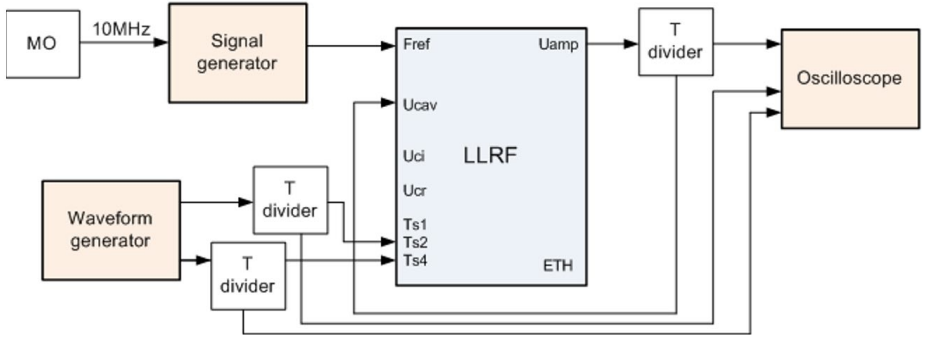




Stability in phase **0.022º**
Stability in amplitude **0.042%**

LLRF Performance results – Feedforward feature

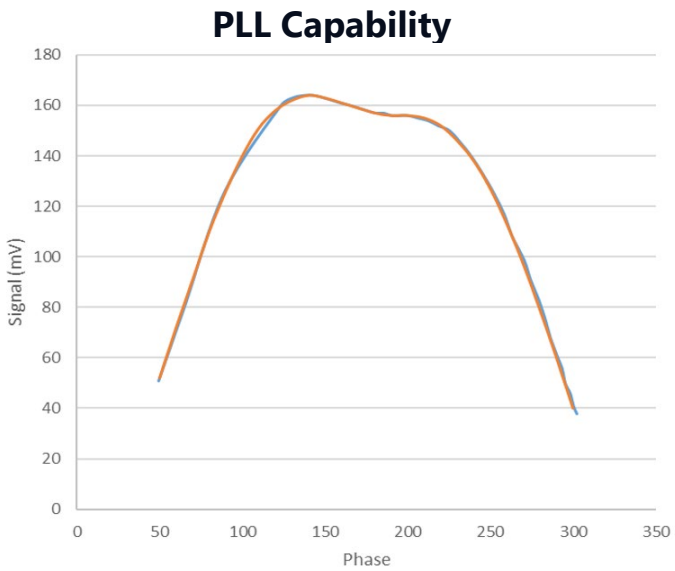


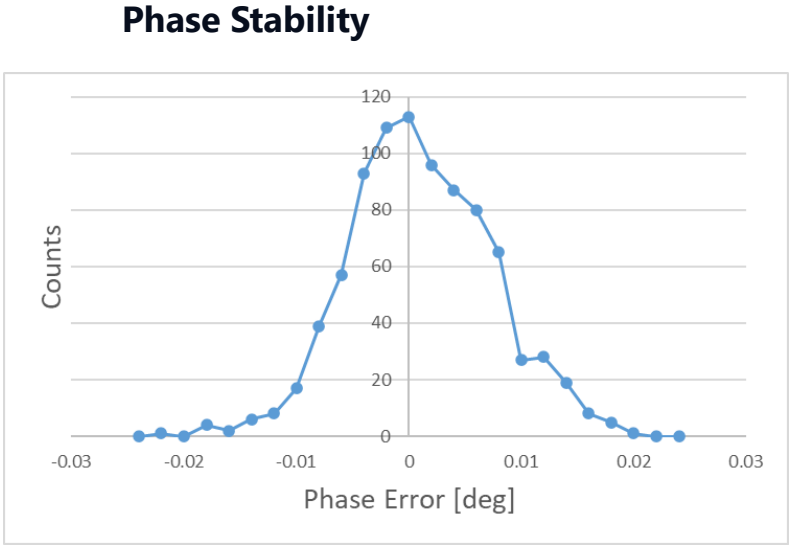


In blue RF gate signal
In yellow beam presence gate
In Pink RF output

Configurable gain and phase used to compensate the beam loading

LLRF Performance results – PLL capability





Charaterization of a cavity filter using the PLL capability

- In blue, characterization by changing frequency shift in open PLL loop
- In red, characterization by changing Phase Offset in closed PLL loop

Achieved phase stability in tests with the superconducting HWRs: **~0.006 deg [RMS]**

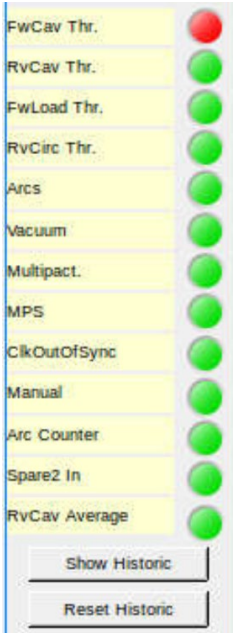
LLRF Control/Monitoring features

GUI:

- Parameters configuration
- Variables reading
- System operation

LLRF Control/Monitoring features

Interlocks status



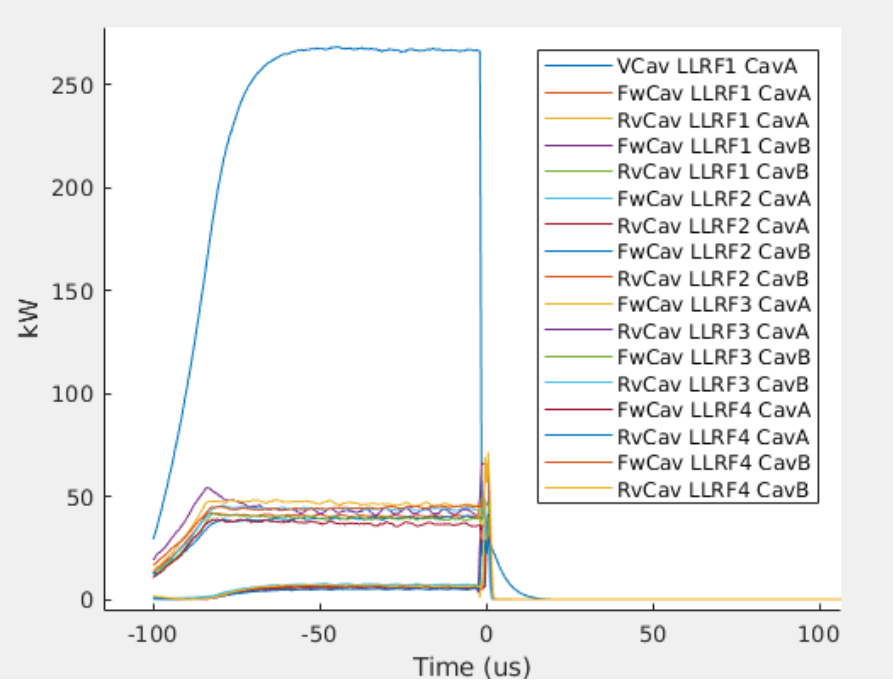
Actual interlock status

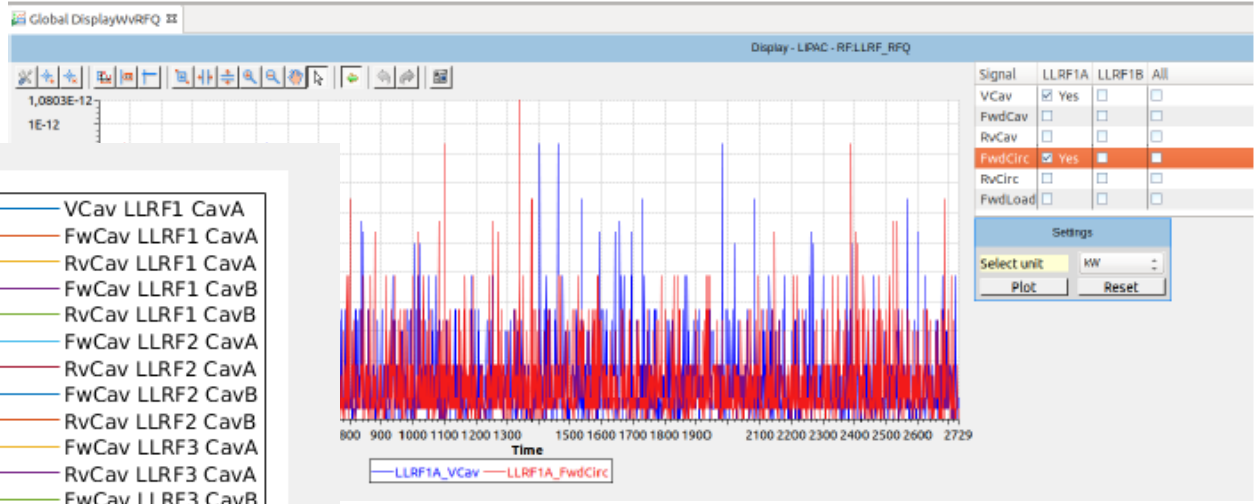
Detects the occurrence of interlocks with nanosecond precision!

Timestamp Activation	Timestamp Deactivation	Status	Interlock
13:20:43 (282,377,520 ns)			LLRF1_CavA:TxReady
	13:21:10 (615,001,570 ns)		LLRF1_CavA:TxReady
13:21:10 (615,004,110 ns)			LLRF1_CavA:FwCav
13:21:10 (615,004,120 ns)			LLRF1_CavA:FIM

Enables the view of the Historic of interlocks

LLRF Control/Monitoring features

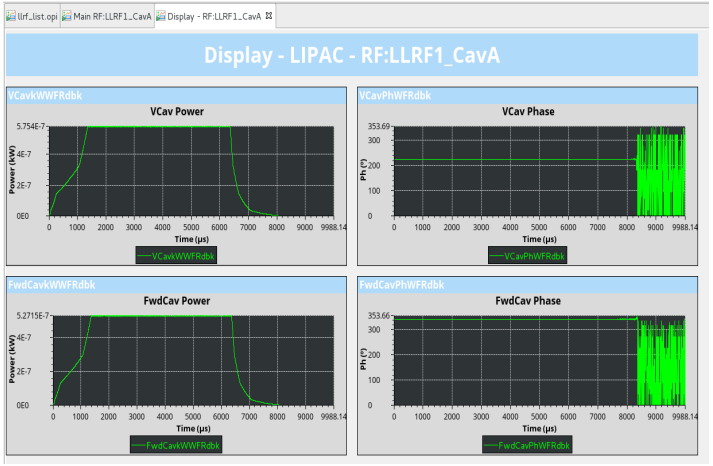


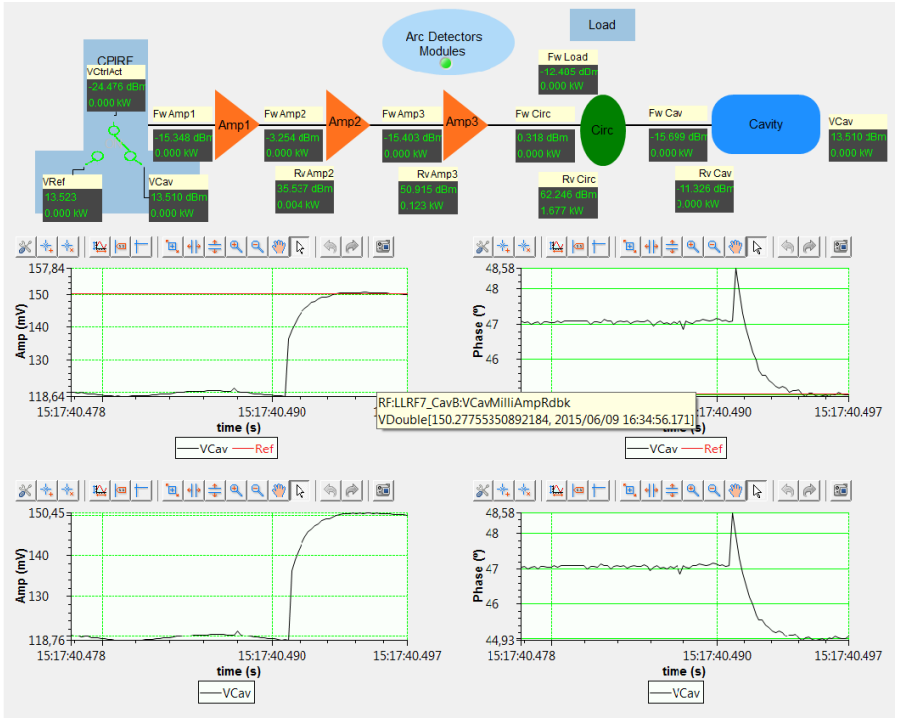


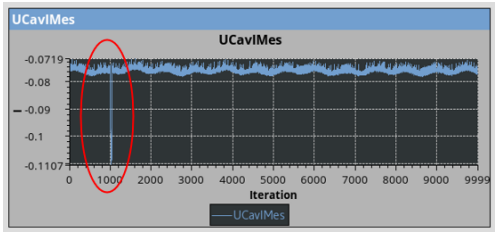
Data plotting

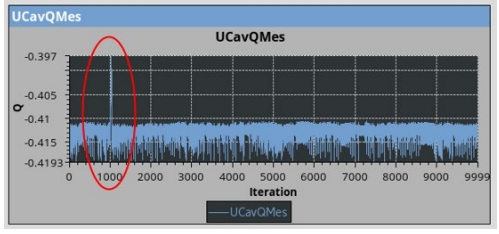
LLRF Control/Monitoring features

Real time data representation









Short beam pulse detection during commissioning

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