Gas TPC Readout Electronics

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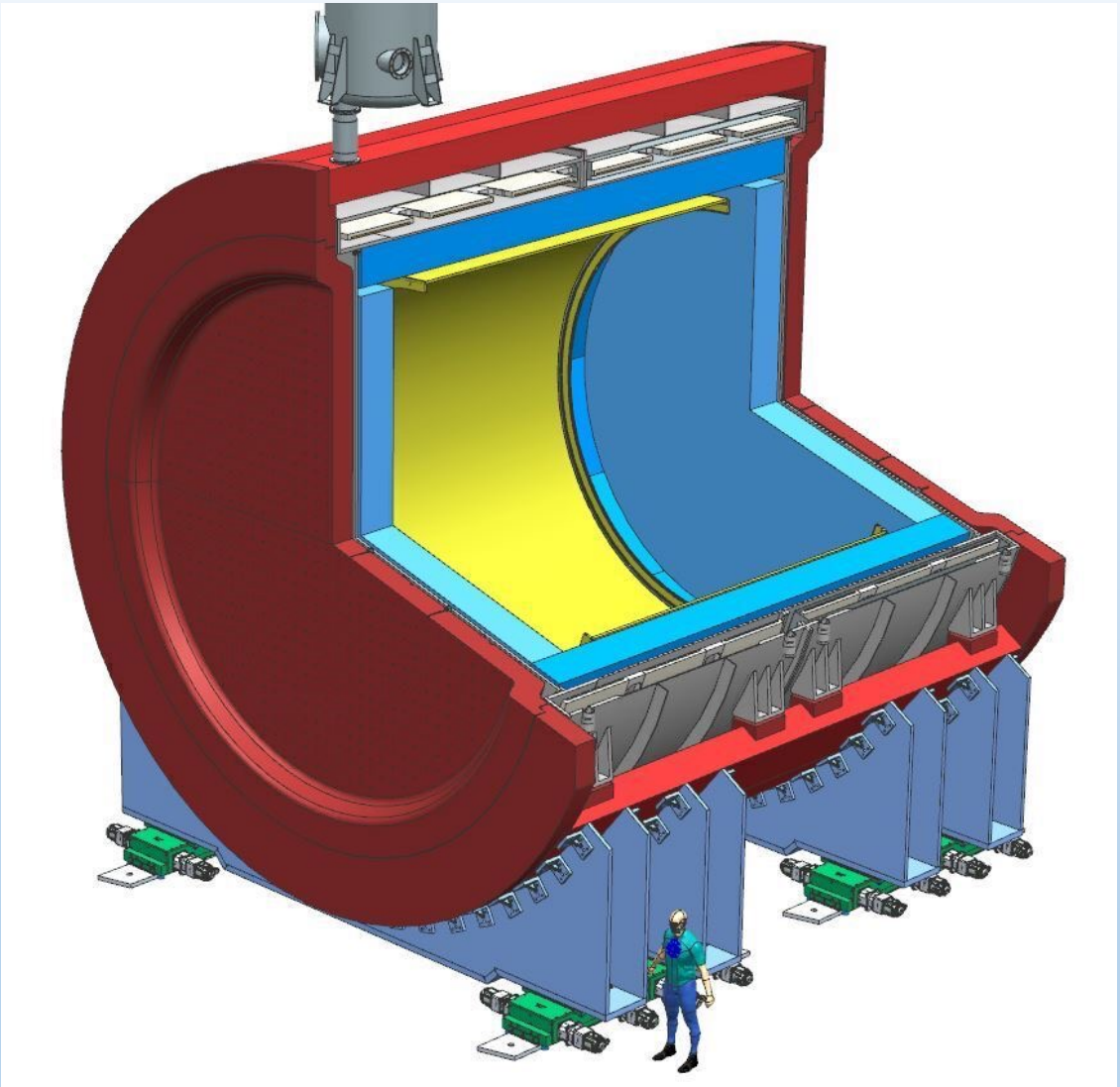
Introduction

- Introduce requirements for gas TPC electronics



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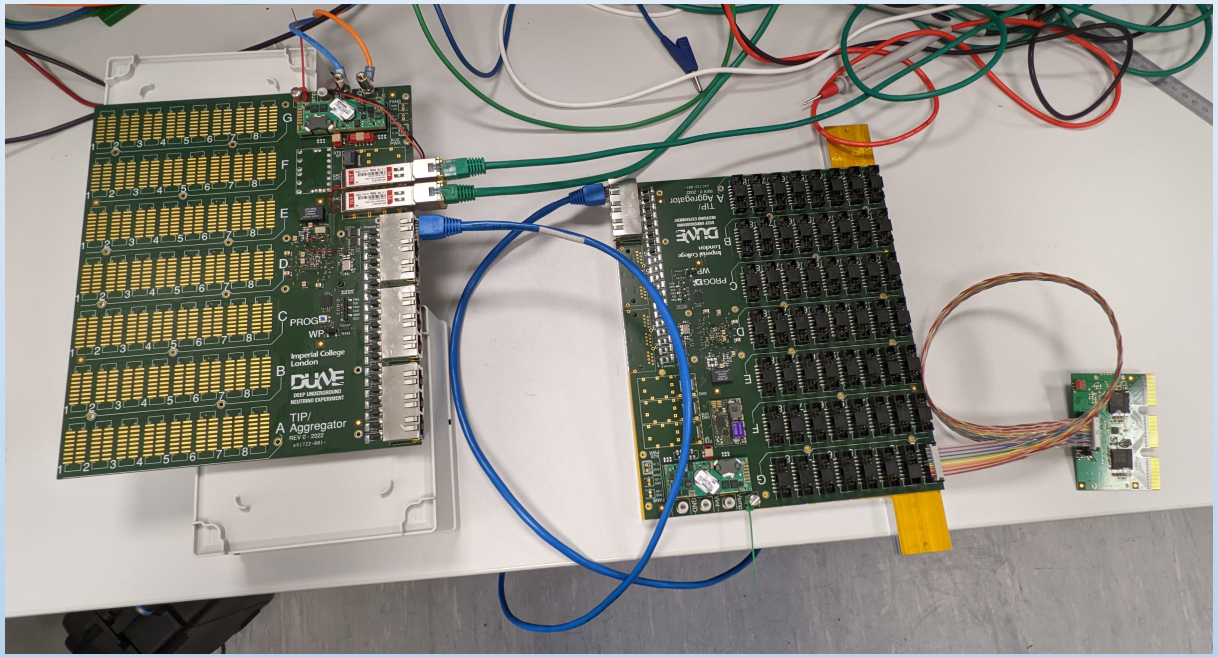
Introduction

- Introduce requirements for gas TPC electronics
- Describe system designed so far
  - including how we've made it much cheaper than sPHENIX/ALICE's systems



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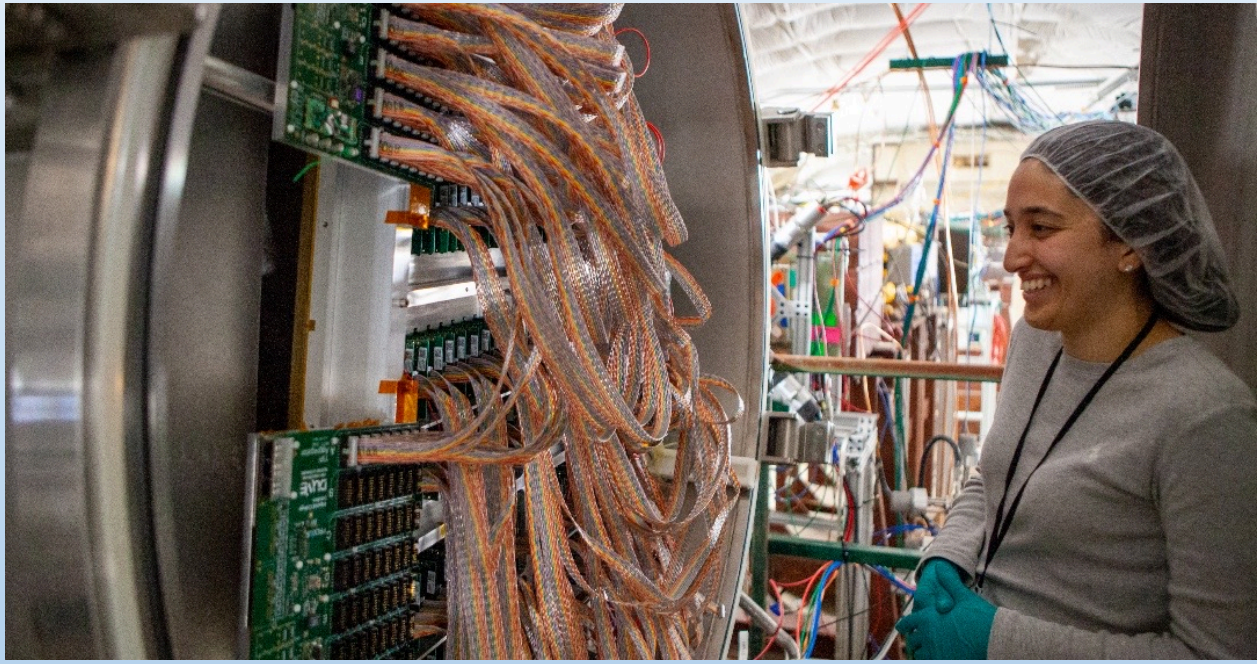
Introduction

- Introduce requirements for gas TPC electronics
- Describe system designed so far
  - including how we've made it much cheaper than sPHENIX/ALICE's systems
- Outline current prototyping progress including tests at TOAD



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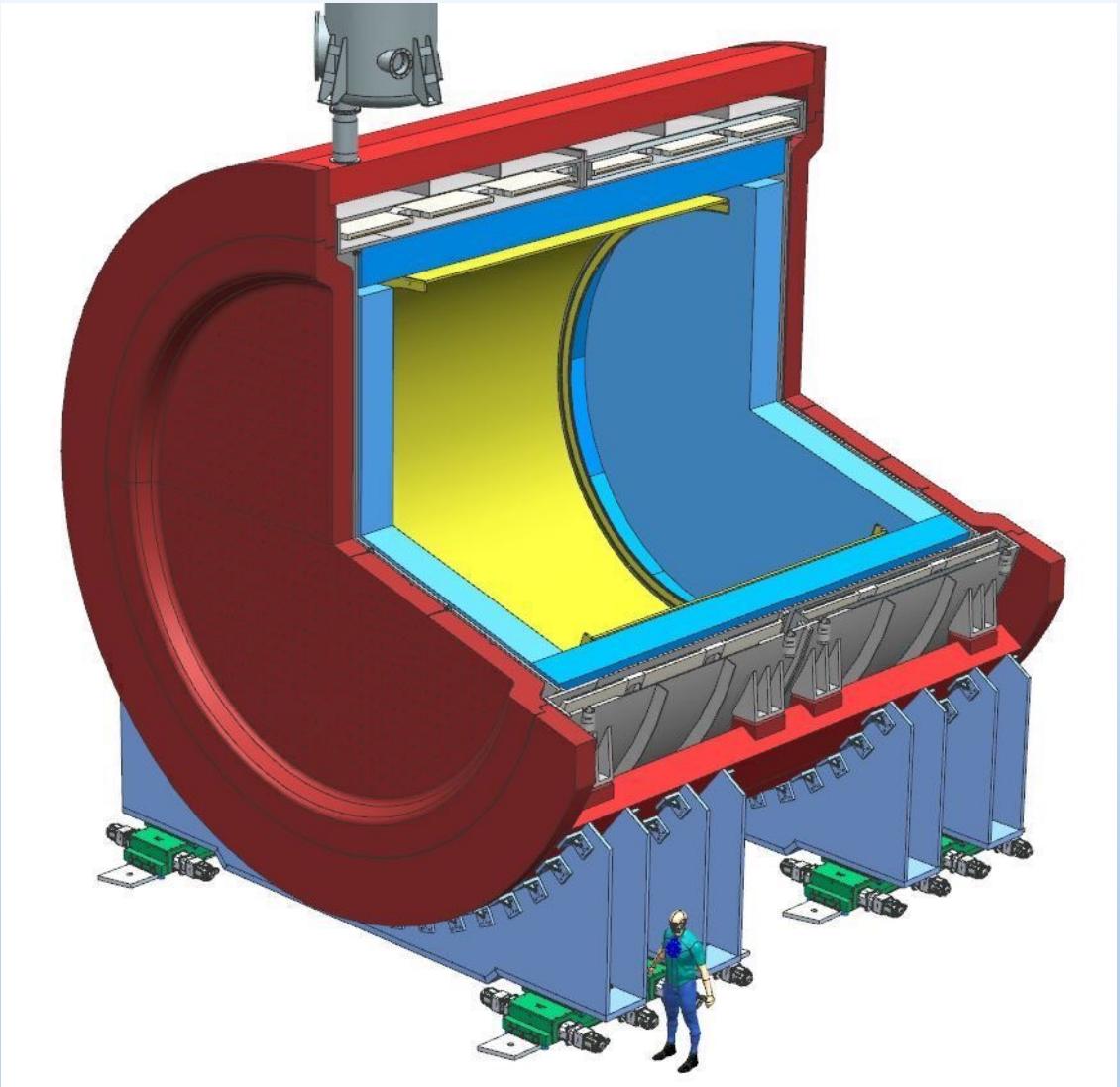
System Requirements



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Requirements and differences from LAr

- Cm-scale track resolution means few mm2 pixel spacing
  - Implies ~350k channels per end of the detector.
- HPgTPC is a gaseous TPC so drift speed is faster than LAr
  - Matching pixel spacing in drift direction we'd want to sample at ~mm-scale
- We haven't decided on our amplification stage
  - Designed system should be flexible to allow GEMs vs wires etc.
- Our detector is in a pressure vessel
  - Electronics must minimise penetrations of the pressure vessel
  - We must digitise inside the pressure vessel or analogue path will give large noise
- Shouldn't require redesign of wider DUNE ND DAQ
  - Other detectors use streaming triggerless readout

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Choosing an ASIC – Sample frequency

- Choice of digitizer ASIC must have sufficient sampling frequency
- Argon gas has drift velocities O(10cm/us)

Required resolution	Implied Sampling Frequency
1cm	10 MHz
1mm	100 MHz
100um	1 GHz

- Ignores longitudinal diffusion
- However, these are single sample resolutions so significant improvement from fitting multiple samples from adjacent pixels
  - ALICE achieve 1300um precision with 5-10 MHz sampling

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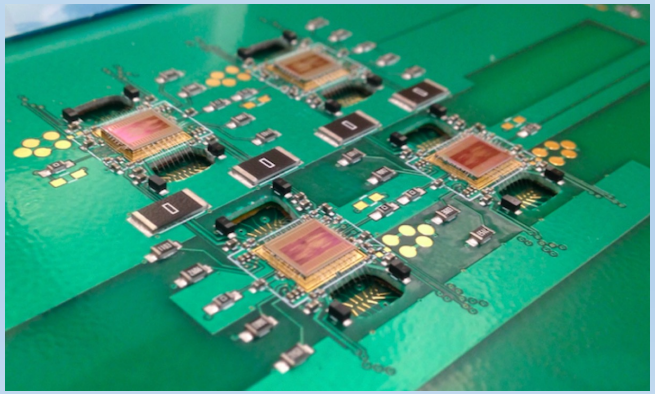
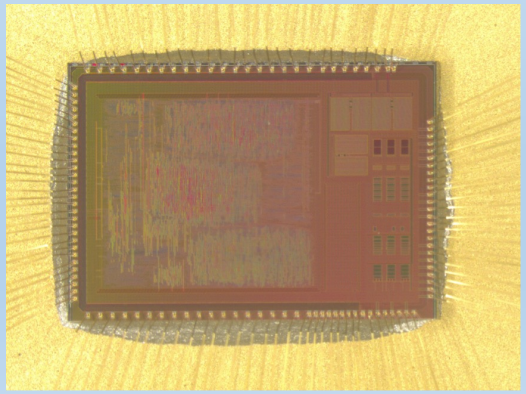
Digitiser ASIC options

- Needs to be magnetic tolerant and have appropriate resolution and gain
- Thermal budget is also important
- 3 possible options considered:

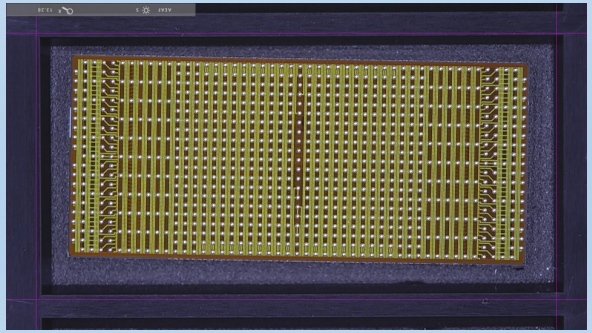
LArPix v2 chip
- 64 channels at 500kHz
- Speed would need upgrading
- ~100 uW/channel (more with speed increase)



SAMPA chip developed for ALICE TPC upgrade and sPHENIX
- 32 channels at 5 or 10 MHz
- ~35 mW/channel



HGROC chip developed for CMS HGCAL
- 72 channels at 40 MHz
- ~15 mW/channel
- Not designed for wire chambers



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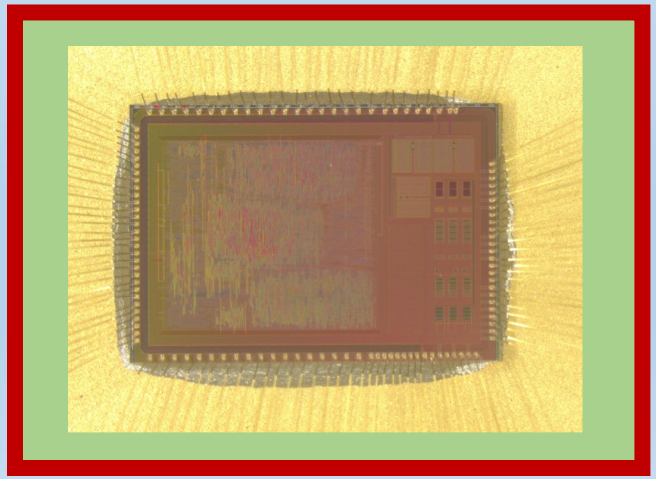
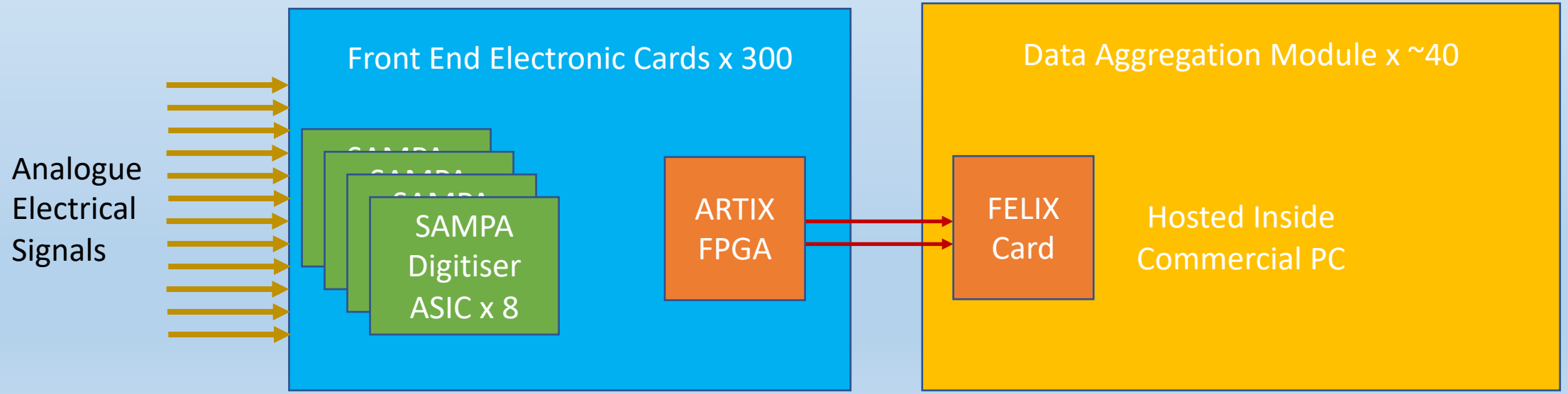
Digitiser ASIC options

- SAMPA ASIC has desired sampling rate with no upgrade
- Has resolution and gain suitable for both wire and GEM readout TPCs
  - Has been used with both
- Designed to support zero-suppressed streaming triggerless readout
- Available for prototyping and we have assurances that we could make more for full ND-GAr at reasonable cost



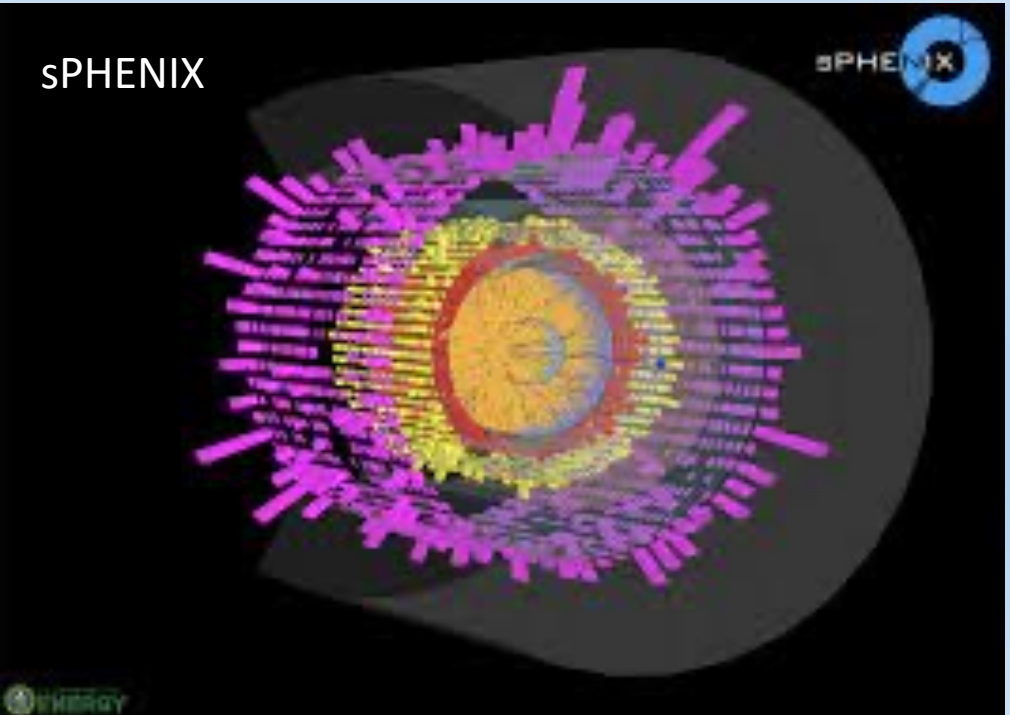
Starting point and cost comparison

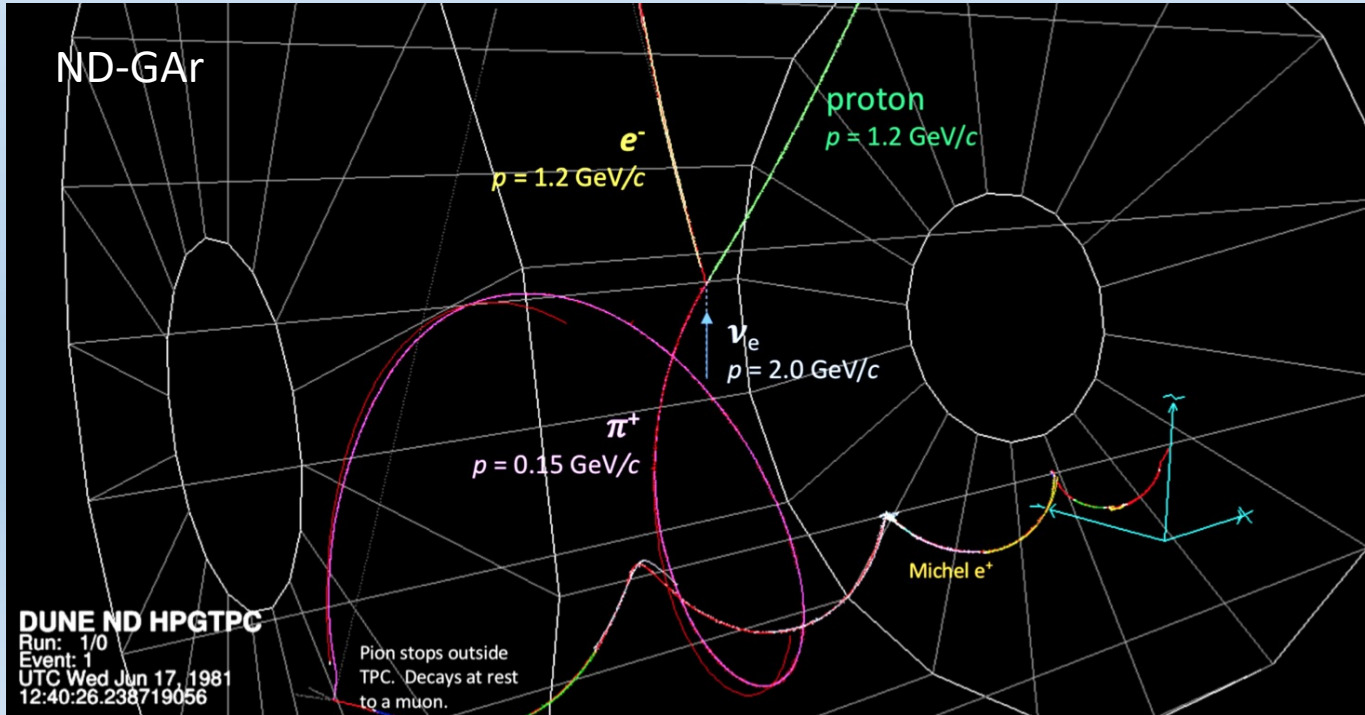
- Funding agencies want to know what this will cost
- Natural comparison is to sPHENIX which uses same digitiser
- Scaling up sPHENIX system cost by channel count gives ~$100M
- This is large enough to drive the overall detector cost



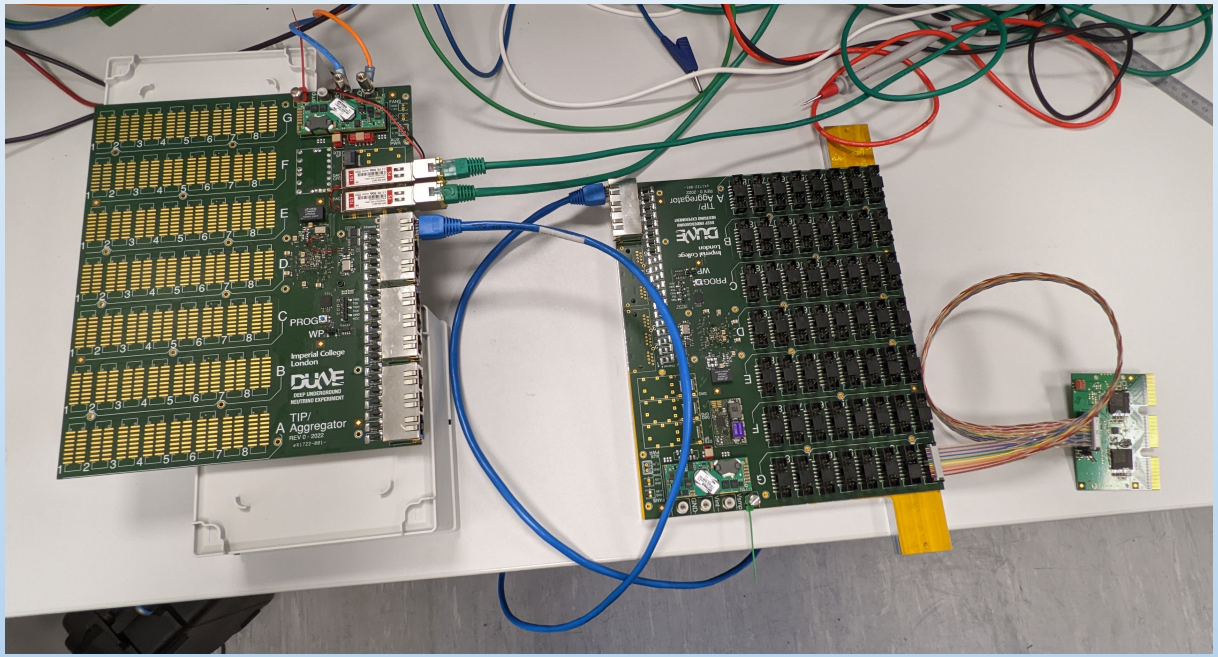
Why we are not sPHENIX

- sPHENIX bunch crossing rate is 200 kHz → We have O(1 Hz)
- We see O(10s) of tracks per spill not nearly saturated heavy ion events
- Both mean many more digitisers per FPGA and less sophisticated backend
- Initial cost estimates for system described today of ~£2M for 700k channels





System Design



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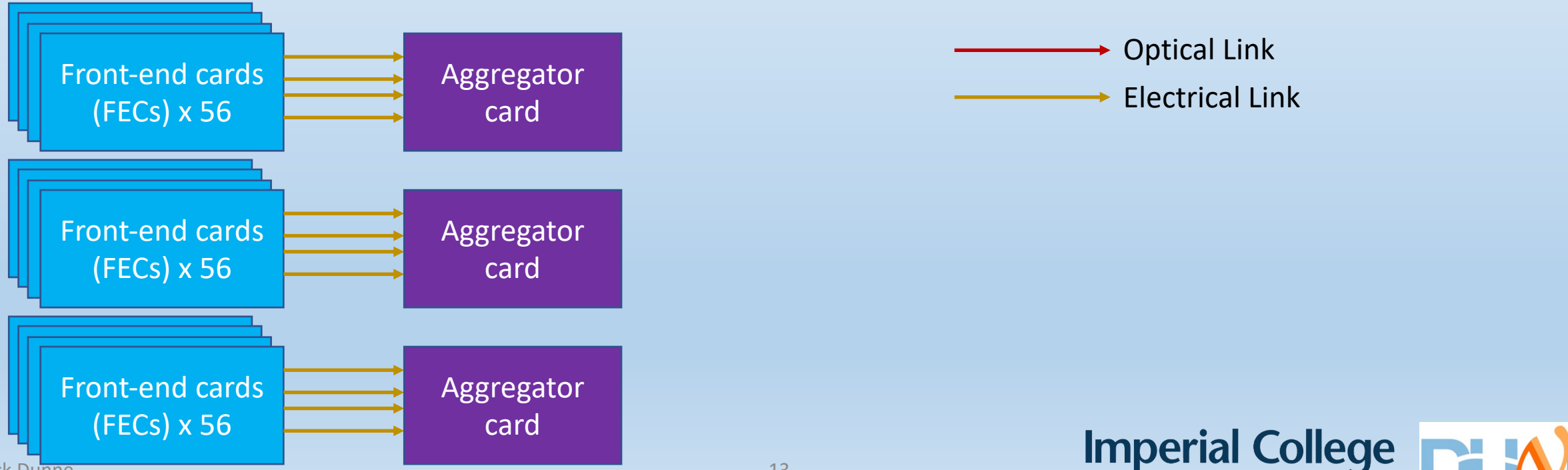
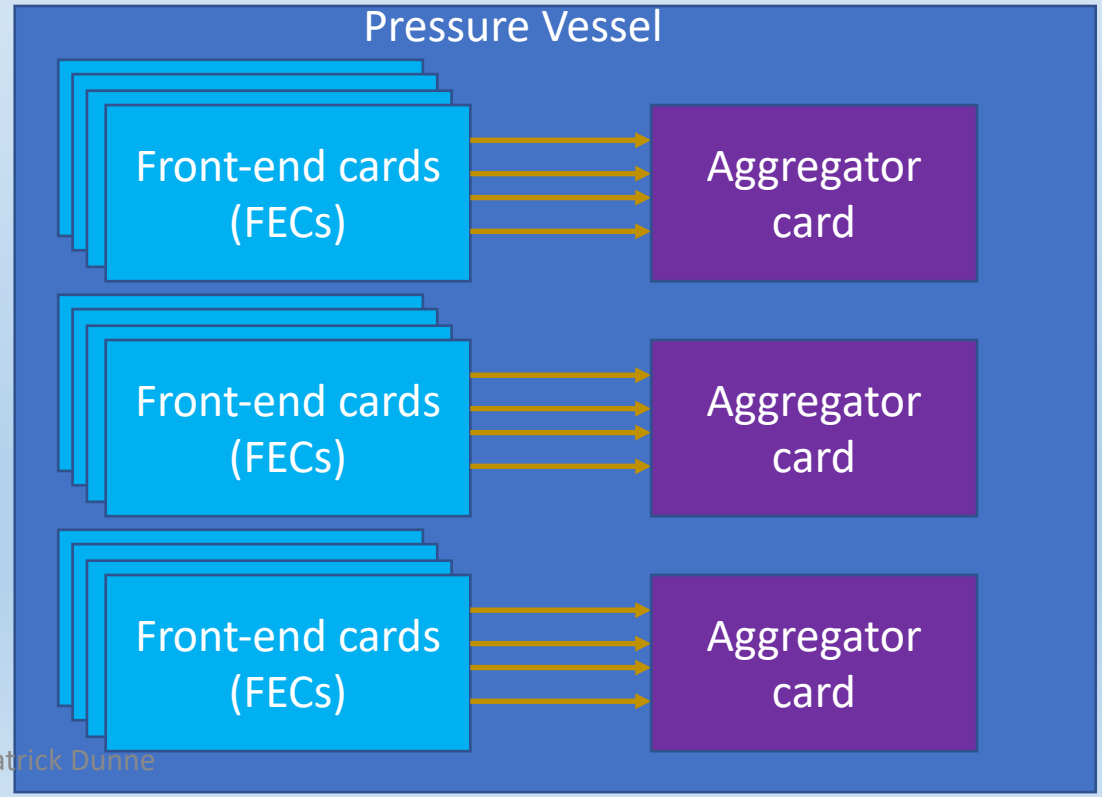
System design – FPGAs per channel

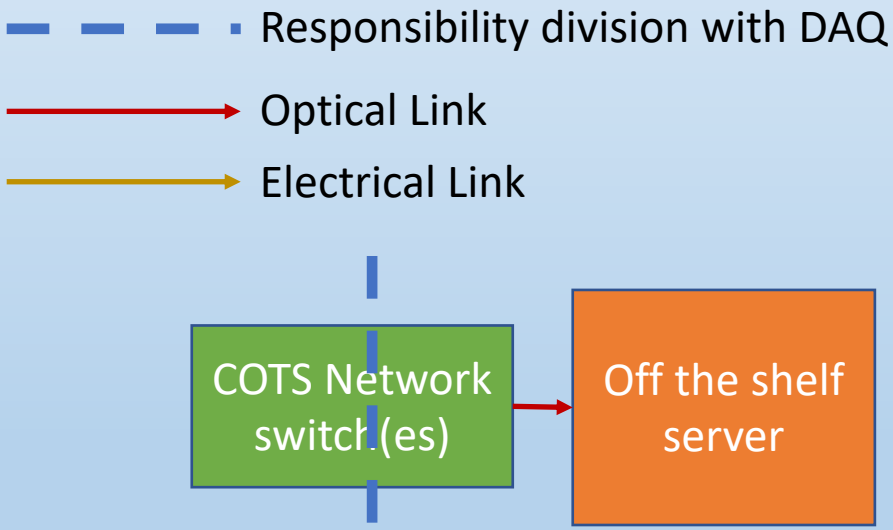
- Number of ASICs per FPGA driven by connector count not data rate
- ALICE connector has 64 channels meaning 2 ASICs per front end card (FEC)
  - ~5,500 FECs per end of the detector
- FPGA has enough links for 56 FECs per FPGA → ~100 aggregation FPGAs per end
  - One FPGA per 112 ASICs → order of magnitude fewer FPGAs per channel than sPHENIX



System design – Getting from pressure to DAQ

- Cannot have 5,500 pressure vessel penetrations so aggregation must be inside
- DUNE ND DAQ requires connection to off the shelf TCP network switches
- We must also power the in-vessel electronics and distribute timing information





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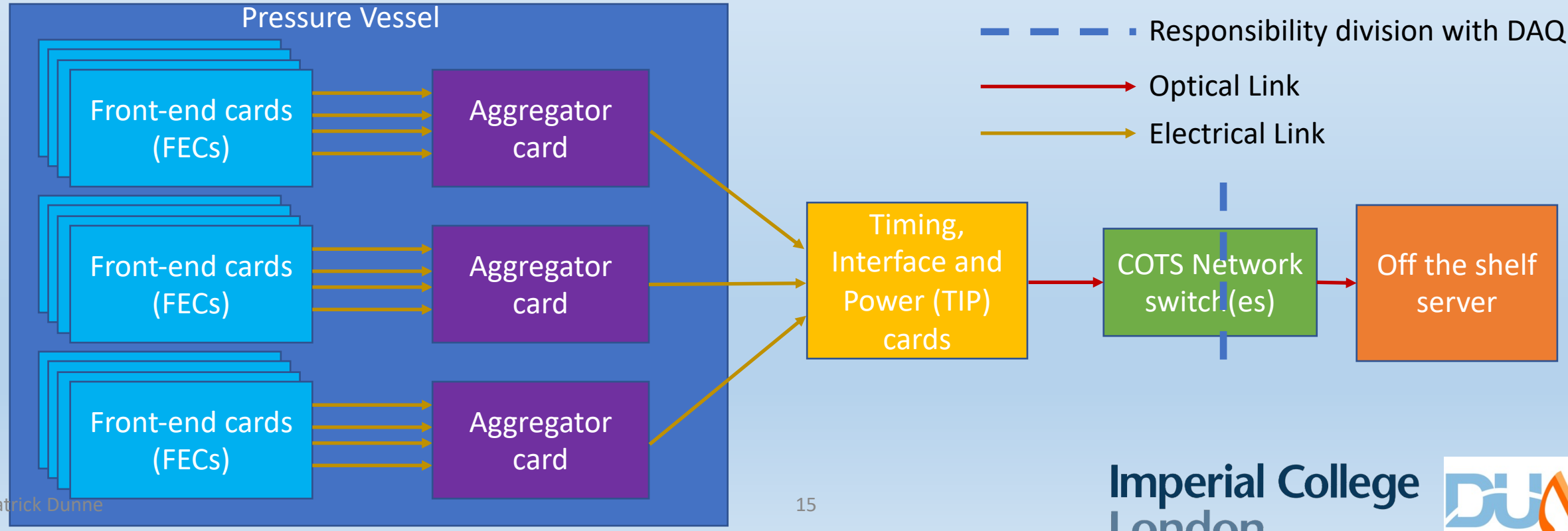
System design – Getting from pressure to DAQ

- Timing, interface and power (TIP) cards each handle 9 aggregators
  - 12 TIPs per detector end
- Power delivered down signal cables similarly to power over ethernet
- TIPs further aggregate signal and convert to TCP over Gb ethernet



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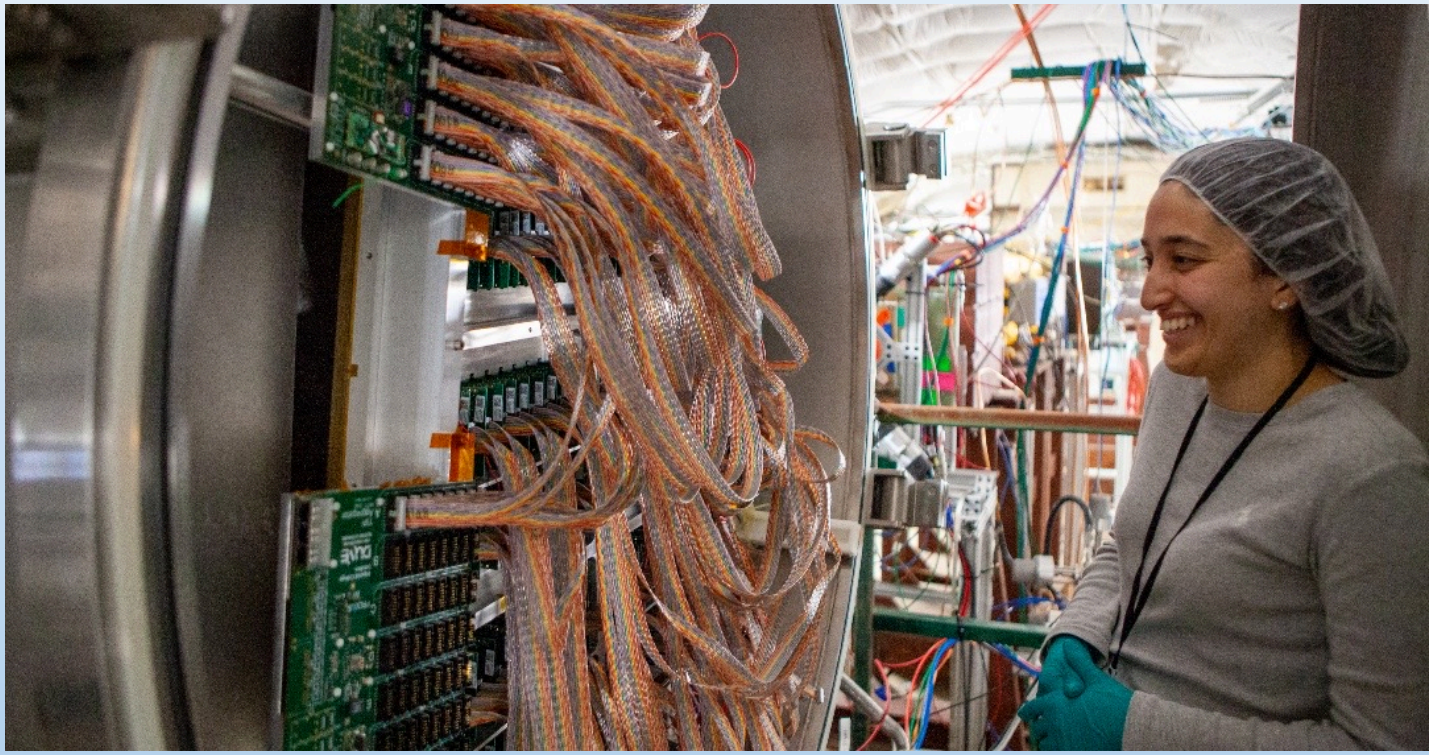
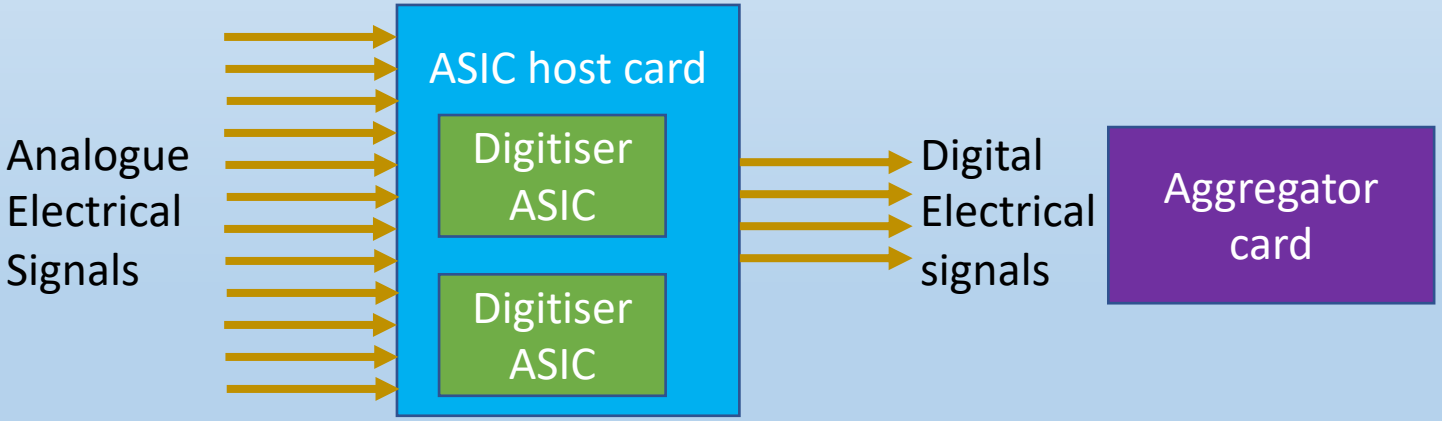
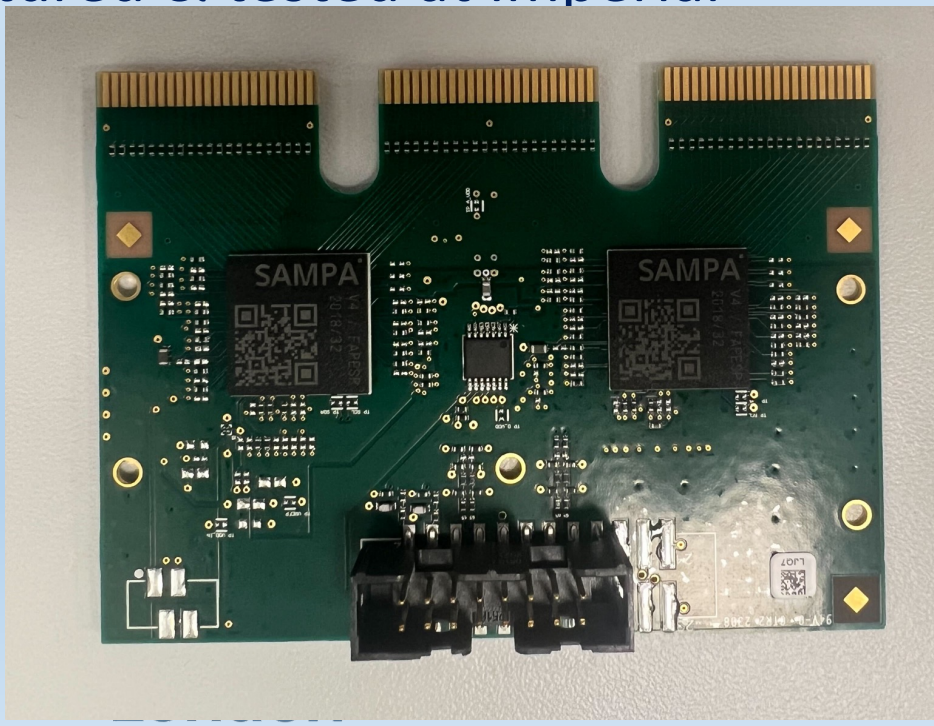
Design, Prototyping & Testing



Front end cards (FECs)

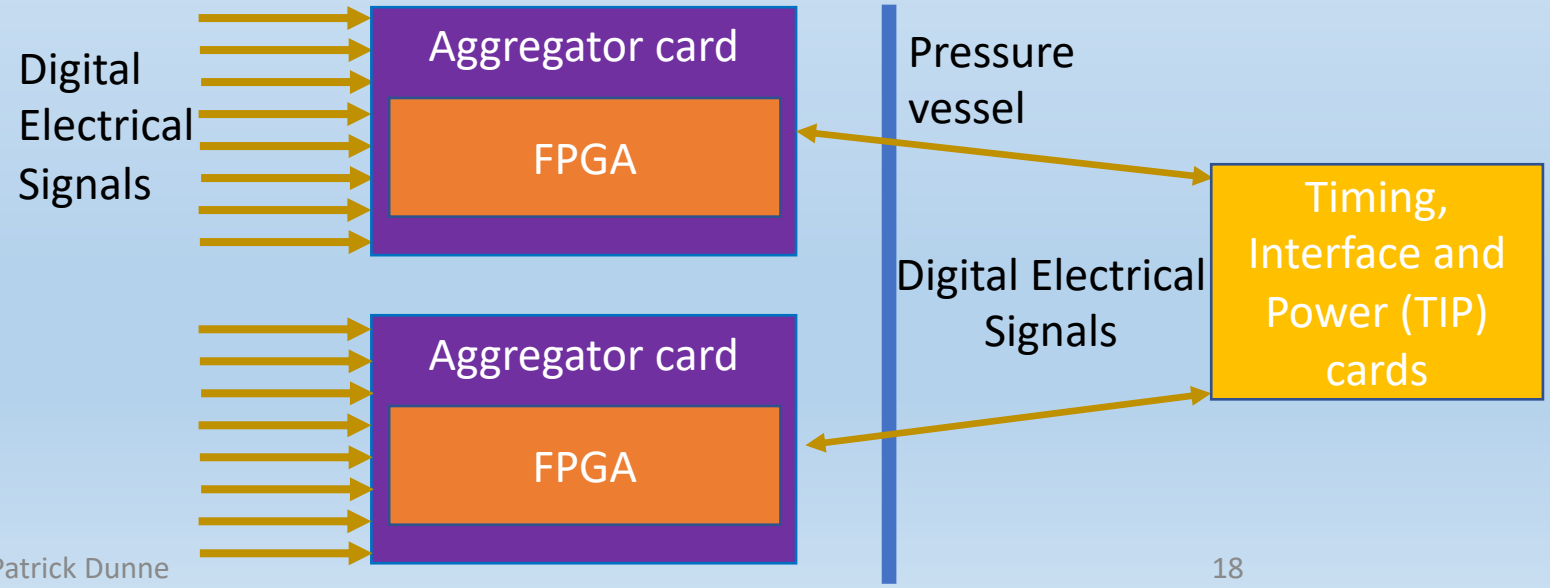
- Input is analogue electrical signals from detector
  - Positioned on-detector using 64 channel edge connector
- 2 SAMPA ASICs hosted on each card
- ASICs are daisy chained with one primary ASIC communicating with aggregator and other ASIC using custom protocol
- Cards designed by Fermilab/Pittsburgh, 160 manufactured & tested at Imperial

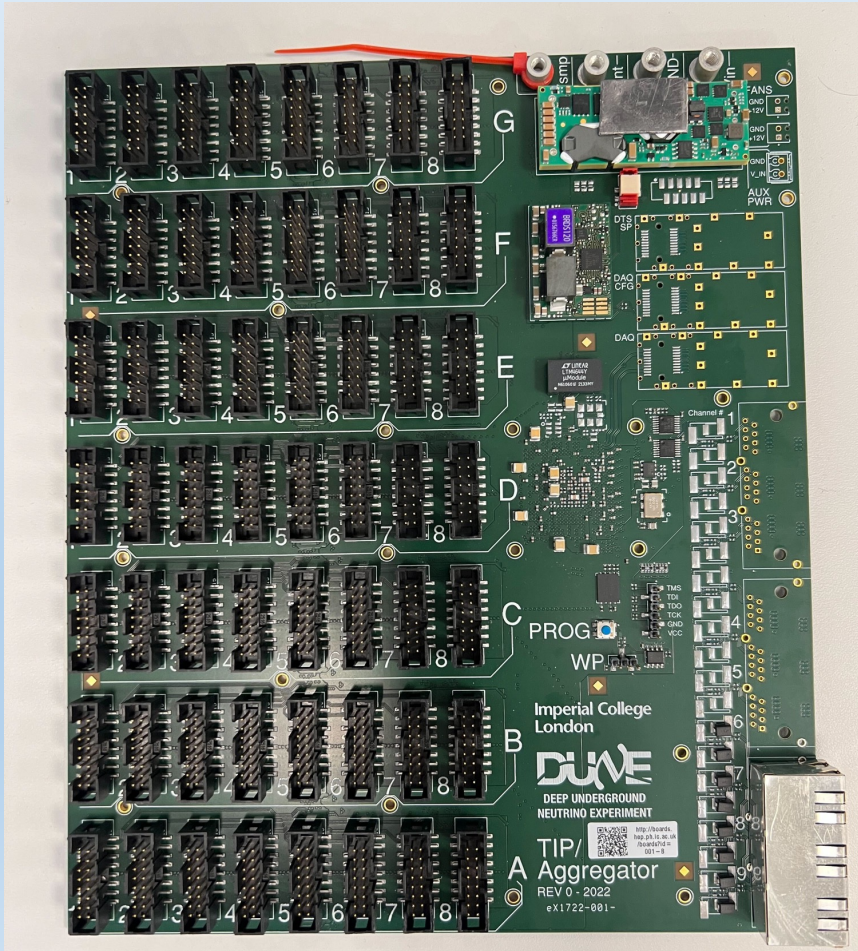




Aggregator cards

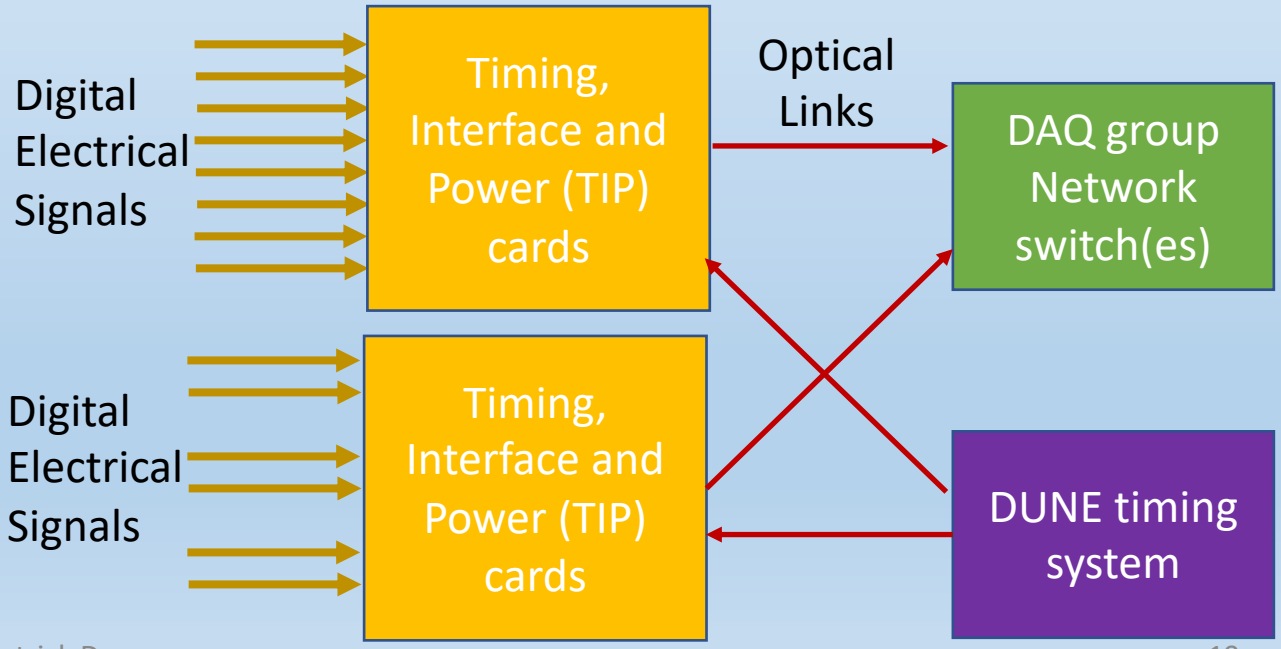
- Input is custom protocol electrical signals from ASIC cards
- Controls and powers ASIC cards and consolidates into fewer links
- Communicates with TIP using AURORA protocol using ethernet cables which are also used for power
- Designed, manufactured and had firmware written at Imperial

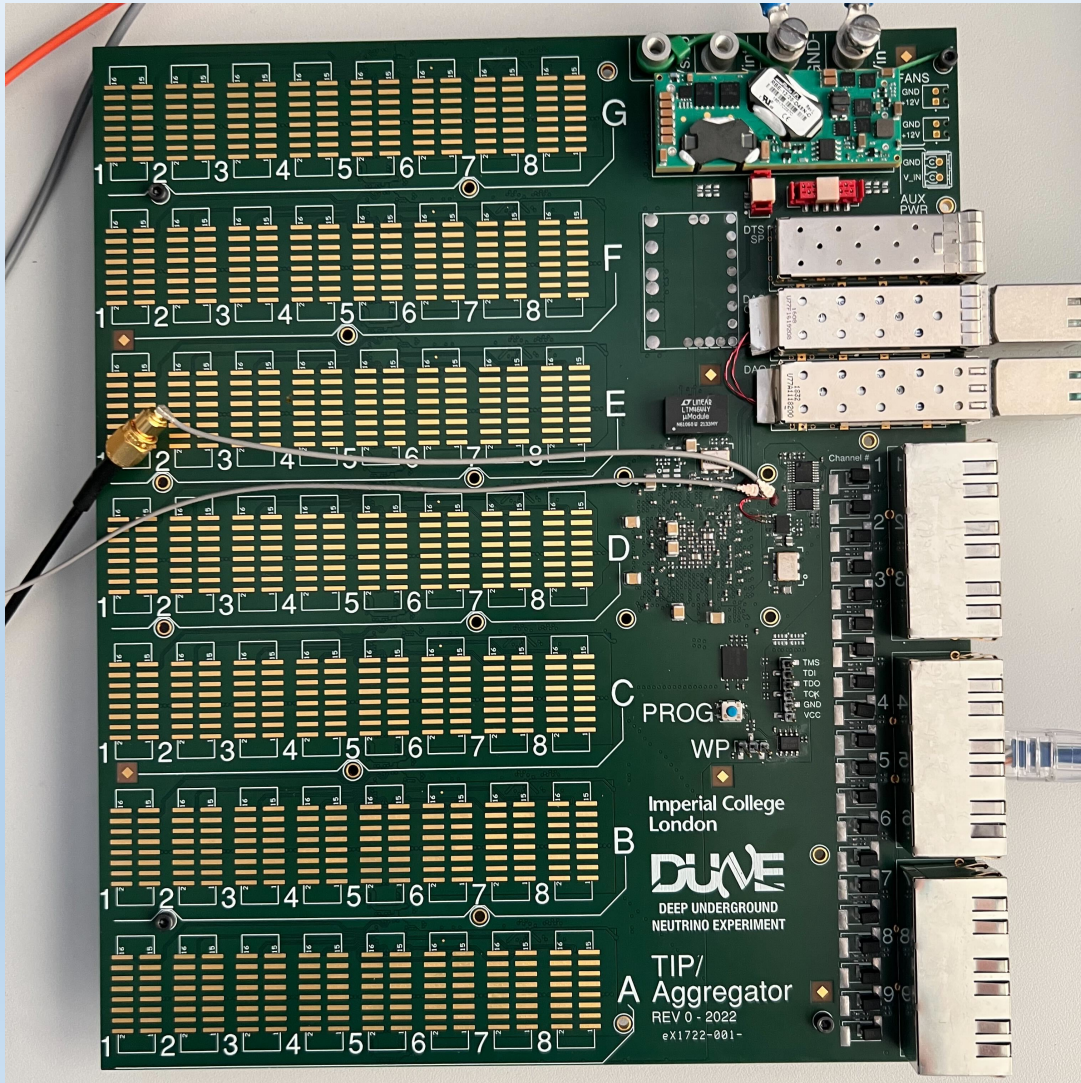




Timing, Interface and Power (TIP) cards

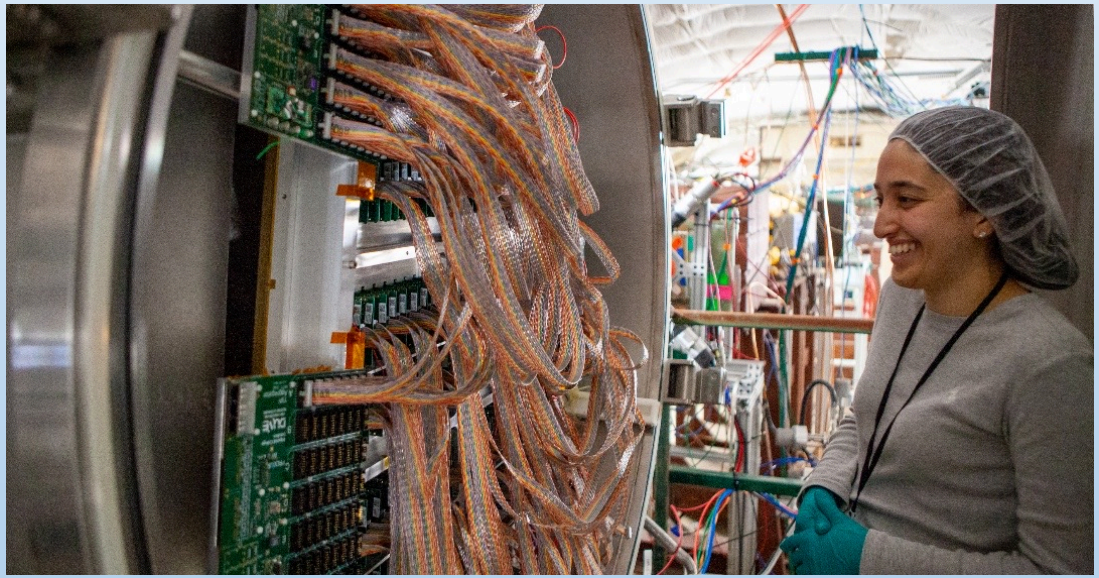
- Input is AURORA links from aggregator
- Controls and powers aggregator cards and interfacing between DAQ consortium hardware and our electronics
- Already fully integrated with DUNE FD1 timing system and DAQ software including control, configuration and monitoring system
- Designed, manufactured and had firmware written at IC





Testing at TOAD

- 10,000 channels of the TOAD experiment are currently instrumented with this system
- We are in the process of commissioning the system
  - Pressure, noise, stability testing
- After TOAD concludes we will take lessons learned and build v2 of each component
- UK R&D funding secure for several more iterations



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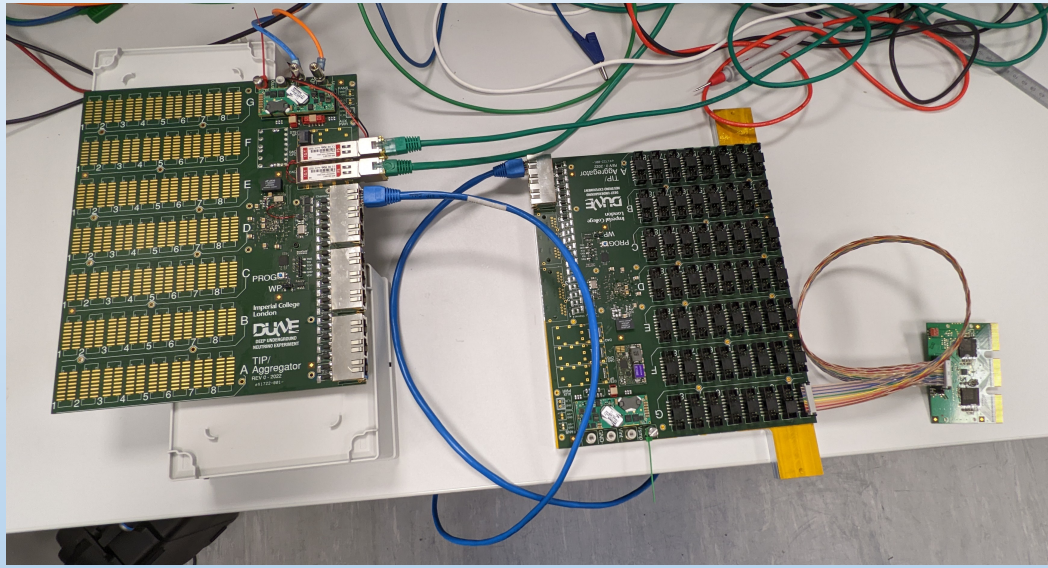
Summary

- TPC readout electronics design and prototyping is well underway
- System uses existing SAMPA ASIC to reduce R&D risk and increase versatility
  - Minimal changes needed to operate with a different charge amplification stage
- Much lower neutrino experiment data rates allow much cheaper system than sPHENIX
  - Initial estimate is £2M for full 700k channel system
- TOAD will provide a full slice test of 10,000 channels operating in beam
- More details in talks from Ioannis Xiotidis and Naseem Khan at ND-GAr meetings



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