DEEP UNDERGROUND NEUTRINO EXPERIMENT

Brookhaven National Laboratory

U.S. DEPARTMENT OF ENERGY

Development of DAT for DUNE ASICs QC Tests

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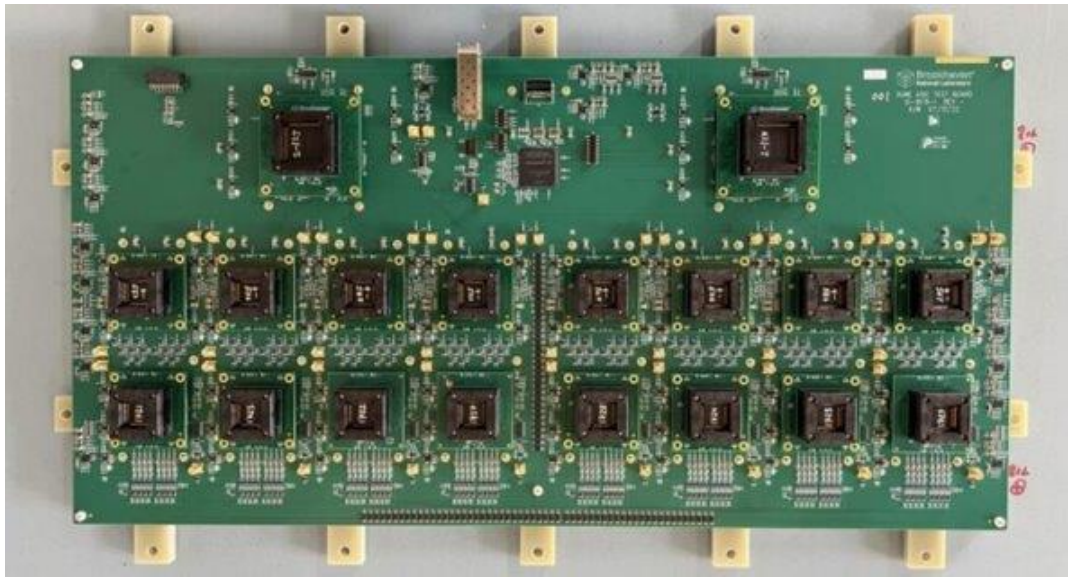
Outline

- DAT goals
- Hardware overview
- Monitoring capabilities
- Test pulse injection
- Preliminary results
- Software toolset
- Current development status

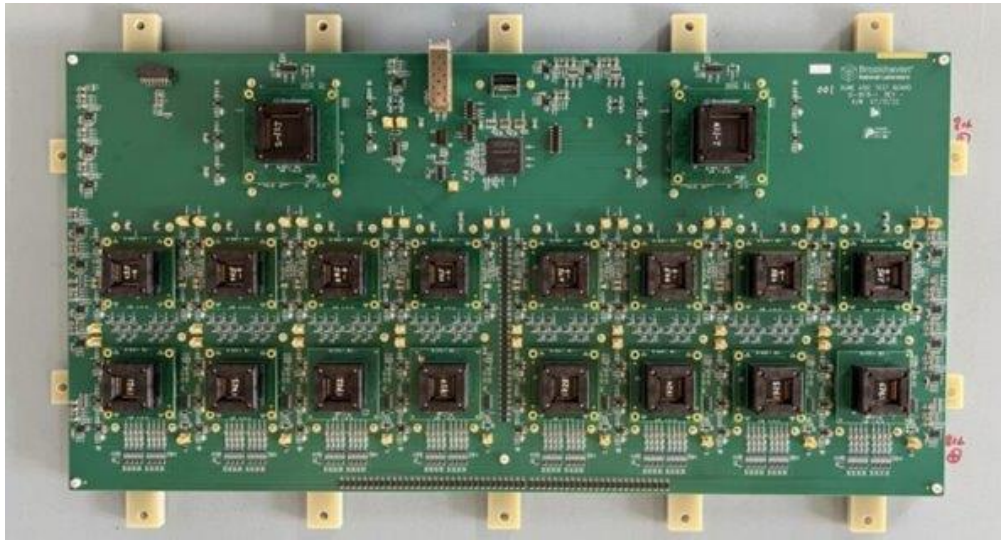


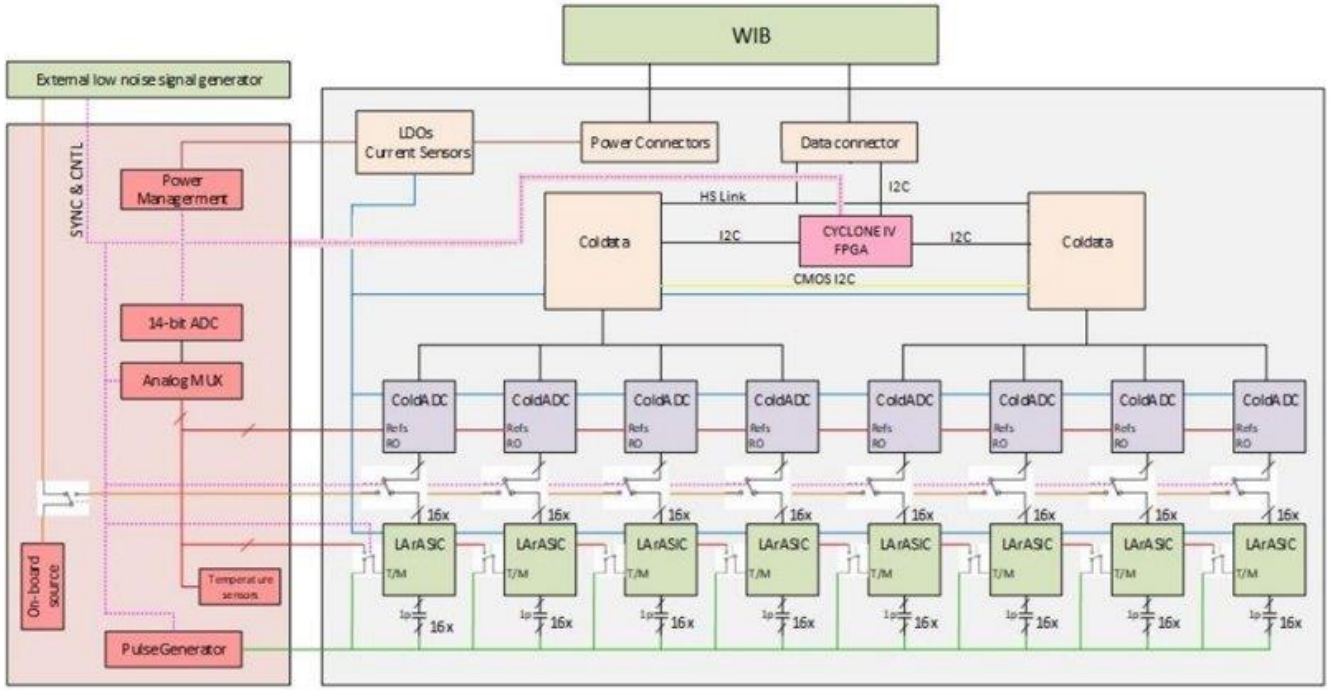
DAT Goals

- Test 1 FEMB's worth of ASICs
  - 2 COLDATA ASICs
  - 8 ColdADC ASICs
  - 8 LArASICs
- Ability to monitor all ASIC power rails
- Test all ASIC analog and digital IO
- Increased test pulse injection capability over FEMB
- Needs to be compatible with production WIB firmware
  - Will use a superset of current WIB software for QC tests

Hardware Overview

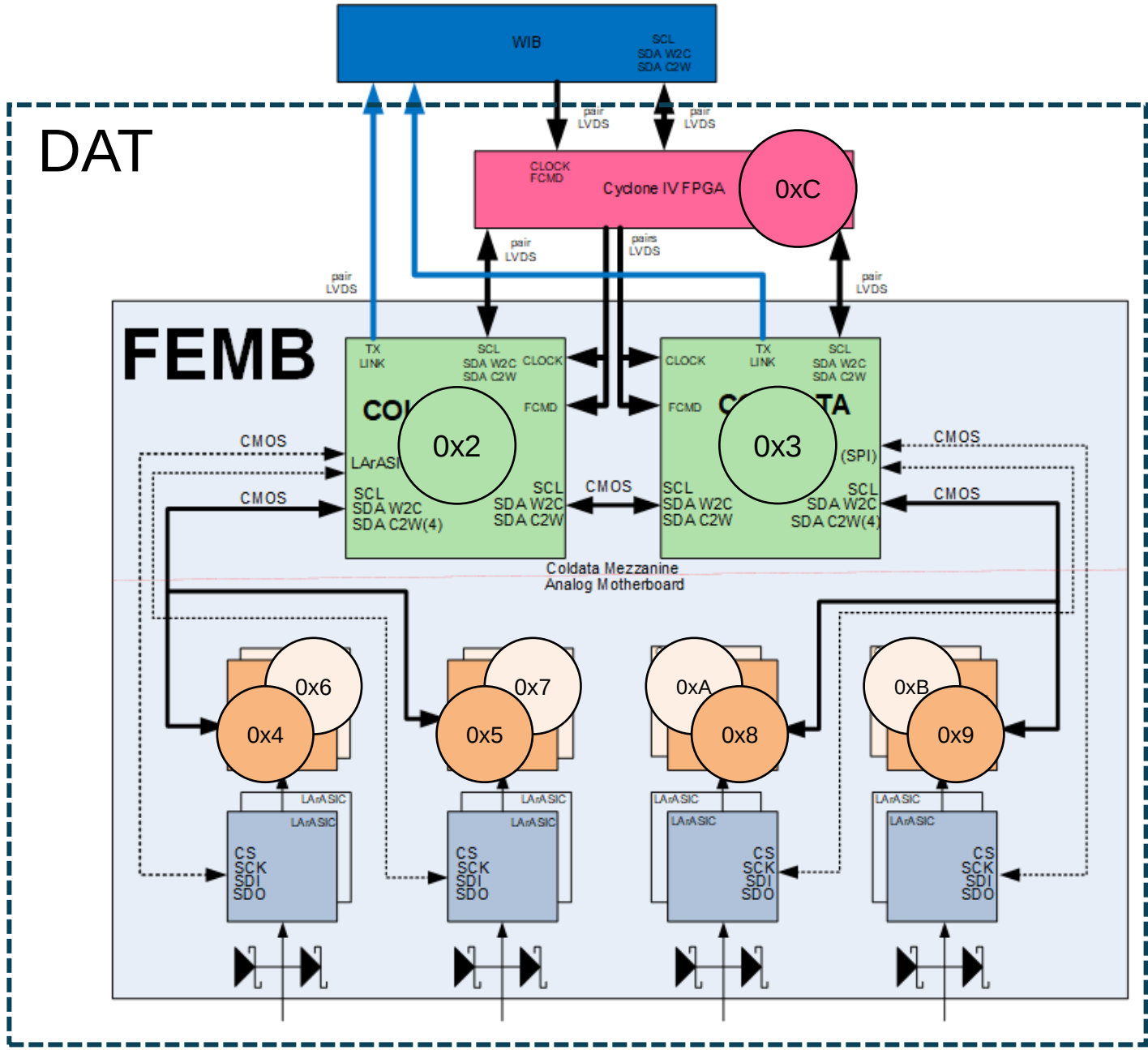
- Intel Cyclone IV FPGA
- Replaceable ASIC sockets
- Voltage and current monitors
- Reconfigurable IO
- Multiple test DACs
- All components cryo-capable



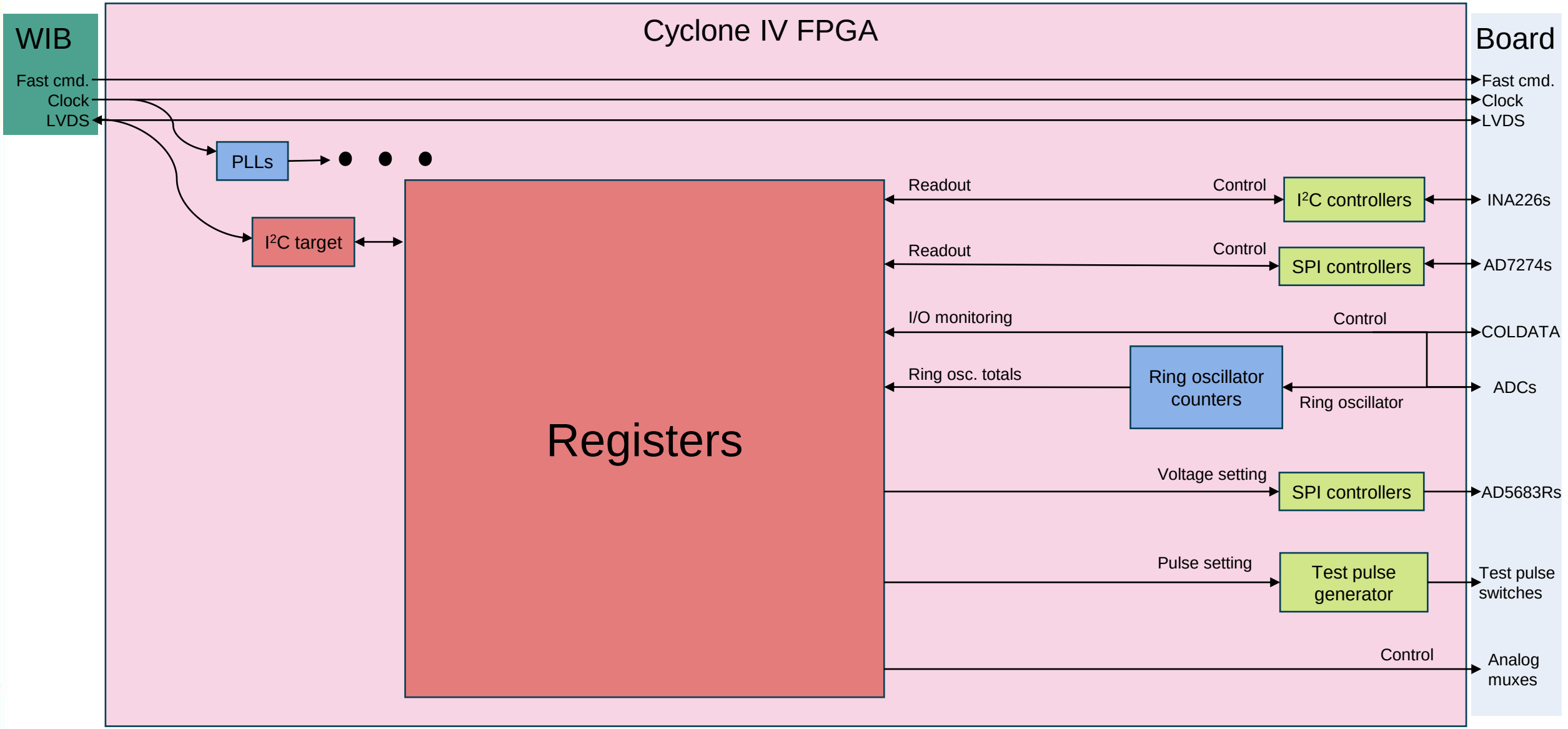


Interface to WIB

- WIB to DAT FPGA
  - System clock
  - Fast command
  - I^2C
    - DAT FPGA I^2C address: 0xC
    - 61 DAT FPGA registers
- COLDATA to WIB
  - 4 high speed data links



Block diagram of the DAT FPGA's firmware

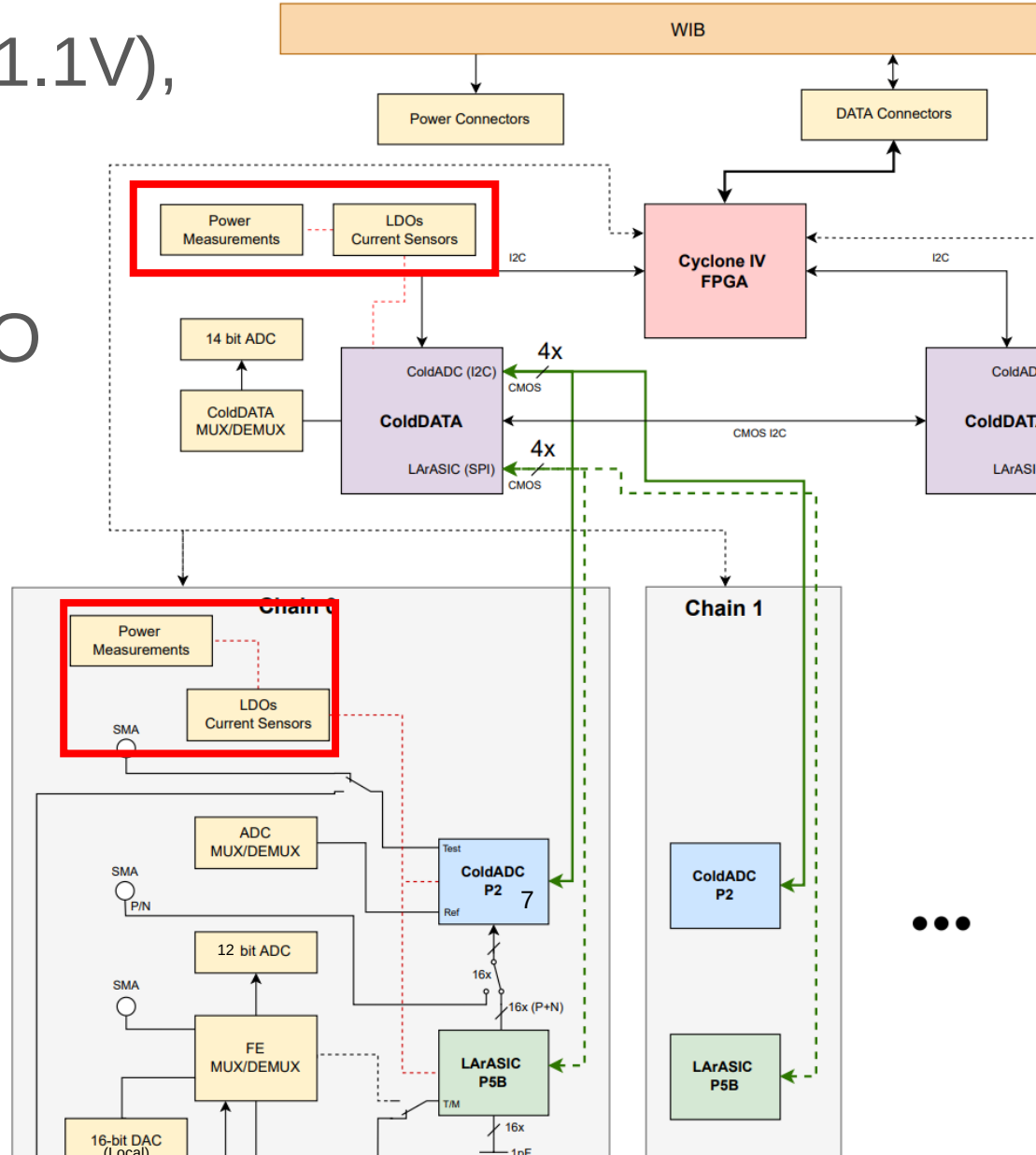


Monitoring: INA226 Power Monitors (I^2C)

COLDATA: VDDA, VDDCORE, VDDD (1.1V), VDDIO (2.25V), VDD_LArASIC (1.8V)

LArASIC: VDD, VDDO, VDDP (1.8V)

ColdADC: VDDA2P5, VDDD2P5, VDDIO (2.25V), VDDD1P2 (1.1V)



Power Measurement

Power Rail	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA
	COLDATA#1								COLDATA#2							
VDDA	1.193	9.3							1.193	9.1						
VDD_LArASIC	1.786	0.0							1.783	0.0						
VDDCORE	1.089	9.2							1.088	9.2						
VDDD	1.089	19.5							1.086	19.5						
VDDIO	2.234	66.9							2.228	67.6						
	ColdADC #1		ColdADC #2		ColdADC #3		ColdADC #4		ColdADC #5		ColdADC #6		ColdADC #7		ColdADC #8	
VDDA2P5	2.190	132.6	2.185	133.0	2.184	132.3	2.181	134.6	2.184	125.0	2.184	132.8	2.186	121.1	2.189	135.4
VDDD2P5	2.206	5.2	2.206	5.3	2.206	5.3	2.206	5.3	2.210	5.0	2.211	5.1	2.211	5.2	2.211	5.2
VDDIO	2.205	17.2	2.206	17.7	2.205	17.5	2.205	15.6	2.210	17.5	2.209	16.4	2.209	17.1	2.210	14.7
VDDD1P2	1.095	1.5	1.095	1.4	1.094	1.5	1.094	1.5	1.094	1.4	1.098	1.4	1.099	1.4	1.099	1.5
	LArASIC #1		LArASIC #2		LArASIC #3		LArASIC #4		LArASIC #5		LArASIC #6		LArASIC #7		LArASIC #8	
VDDA	1.778	21.5	1.778	21.4	1.776	21.7	1.776	20.5	1.771	21.4	1.771	21.5	1.773	21.4	1.771	21.5
VDDO	1.781	0.0	1.780	0.0	1.780	0.0	1.781	0.0	1.776	0.0	1.776	0.0	1.776	655.3	1.775	0.0
VDDP	1.776	32.5	1.775	32.6	1.775	32.4	1.774	32.2	1.769	32.2	1.770	32.3	1.769	32.3	1.771	32.4

- All 66 ASIC power rails are measured independently by 66 INA226 chips
  - Each COLDATA: 5 power rails
  - Each ColdADC: 4 power rails
  - Each LArASIC: 3 power rails

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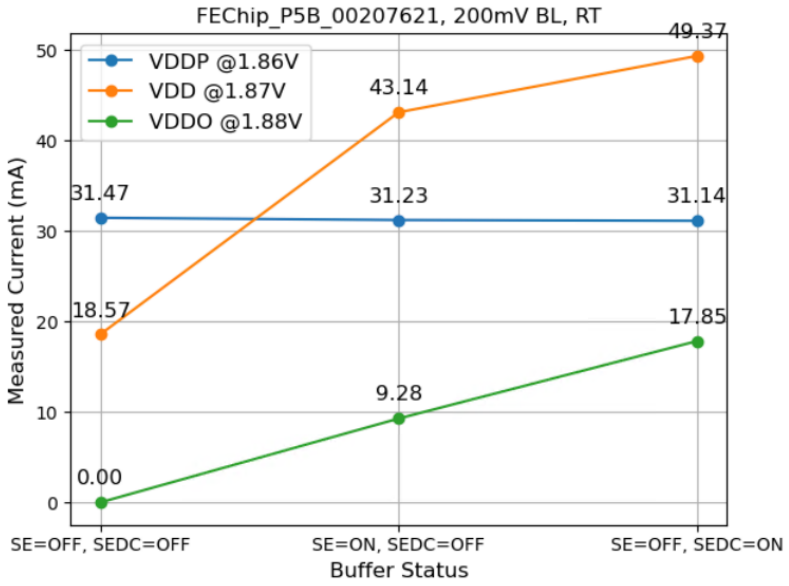
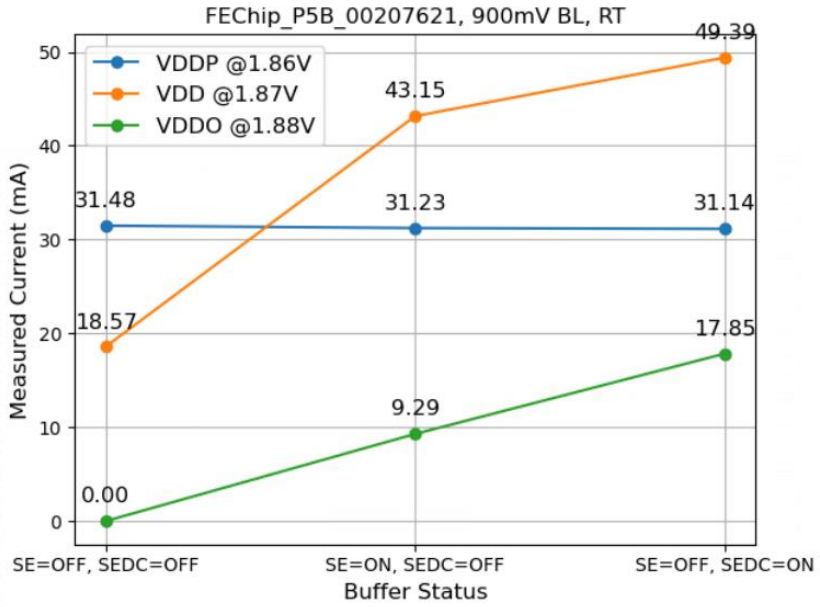
LArASIC power measurement scheme during QC

- 7 configurations
  - Power On (default)
  - Single-ended buffer enable/disable
  - Single-ended to differential buffer enable/disable
  - 200mV/900mV baseline





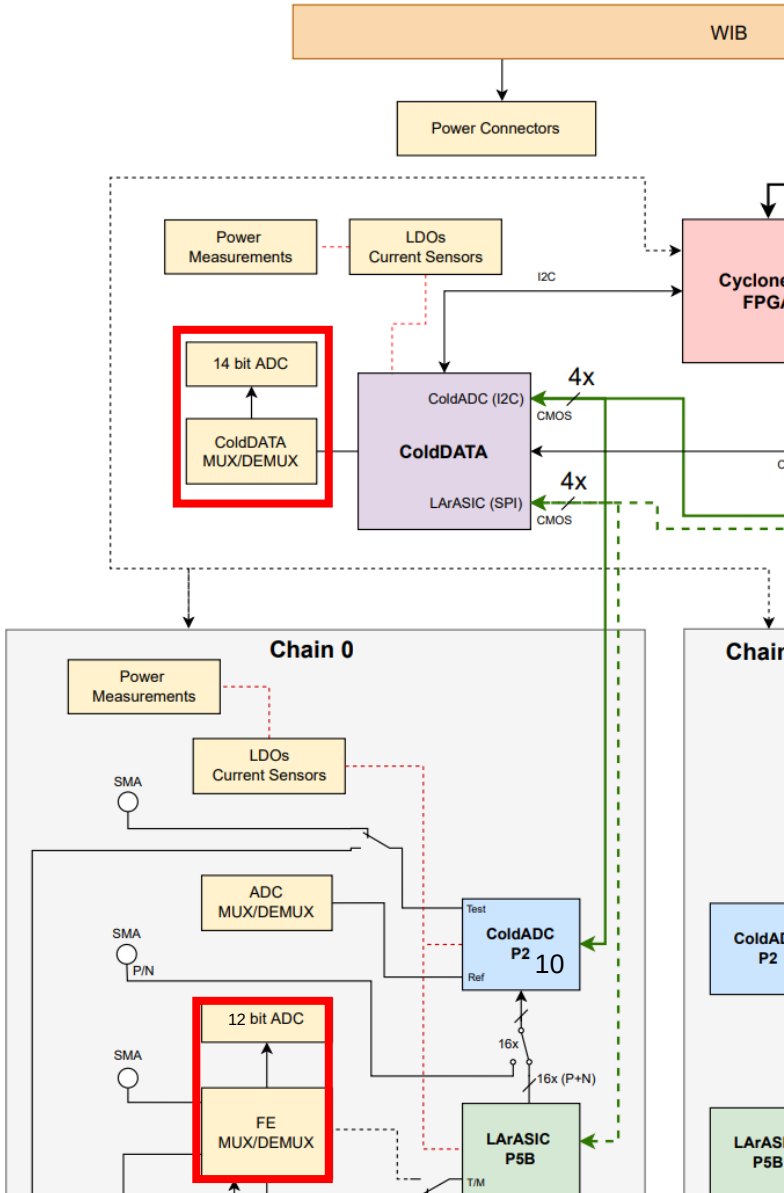
Monitoring: AD5683R MonADCs (SPI)

COLDATA: VCEXT, VDDIO, VDDCORE, VDDD, ATO, LOCK

LArASIC: VBGR (1.18V), test pulse sources

ColdADC: VOLTAGE_MONITOR, CURRENT_MONITOR, AUX_VOLTAGE, VREFP, VREFN, VCMI, VCMO, AUX_ISINK, AUX_ISOURCE, test pulse sources

```
FEMB0 is configurated
measure LArASIC 200mV BL through Monitoring pin
900mV, FE 1 CHN 0  MonADC DNI[To_AmpADC] : 0.9508583984375 V     0x5ef   010111101111
900mV, FE 1 CHN 1  MonADC DNI[To_AmpADC] : 0.947728515625 V      0x5ea   010111101010
900mV, FE 1 CHN 2  MonADC DNI[To_AmpADC] : 0.9445986328125 V     0x5e5   010111100101
900mV, FE 1 CHN 3  MonADC DNI[To_AmpADC] : 0.9521103515625 V     0x5f1   010111110001
900mV, FE 1 CHN 4  MonADC DNI[To_AmpADC] : 0.9496064453125 V     0x5ed   010111101101
900mV, FE 1 CHN 5  MonADC DNI[To_AmpADC] : 0.94397265625 V       0x5e4   010111100100
900mV, FE 1 CHN 6  MonADC DNI[To_AmpADC] : 0.9464765625 V        0x5e8   010111101000
900mV, FE 1 CHN 7  MonADC DNI[To_AmpADC] : 0.9471025390625 V     0x5e9   010111101001
900mV, FE 1 CHN 8  MonADC DNI[To_AmpADC] : 0.9464765625 V        0x5e8   010111101000
900mV, FE 1 CHN 9  MonADC DNI[To_AmpADC] : 0.9483544921875 V     0x5eb   010111101011
900mV, FE 1 CHN 10  MonADC DNI[To_AmpADC] : 0.950232421875 V     0x5ee   010111101110
900mV, FE 1 CHN 11  MonADC DNI[To_AmpADC] : 0.9433466796875 V    0x5e3   010111100011
900mV, FE 1 CHN 12  MonADC DNI[To_AmpADC] : 0.9558662109375 V    0x5f7   010111110111
900mV, FE 1 CHN 13  MonADC DNI[To_AmpADC] : 0.9408427734375 V    0x5df   010111011111
900mV, FE 1 CHN 14  MonADC DNI[To_AmpADC] : 0.9508583984375 V    0x5ef   010111101111
900mV, FE 1 CHN 15  MonADC DNI[To_AmpADC] : 0.94898046875 V      0x5ec   010111101100
200mV, FE 1 CHN 0  MonADC DNI[To_AmpADC] : 0.26666601562500003 V         0x1aa   000110101010
200mV, FE 1 CHN 1  MonADC DNI[To_AmpADC] : 0.26791796875 V       0x1ac   000110101100
200mV, FE 1 CHN 2  MonADC DNI[To_AmpADC] : 0.26666601562500003 V         0x1aa   000110101010
```



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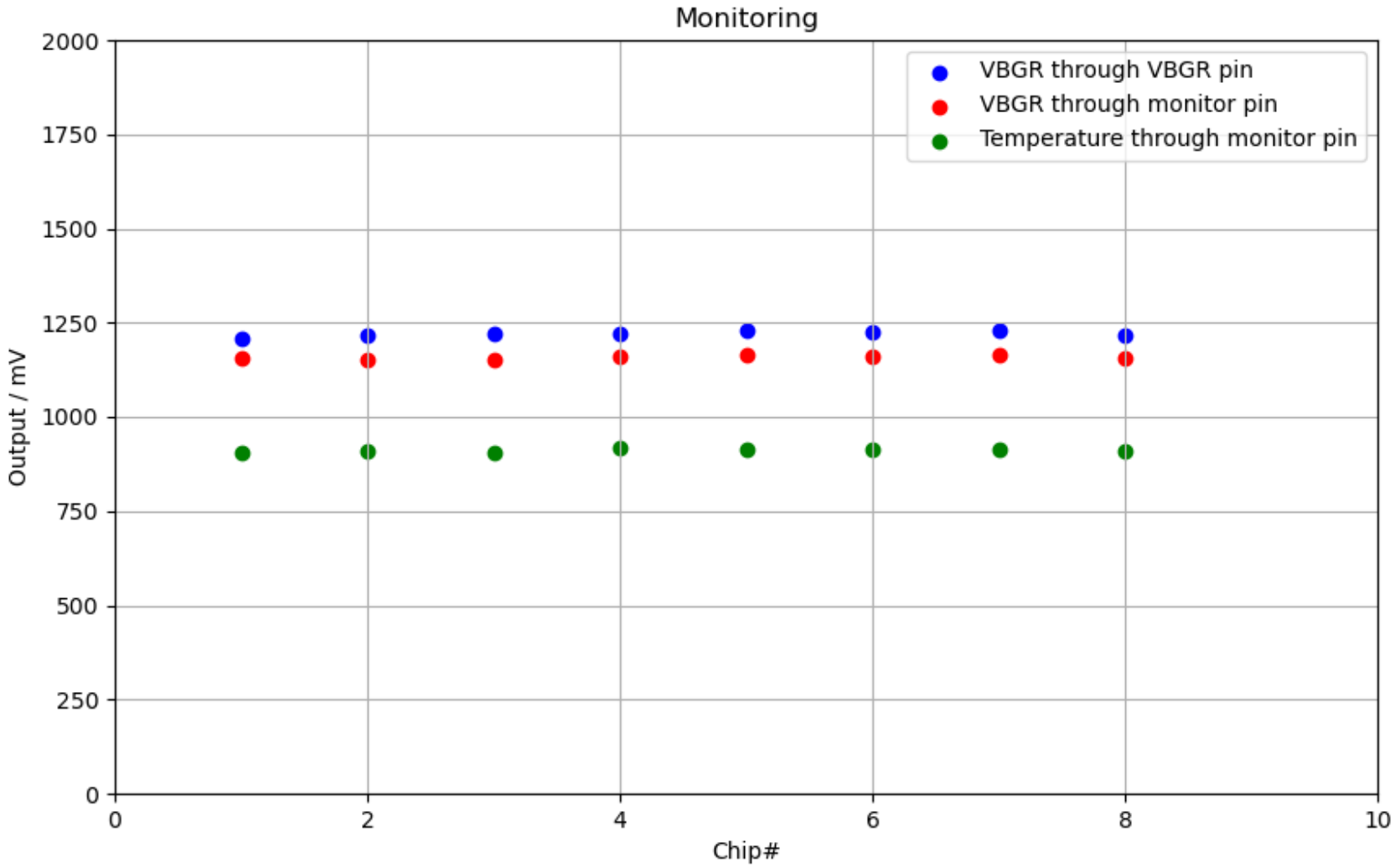
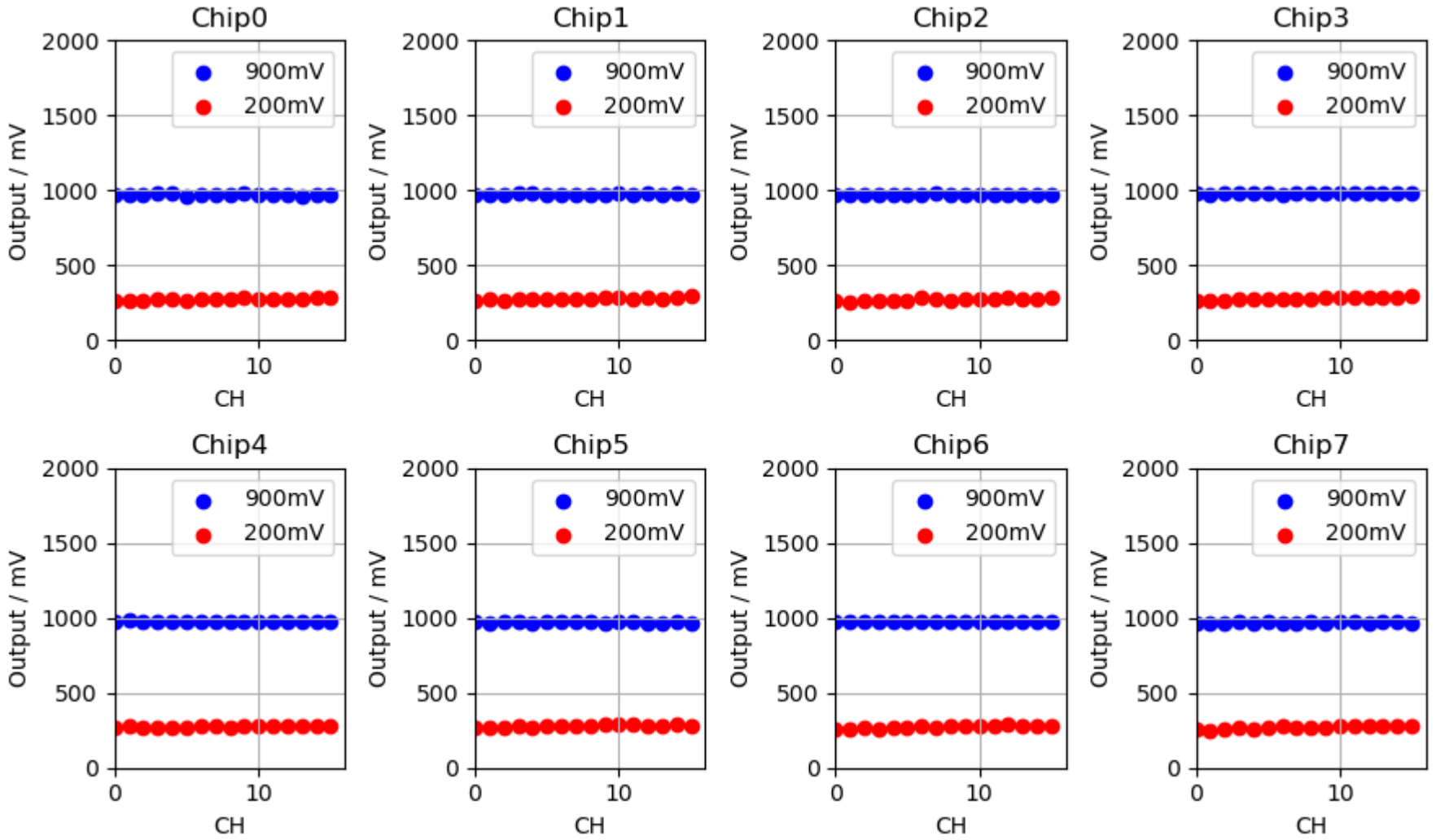
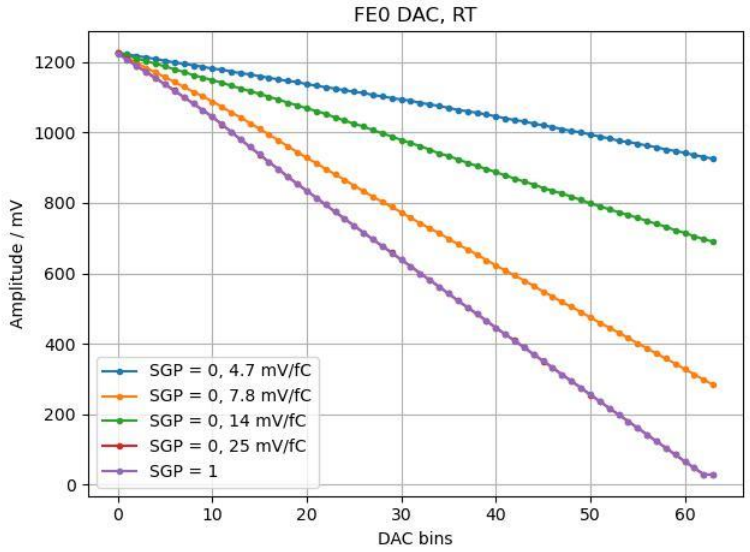
Monitoring (FE Bandgap Reference & Temperature)

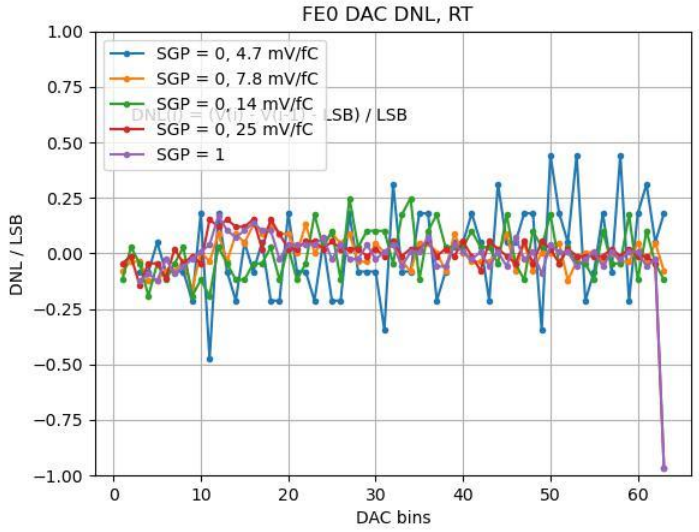


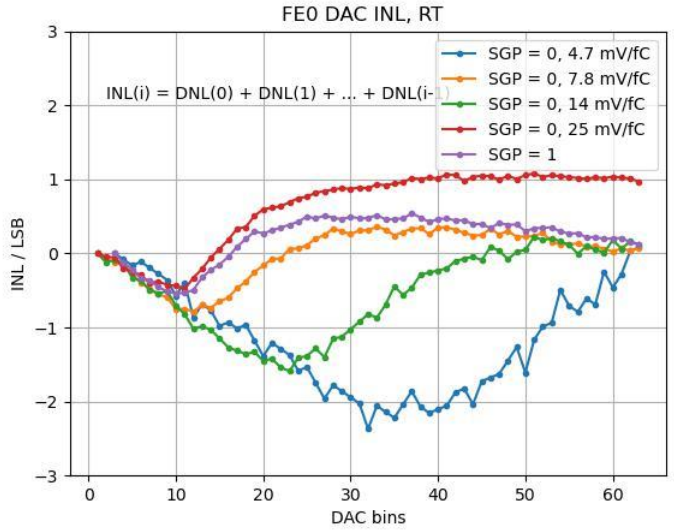
Monitoring (FE Baseline through monitoring pin)



Monitoring (FE 6-bit DAC)



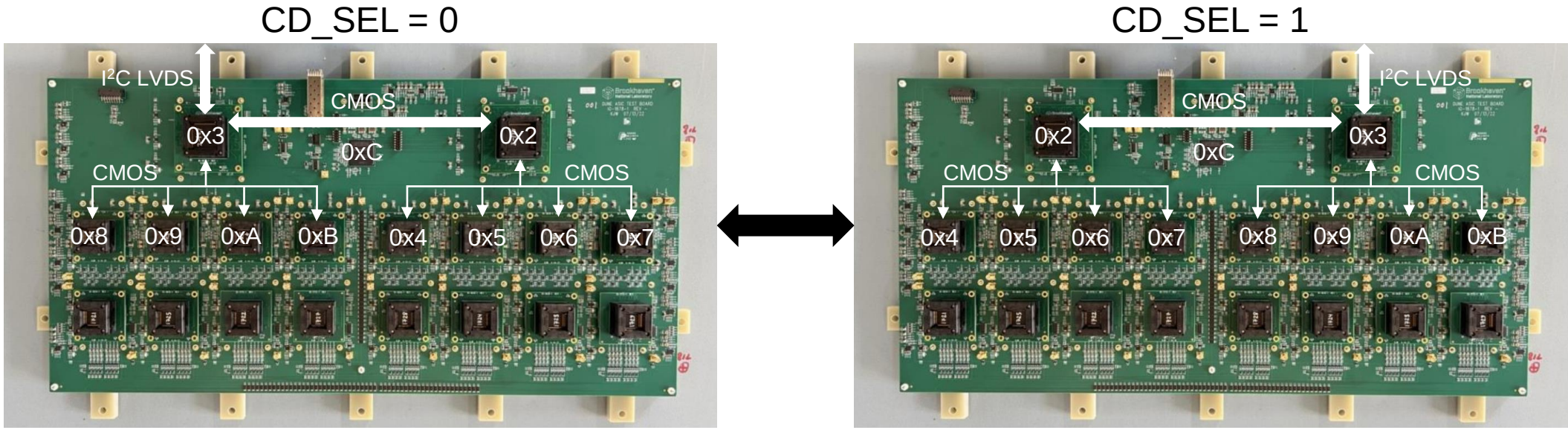




- Each LArASIC 6-bit DAC will be measured independently
  - DAC measurement needs to be optimized, INL/DNL is worse than LArASIC characterization we did before (INL < 1 LSB).

Control

- We need to test *both* COLDATA's LVDS and CMOS I²C links
- Toggling the CD_SEL bit in register 1 swaps the COLDATA's roles as well as all chips' I²C addresses
- Allows us to test all COLDATA & ColdADC address IO pins



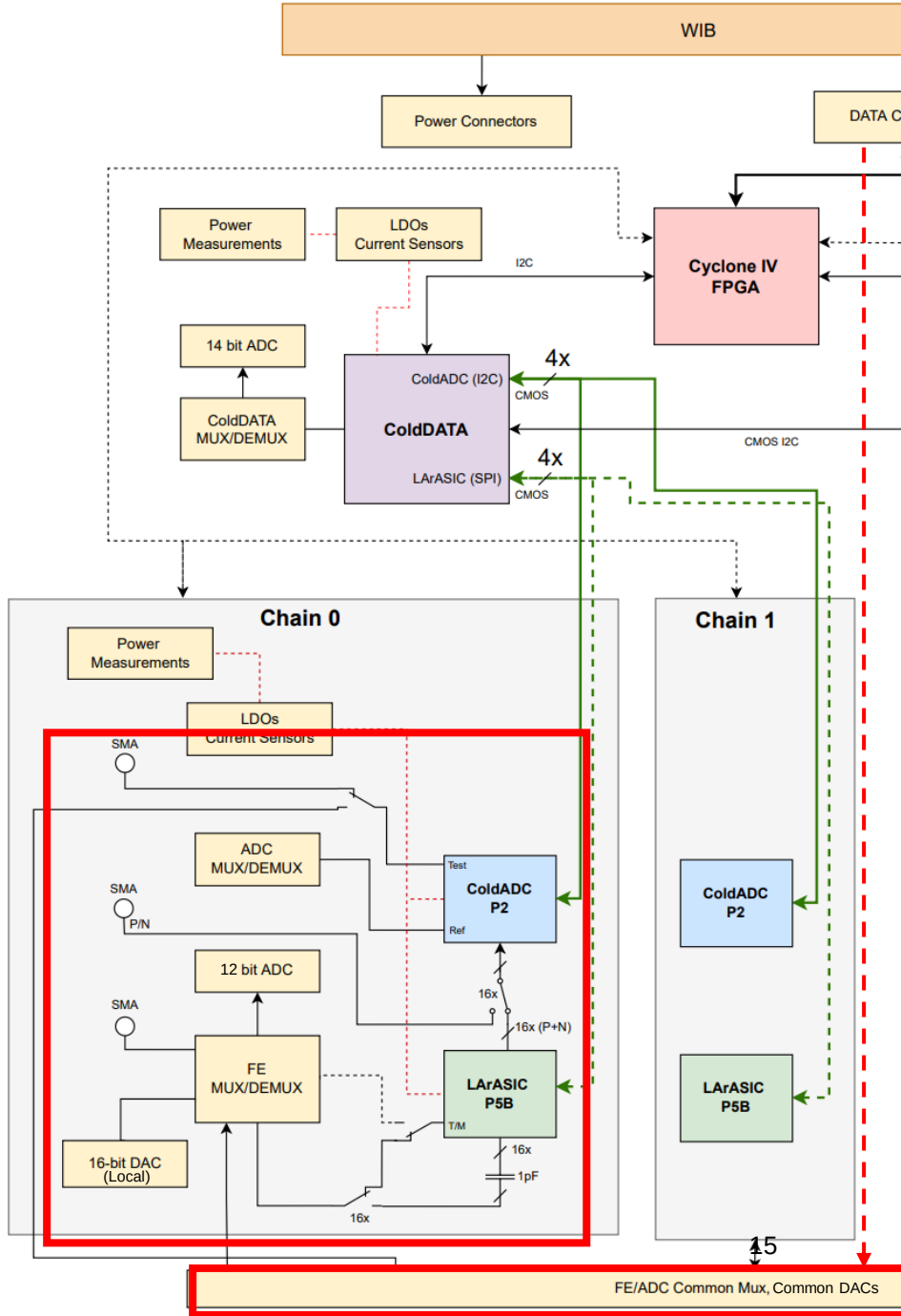
Test pulse injection

LArASIC

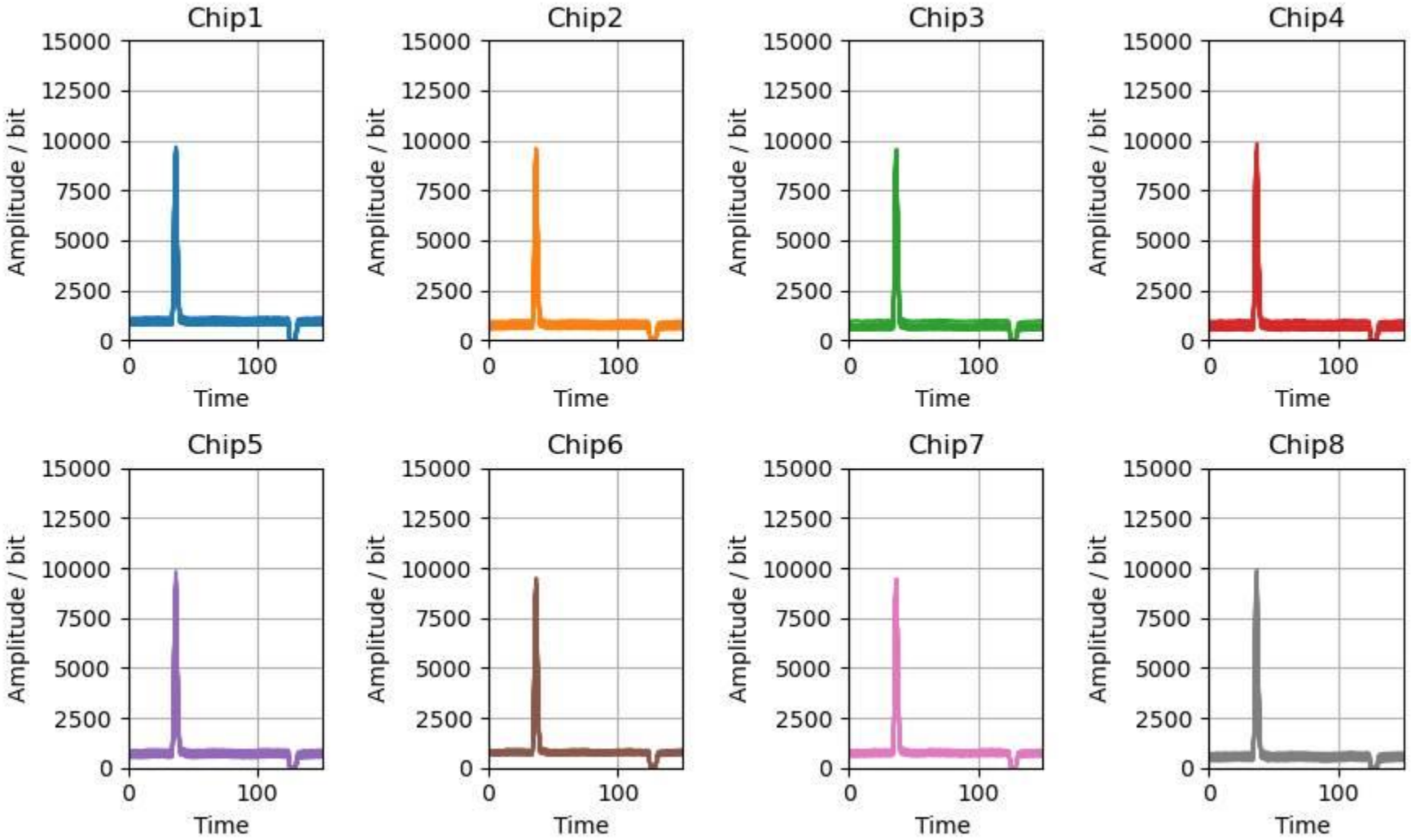
- 6-bit Internal DAC
- 16-bit Local DAC (DAT only)
- 16-bit Common DAC (DAT only)
- 16-bit WIB DAC
- Local & common SMA injection (DAT only)
- Injection from WIB via LEMO
- Front end input injection (DAT only)
  - Channel specific

ColdADC (all DAT only)

- 16-bit Common DAC
- 16-bit WIB DAC
- Local & common SMA injection
- Injection from WIB via LEMO



DAT 16-bit DAC frontend injected pulse



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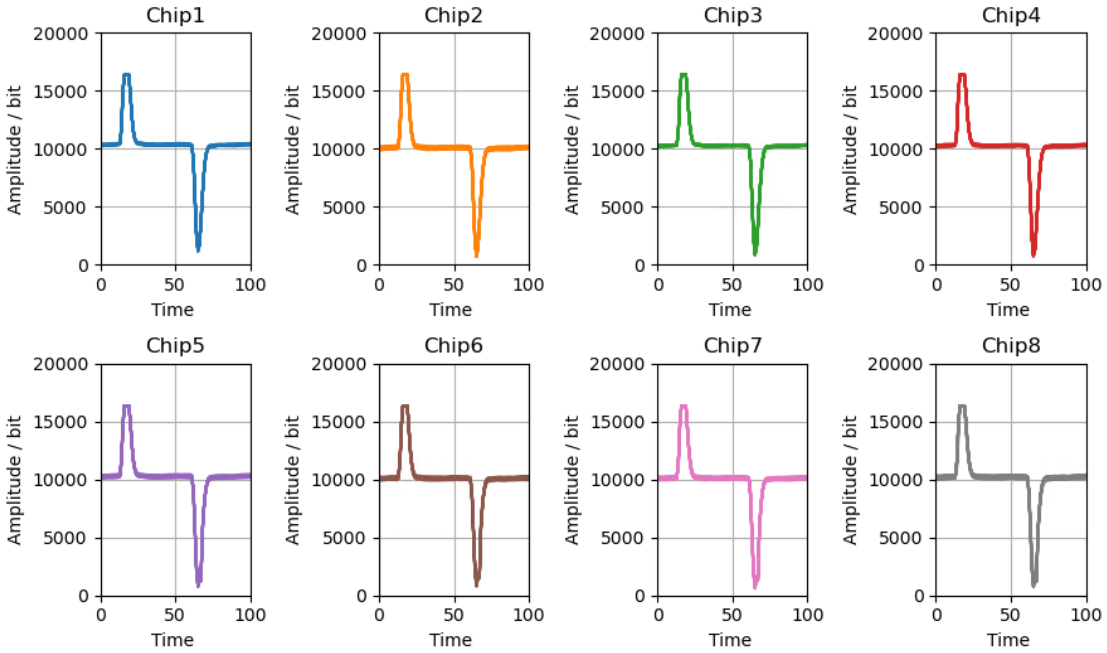
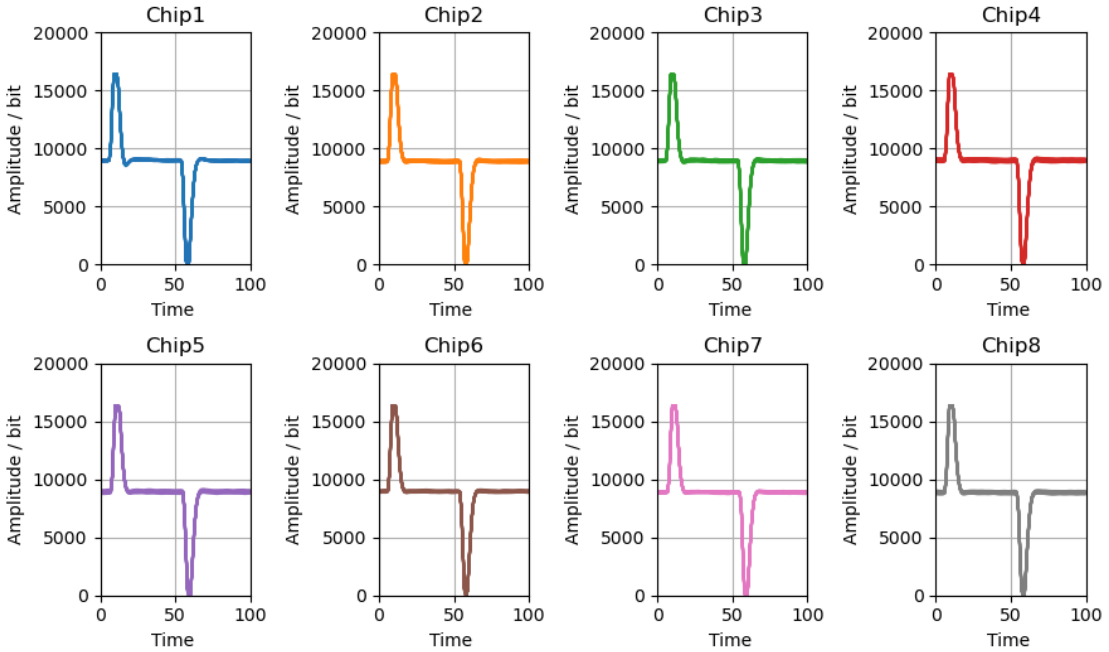
Pulse Response through 6-bit LArASIC DAC



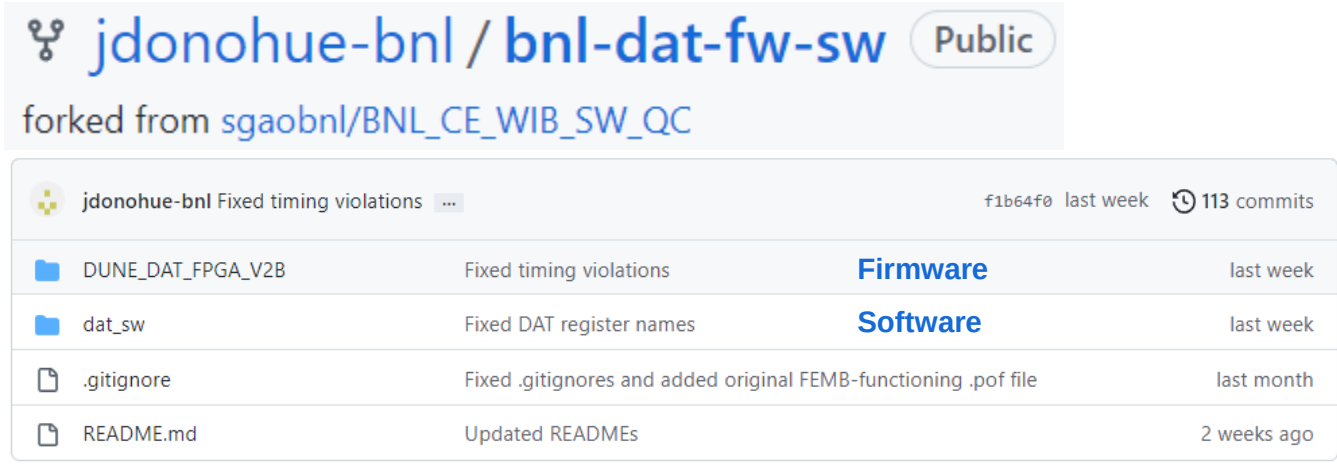
Single-ended Interface Between LArASIC & ColdADC



Differential Interface Between LArASIC & ColdADC

Software toolset

- Built as superset of WIB QC software
- Hosted on Github in folder alongside corresponding firmware & documentation
- Current software functions:
  - R/W of DAT registers (cdpeek/cdpoke with address 0xC)
  - INA226 communication & readout
  - AD7274 readout
  - Setting the DACs
  - Creating FPGA-generated pulse




```
void datpower_poke(uint8_t dev_addr, uint8_t reg_addr, uint16_t data, uint8_t cd, uint8_t fe);
uint16_t datpower_peek(uint8_t dev_addr, uint8_t reg_addr, uint8_t cd, uint8_t fe);

double datpower_getvoltage(uint8_t addr, uint8_t cd, uint8_t fe);
double datpower_getcurrent(uint8_t addr, uint8_t cd, uint8_t fe);

void dat_monadc_trigger();
bool dat_monadc_busy(uint8_t cd, uint8_t adc, uint8_t fe);
uint16_t dat_monadc_getdata(uint8_t cd, uint8_t adc, uint8_t fe);

void dat_set_dac(float val, uint8_t fe, uint8_t adc, uint8_t fe_cal);
void dat_set_pulse(uint8_t en, uint16_t period, uint16_t width, float amplitude);
```

```
dat_set_pulse(0xff, 0x2e4, 0x50, 1.0)
```

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Development Summary

- DAT future hardware revision
  - COLDATA EFUSE programming capability
  - Correcting minor FPGA I/O assignments
- DAT firmware is basically complete
  - Will need to be adjusted for DAT board revisions and possibly for particular use cases, but overall operation will not change
- Documentation is under development (docs/README.md)
- Test script LArASIC QC procedure based on DAT is under development
- Evaluation of DAT board for COLDATA & ColdADC QC will start soon
- DAT cold test is to be scheduled
  - Mini cold box is under safety review

Extra slides

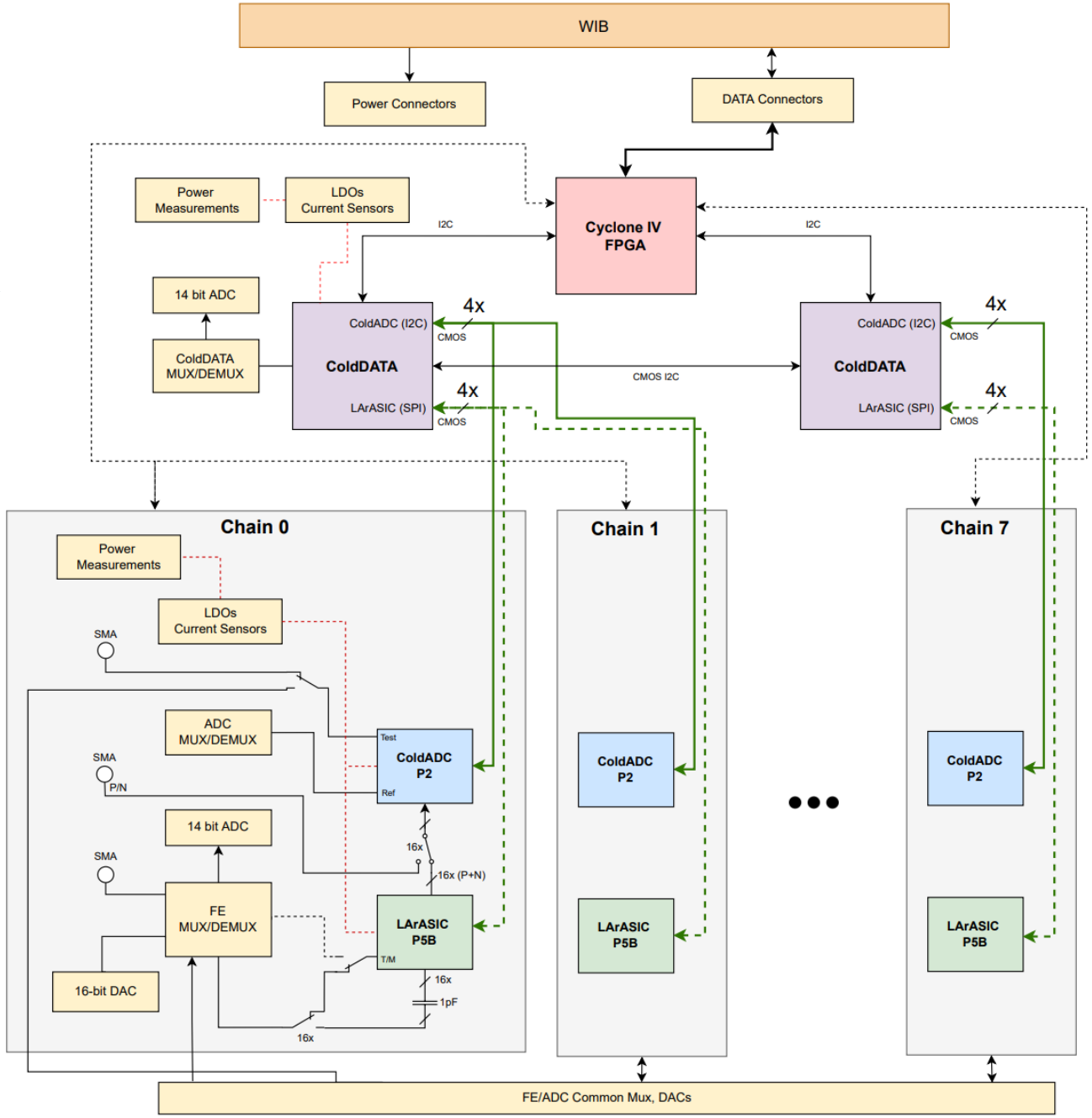
DAT Board

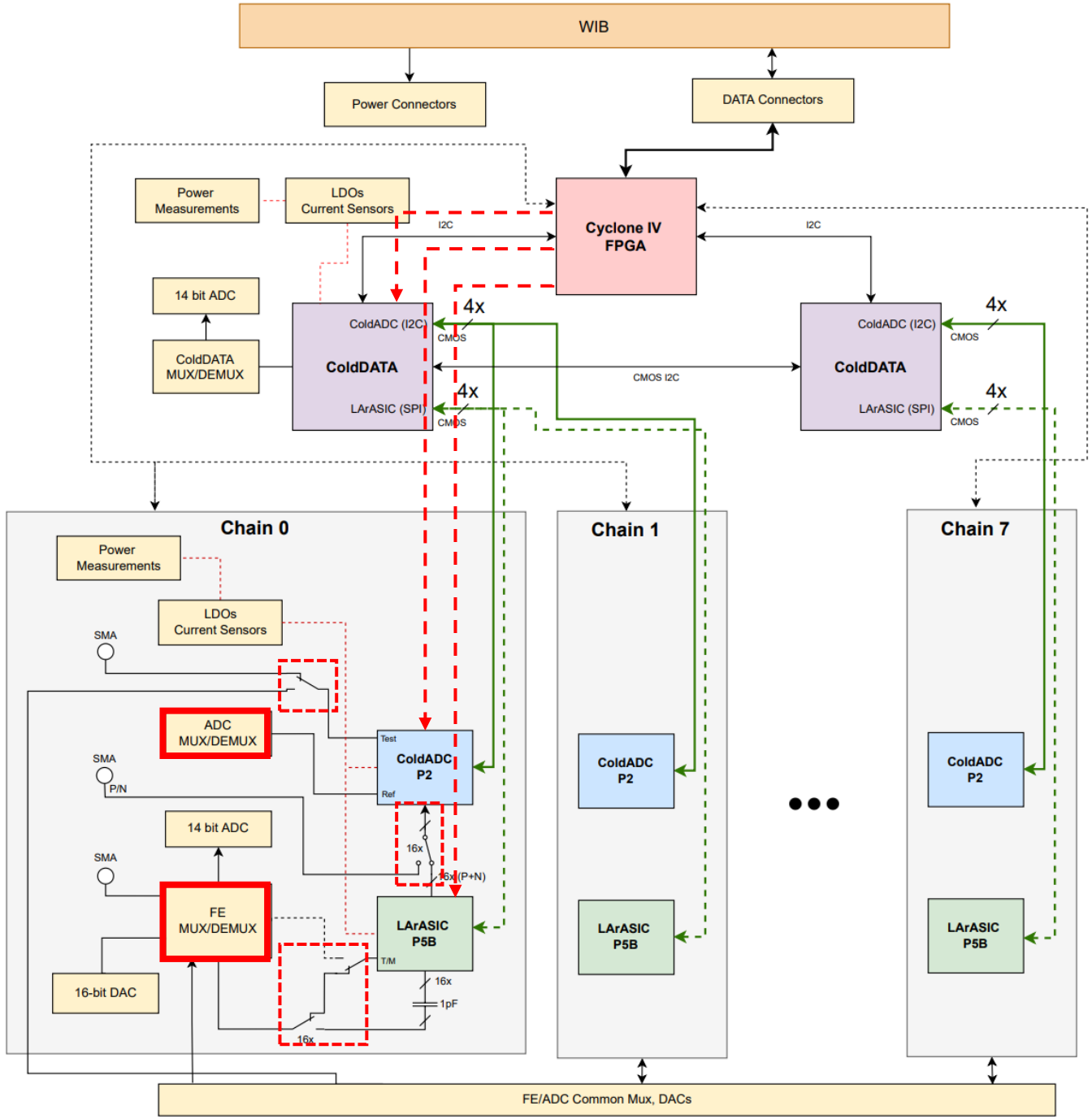
DUNE ASIC Test (DAT) Board

- Unified ASIC test board for LArASIC, ColdADC, and COLDATA QC
- Compatible power and data interface with WIB. It acts as exactly as a FEMB to WIB
- Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU new RTS
- Aim for DUNE-FD1 & FD2 ASIC QC carried out in several test sites

A single big board solution with ASIC socket mezzanines

- ASIC socket suffers mechanical degradation through thermal cycling
- More commercial semiconductor devices have been identified for cryogenic operation and used in DAT board, Such as Analog MUX: SN74LV4051, Power Monitoring Chip: INA226, I2C Bridge device: PCA9306, DAC: AD5675ARUZ




WIB
Power Connectors
DATA Connectors
Power Measurements
LDOs Current Sensors
I2C
Cyclone IV FPGA
I2C
14 bit ADC
ColdADC (I2C)
4x
CMOS
ColdDATA MUX/DEMUX
ColdDATA
LArASIC (SPI)
4x
CMOS
CMOS I2C
ColdADC (I2C)
4x
CMOS
ColdDATA
LArASIC (SPI)
4x
CMOS
Chain 0
Chain 1
Chain 7
Power Measurements
LDOs Current Sensors
SMA
ADC MUX/DEMUX
Test
ColdADC P2
Ref
SMA
P/N
14 bit ADC
16x
16x (P+N)
SMA
FE MUX/DEMUX
LArASIC P5B
T/M
16-bit DAC
16x
1pF
16x
ColdADC P2
LArASIC P5B
ColdADC P2
LArASIC P5B
FE/ADC Common Mux, DACs