



# QC Progress of FEMBs & WIBs for ProtoDUNE-VD at BNL

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03/14/2023



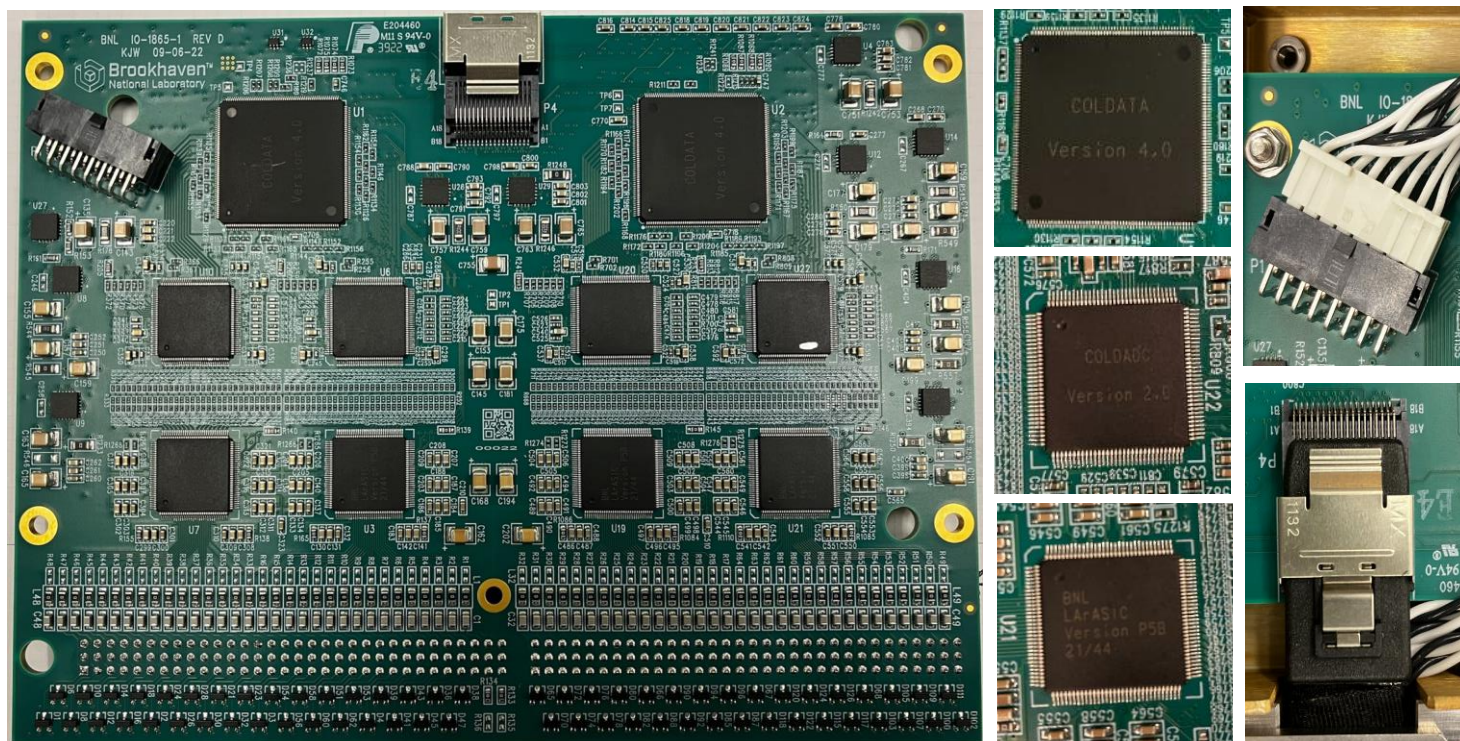
# Outline

- ❑ FEMB-VD QC test procedure
- ❑ FEMB-VD QC test results
- ❑ WIB QC test procedure
- ❑ WIB QC test results
- ❑ Cable inspection
- ❑ Next steps
- ❑ Summary

# FEMB-VD

## ➤ Perform digitized readout of 128 TPC electrodes in liquid Argon

- Joint efforts by many institutes under the coordination of DUNE TPC Electronics Consortium

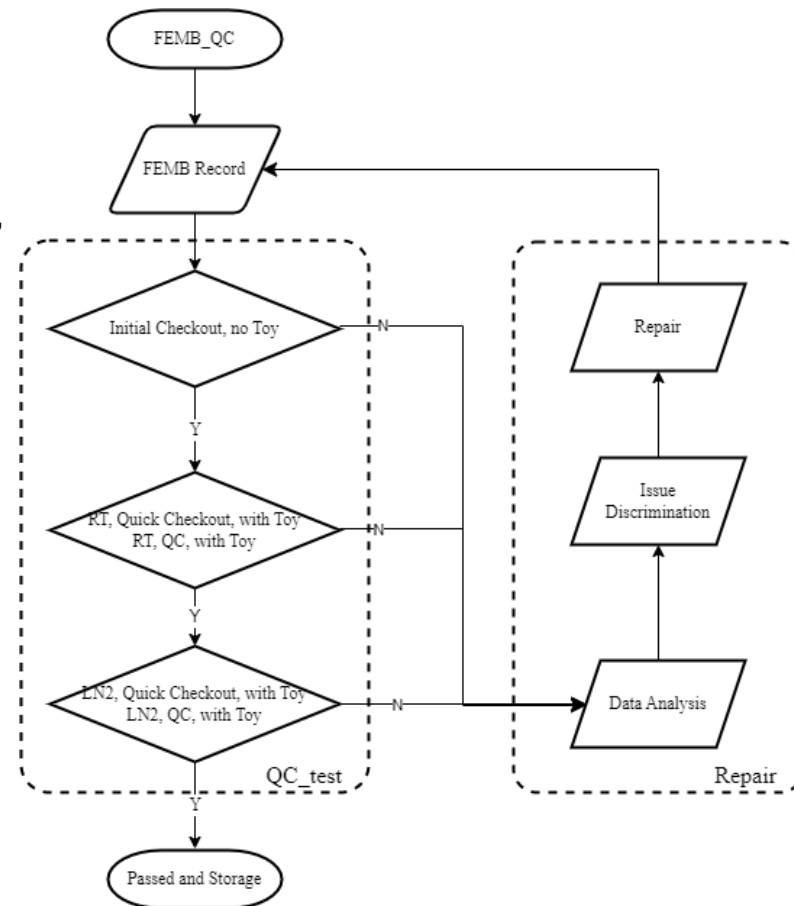


- ❑ 8x P5B LArASIC: 16-ch programmable charge-sensitive amplifier
- ❑ 8x P2 ColdADC: 16-ch 2 MS/s cryogenic ADC
- ❑ 2x P4 COLDATA: one chip corresponding to 64 readout channels

Power & Data  
connectors

# FEMB QC Items

- FEMB QC is performed after the board is enclosed in CE box
  - With external 150pF Toy TPC boards
- QC test
  - Current QC Items are a part of the final DUNE FEMB QC Items,
  - WIB V3 is used
  - **4 FEMBs** tested at RT & LN2 per test stand **per day**
    - Efficiency should be improved in future with new scripts
    - Aim to accelerate the test procedure
- Main QC Items
  - Initial checkout
  - Power consumption (RT & LN2)
  - Power cycling (LN2 only)
  - Pulse checkout
  - Noise & calibration measurement
  - Monitoring



# Issue From the Checkout & QC Test

- FEMB QC implementation
  - 60 FEMBs have been tested
  - Includes Batch#1: 20 boards, Batch#2: 40 boards
  - 7 hours per test group

Test Item	Checkout	RT_Checkout	RT_QC	LN2_Checkout	LN2_QC
Time Used	2 mins	2 mins	3 hours	2 mins	3 hours
Environment	RT	RT	RT	LN2	LN2

- Post-assembly checkout
  - 7 FEMBs did not pass

Batch	FEMB	Failure Modes	Description
1	07	Assembly	U20 (ColdADC) has two pins shorted together
1	70	Assembly	FE-ADC CH02: open caused by poorly assembled 0201 resistor
1	22	Assembly	FE-ADC CH83, 84: open caused by poorly assembled 0201 resistor
2	47	Assembly	CH17 (0201 resistor is open)
2	69	COLDATA	low impedance (< 7 Ohm) was observed in U1 (COLDATA) pin 110 (VDD_LArASIC)
2	80	COLDATA	Low impedance (short) observed between power pins to ground pins
2	25	To be debugged	Random configuration error is observed

- Initial QC results shown in the table below
  - 6 FEMBs failed
  - Tests performed in RT & LN2

Batch	FEMB	Failure Modes	Observed	Description
2	17	Assembly	RT	CH108 shows lower pulse amplitude with DIFF interface. <b>Open connection of N caused by 0201 resistor</b>
2	52	LArASIC	LN2	CH03 LArASIC is issue, CH54 shows lower leakage current at LN2
2	63	LArASIC	RT	U23 (LArASIC) shows noise slightly lower than other chips at both RT and LN2, it should be replaced for checking
1	73	ColdADC	LN2	<b>One FE-ADC chain (16 channels) shows higher noise at cold, to be retested</b>
2	68	COLDATA	RT	Abnormal data. Sensitive to temperature, can't output good data at warm
2	30	COLDATA	RT	Unstable data at warm

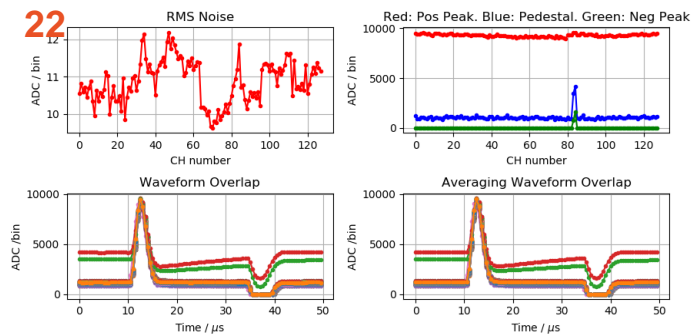
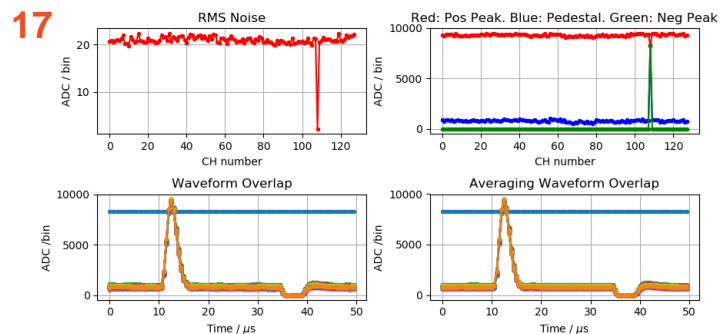
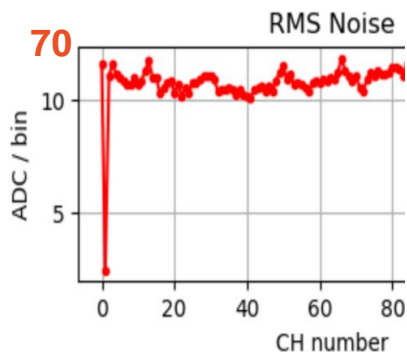
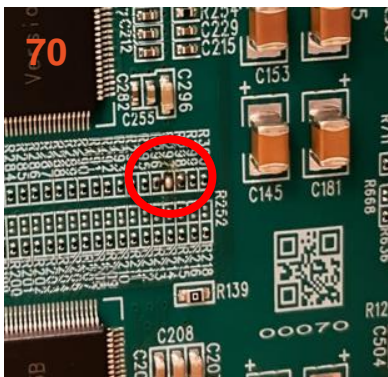
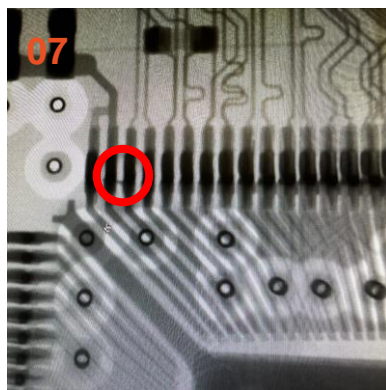
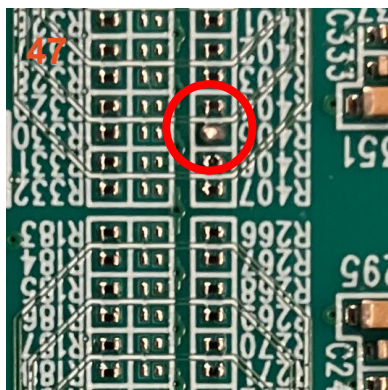


# Failure Modes – Assembly

## Observations

- #07: two pins shorted on U20 (ColdADC)
- #47 CH17: soldering issue of 0201 resistor
- #70 CH01: soldering issue of 0201 resistor
- #22 CH83 & 84: soldering issue of 0201 resistors
- #17 CH108: soldering issue of 0201 resistor

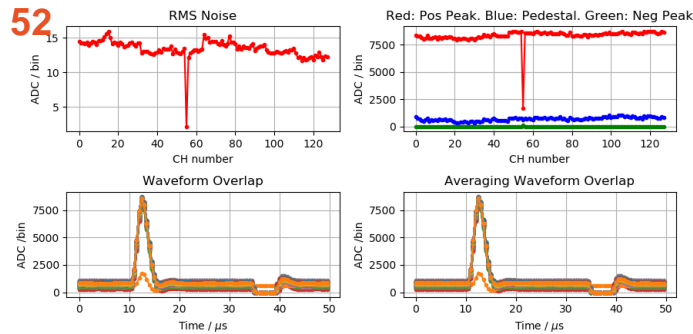
0201 resistors between FE and ADC are not needed, a FEMB revision is proposed to remove them to improve assembly quality



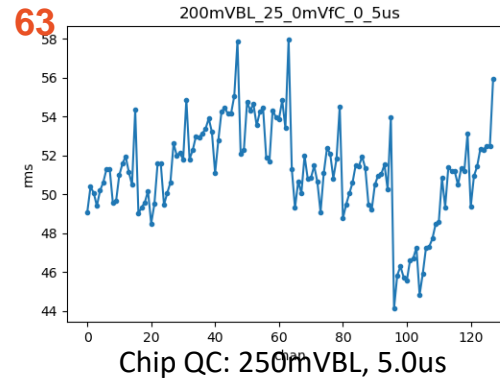
# Failure Modes – LArASIC & ColdADC

## ➤ Observations (LArASIC)

- #52: lower Pos Peak observed in the cold Leakage Current test, RT performance is normal
- #63: U23 (LArASIC) shows RMS noise and all performance slightly lower than other chips at both RT and LN2

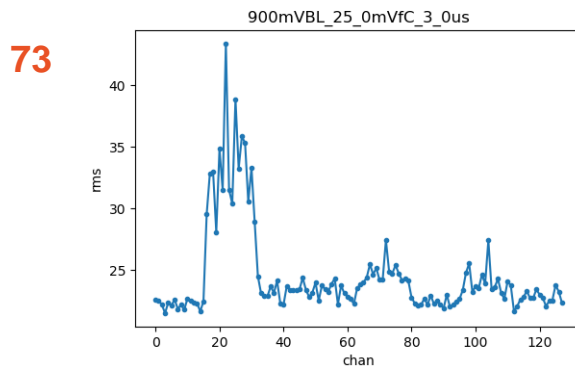


Leakage Current: 200mV 14fC 2us 0.1nA



## ➤ Observations (ColdADC)

- #73: higher RMS noise observed in the cold test, RT measurement is normal

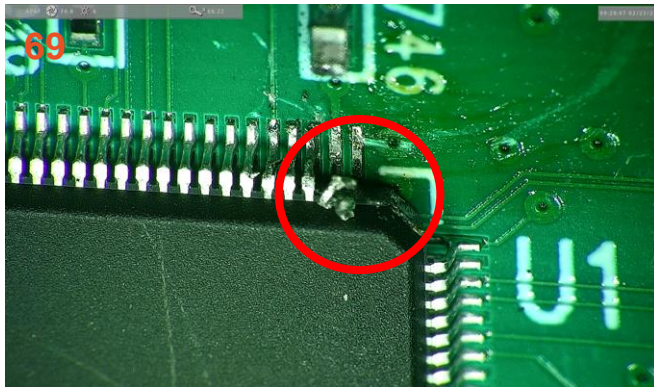


RMS: 900mV 250mVfC 3us

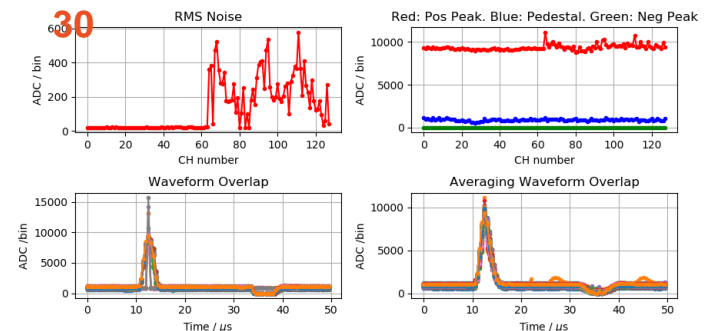
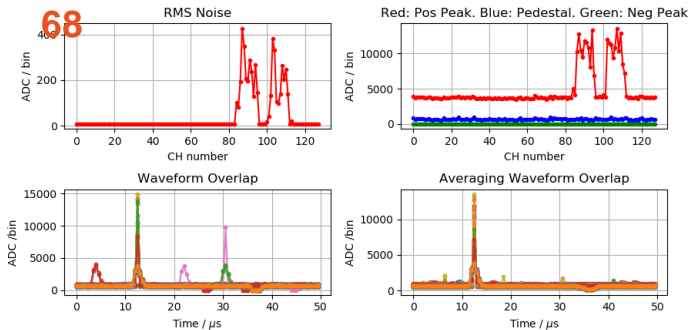
# Failure Modes – COLDDATA

## ➤ Observations

- #69: low impedance (< 7 Ohm) was observed on Pin 110 (VDD\_LArASIC) of U1 (COLDDATA)
- #80: pin VDDIO, VINT shorted, After we removed the chip from board, we figured out the short to ground, which also broken the fuse on WIB
- #68: U2 (secondary COLDDATA) is sensitive to temperature, can't output good data at warm.
- #30: COLDDATA (U2, address=0x02) (CONFIG\_PLL\_BAND. Register 65 (0x41) default value 0x20 can't work at RT. Set to 0x19 can work at RT occasionally.



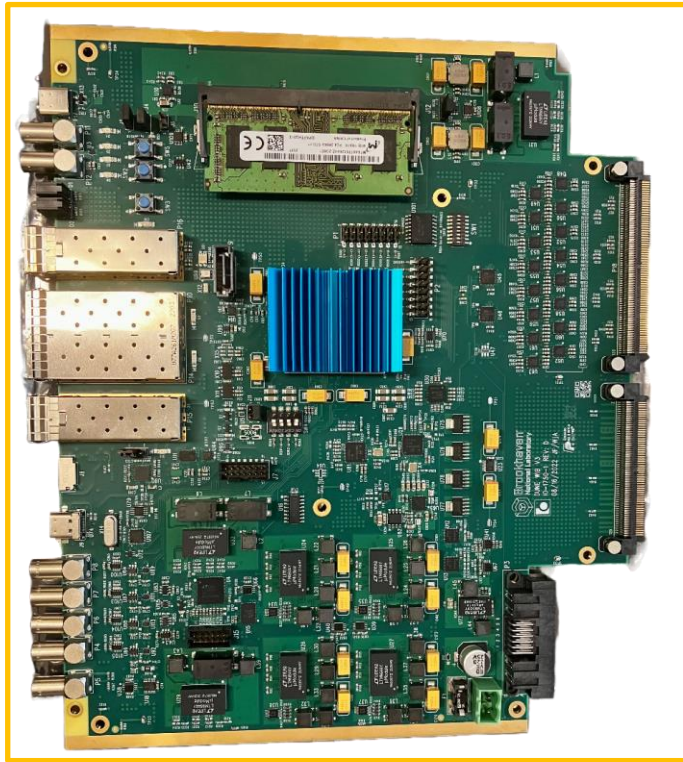
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[ 'Bias5V', 4.99976394, 0.0, 0.0 ]
[ 'PWR_FE', 2.96757032, 0.4394592000000008, 1.3041260787709466 ]
[ 'PWR_CD', 2.99778314, 0.16784900000000214, 0.5031749022658665 ]
[ 'PWR_ADC', 3.42991802, 1.6479719999999975, 5.652408859255432 ]
=====
[ 'Bias5V', 4.9988484, -0.0030517999999979395, -0.0152554855471097 ]
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# WIB Test Setup with Monolithic FEMB

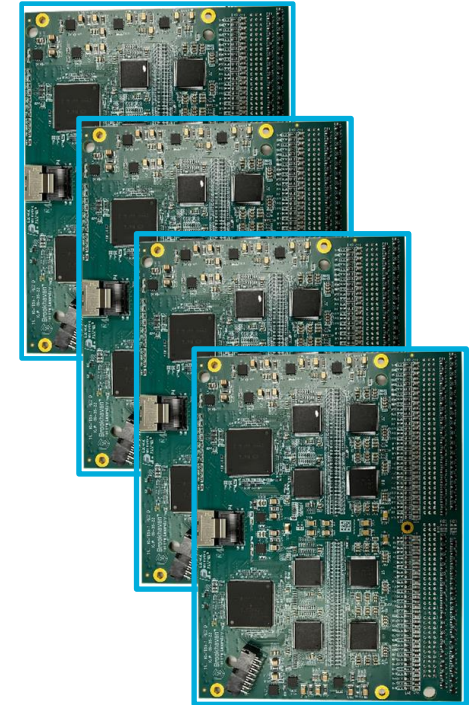
- WIB Performs Real-Time Data Acquisition of FEMB
  - Joint efforts by many institutes under the coordination of DUNE TPC Electronics Consortium



WIB



Adapter Board



FEMB-VD

- Zynq UltraScale+ MPSoC: Use the ARM core and programmable logic to acquire the data from FEMB
- 2x 10 Gb/s SFPs for high-speed data, 1x Gb/s SFP for slow control

# WIB\_V3 QC Test Procedure

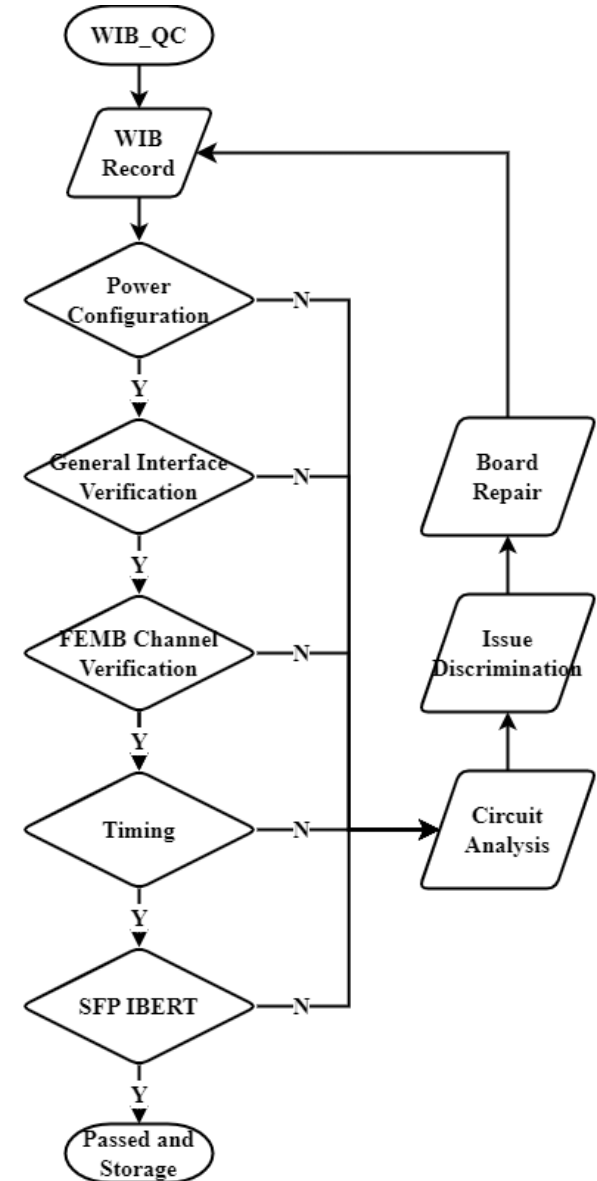
## ➤ WIB QC Test Procedure

- This procedure is a subset of final DUNE WIB QC, main includes 6 parts
- WIB V3 and FEMB-VD are used, test with after installation of the front panel pulser form WIB is not available
- WIB QC was done after installation of the front panel
  - With adapter board and FEMB boards
- Test of 1 WIB takes **0.5 hour** to go through the full QC procedure
  - Efficiency should be improved in future with new scripts, which could perform the test with just a command

WIB_QC_test						
	Initial Check	Power Rail	General Interfaces	FEMB Control	Timing	SFP IBERT
Power Measurement	Initial Ports	<ul style="list-style-type: none"> <li>Disconnect the power</li> <li>Connect the LT controller</li> <li>Check Pin Value</li> </ul>	SD Boot	Overview of the whole interface	SI5344 Configuration	IBERT
			Slow Control	<ul style="list-style-type: none"> <li>1.25 Gbps SFP channel</li> <li>Uart</li> </ul>		FEMB_PWR
Power Record	Operations	<ul style="list-style-type: none"> <li>Go_Online</li> <li>PCROM</li> <li>RAM_NVM</li> </ul>	Network	<ul style="list-style-type: none"> <li>Anaconda</li> <li>Putty</li> </ul>	1.25 Gbps SFP channel	BER Analysis, 10 <sup>-13</sup>
Jumper & adjust SW4	Record and Compare Result		Uart	<ul style="list-style-type: none"> <li>Standard Port</li> <li>Bond rate: 115200</li> </ul>		Check_FEMB_Channel

# WIB\_V3 QC Procedure

- The whole WIB QC Items
  - Initialization Check
    - Insert hardware setting and perform the post-assembly checkout
  - LT Power Control
    - Activate all power chips and check the problem of power regulators
  - Ethernet (TCP, UDP), SD card & UART Interfaces
    - Verify the basic communication interfaces
    - Command and control
  - Measurement & FEMB
    - FEMB\_PWR
    - FEMB\_Mon\_Cali
    - Check FEMB communication and power measurement
  - IBERT
    - 2 SFP fibers, 10 Gb/s, BER < 10<sup>-13</sup>
  - Power Measurement
    - Power regulators
    - With interfaces, DDR4, SD card and FEMBs
  - Timing
  - Si5344 & Si5342



# WIB QC Report

- 15 WIBs have been tested and summarized as follow
  - 10 boards passed the first QC & 5 passed QC after repair
  - 15 boards can be used in experiment
    - 14 boards have been sent to CERN
    - 1 board is kept in BNL
  
- 5 WIBs failed in the 1<sup>st</sup> run of QC shown in the table below
  - 5 boards have assembly issue
  - 1 board has a defective chip of LTC2991

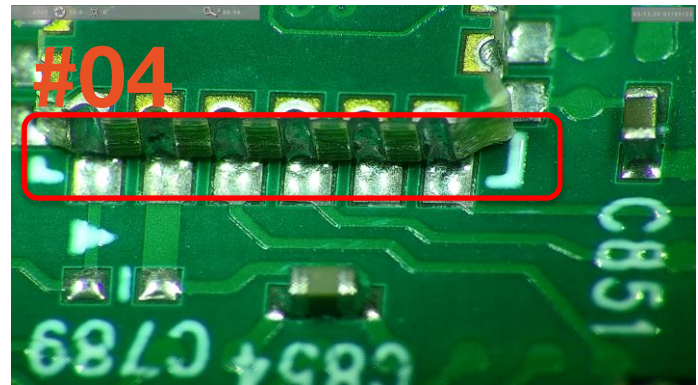
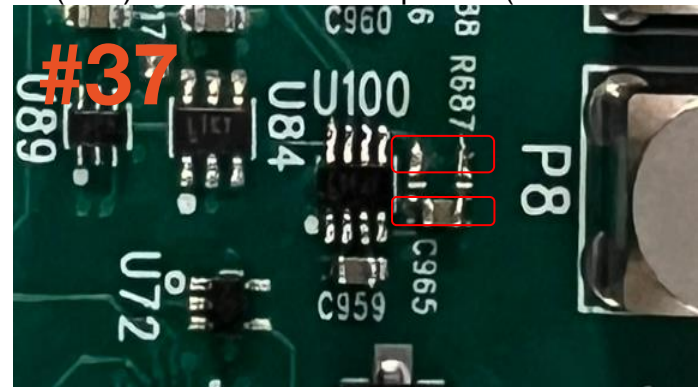
WIB SN	Failure Modes	Description
37	Assembly	LTC2314, R687 and C965 were populated in the wrong direction. U68 open soldering issue.
12	Assembly	Pins on DDR4 SODIMM socket are open, LEMO short because the throughholes
03	Assembly	C372 U96 & R005 have soldering issues (R005 is open)
10	Assembly	LTC2977 has assembly issue
04	Assembly, defective component	Assembly: SD card (FW can't be loaded), bad LTC2991 chip



# Failure Mode – Assembly & Component

## Observations

- SN 03: C372, U96 and R186 have soldering issues and Zynq+ PS can not boot
- SN 37: R687 and C965 are populated in wrong direction
- SN 12: Pins on DDR4 SODIMM socket are open & a LEMO connector is shorted
- SN 10: LTC2977 has assembly issue (not shown in picture)
- **SN 04**: Assembly issue on SD card, also, the chip LTC2991 (U36) is defective and replaced (not shown in picture)

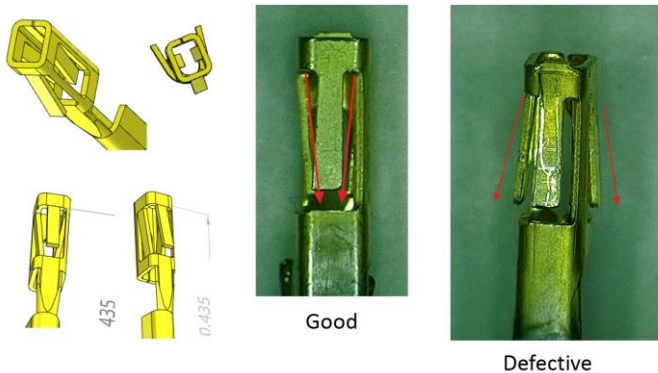




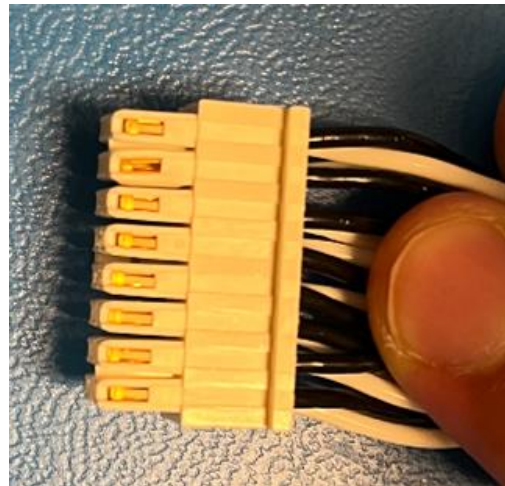
# Cold Cable Inspection

## ➤ Cold Cable Inventory

- 25m Samtec data cable, 65 pcs
- Power cable production achieves a good yield
  - 25m power cable, 65 pcs, two observed quality issues.
  - 2.5m power cable, 65pcs
- 3m miniSAS cable, 50 pcs, used for CRP5
- 2.5m miniSAS cable, 90pcs, used for CRP4
- > 16 sets (>10%) passed cryogenic screening test with CRP5A and cold test with patch panels



Batch#5 (SN0018, 25m): A loose connection was identified when we performed the daisy-chain test. It turns out there is a **defective crimp**



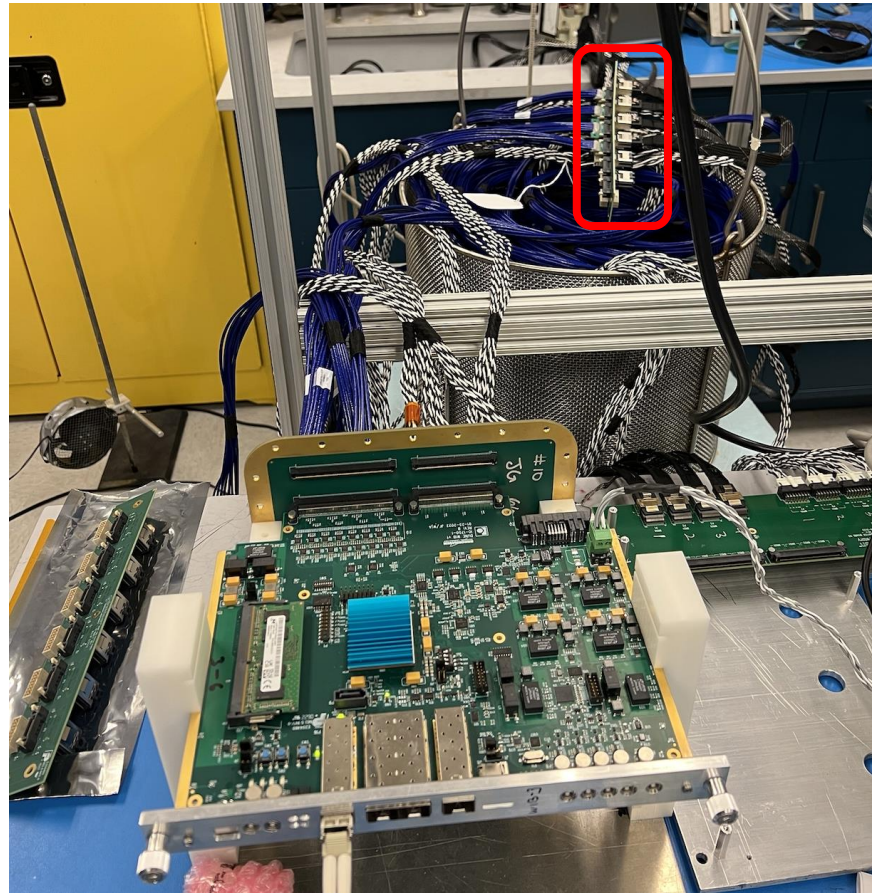
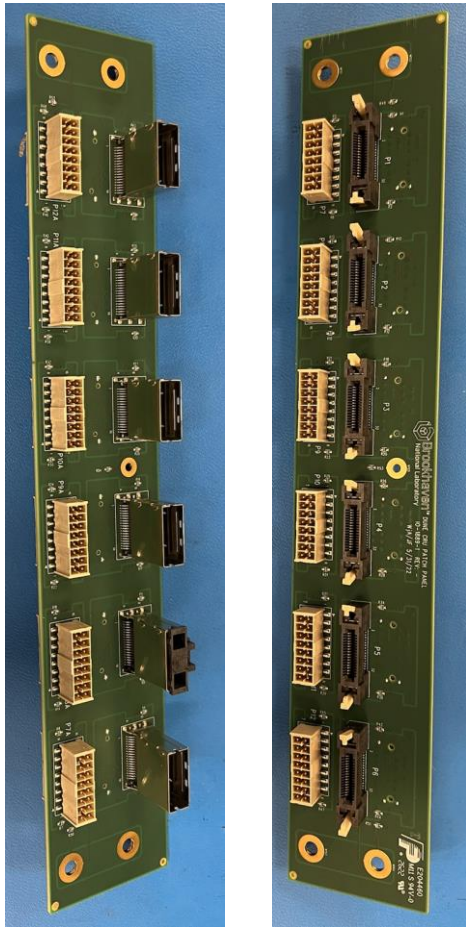
SN0020 had one crimp rotated 90 degrees



The mini-SAS cable is wrapped with black braided sleeving, and baked in the oven **@ 250 F for 3 hours** to achieve maximum solvent resistance

# Patch Cable Inspection

- 9 pcs patch panel board were assembled
  - All passed warm QC, two were selected for cold QC



WIB + Flange + 25m cables + patch panel + 2.5m cables + 4x FEMBs

# Next Steps

## ➤ FEMB

- Remove 0201 resistors in the FEMB revision
- Hanjie develops new script to reduce the QC test time
- Test the boards being repaired

## ➤ WIB

- Finalize the test procedure
- Develop the automatic test script, which will be convenient for operators
- Repair one board returned from CERN

# Summary

## ➤ FEMB QC test

- A QC procedure with scripts has been defined and implemented in the RT and LN tests
- 60 boards have been tested
- 13 boards have issues on assembly and defective chips
  - 5 FEMBs have assembly issues
  - 4 FEMBs have issues on COLDATA, which didn't go through ASIC QC test

## ➤ WIB QC test

- A QC procedure has been defined and implemented in the test
- 15 boards have been tested
- 5 boards have issues on assembly and defective chip
  - 5 WIBs have assembly issues
  - 1 WIB has a defective chip

**Thanks for listening!**