Self-trigger algorithm

Detection algorithm 64R-32R-16R, VHDL implementation and future work

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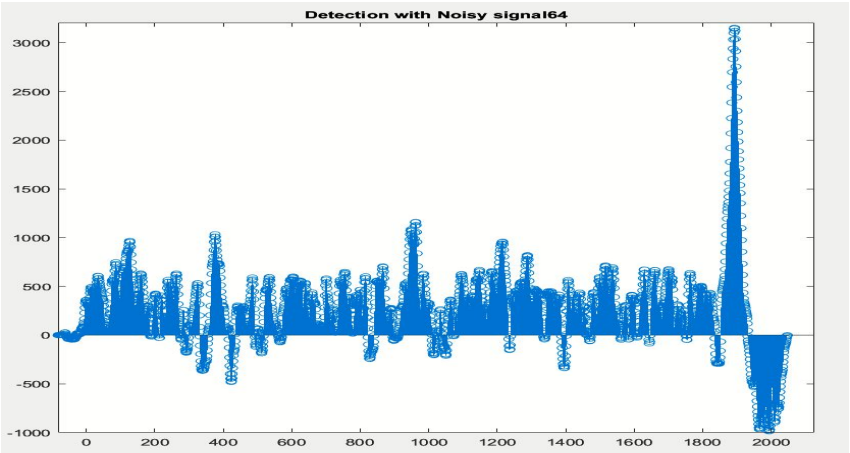
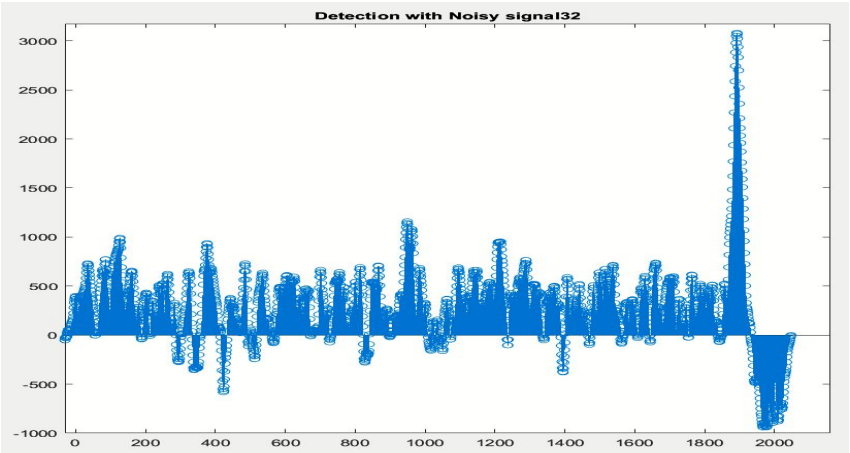
DUNE

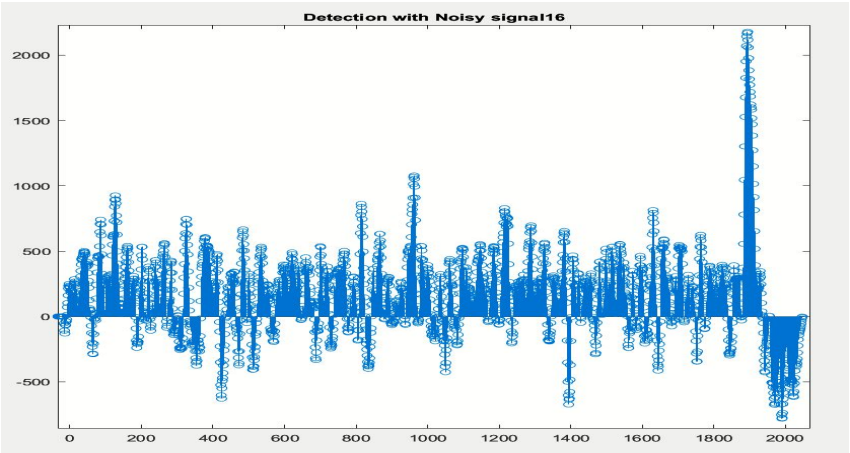
Simulation: Using a 64 register multiplication for the matching filter



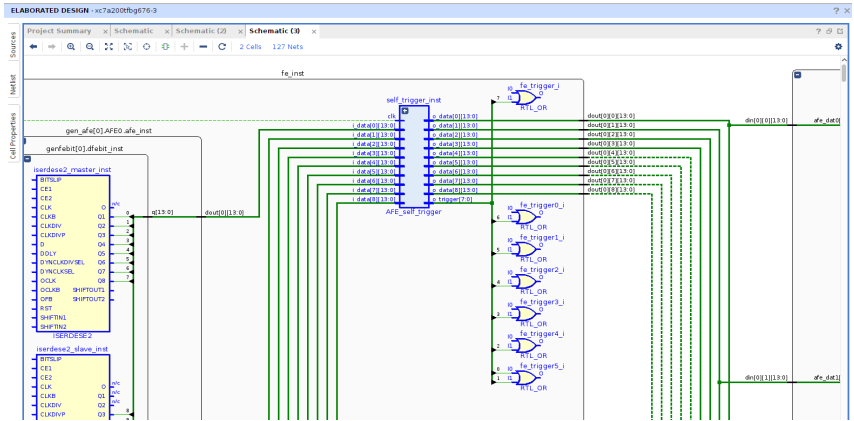
Simulation: Using a 32 register multiplication for the matching filter



Simulation: Using a 16 register multiplication for the matching filter



RTL schematic of the self-trigger integrated inside DAPHNE V2a firmware



Integration of a self-trigger algorithm for 40 channels

```
28 1. Slice Logic
29 --------------
30
31 +----------------------------+-------+-------+-----------+-------+
32 |          Site Type         |  Used | Fixed | Available | Util% |
33 +----------------------------+-------+-------+-----------+-------+
34 | Slice LUTs                 |  8718 |     0 |    133800 |  6.52 |
35 |   LUT as Logic             |  6109 |     0 |    133800 |  4.57 |
36 |   LUT as Memory            |  2609 |     0 |     46200 |  5.65 |
37 |     LUT as Distributed RAM |     0 |     0 |           |       |
38 |     LUT as Shift Register  |  2609 |     0 |           |       |
39 | Slice Registers            | 15749 |     0 |    267600 |  5.89 |
40 |   Register as Flip Flop    | 15749 |     0 |    267600 |  5.89 |
41 |   Register as Latch        |     0 |     0 |    267600 |  0.00 |
42 | F7 Muxes                   |   258 |     0 |     66900 |  0.39 |
43 | F8 Muxes                   |    45 |     0 |     33450 |  0.13 |
44 +----------------------------+-------+-------+-----------+-------+
45
```

Integration of a self-trigger algorithm using a 16 register multiplication

```
+----------------------+-------+-------+------------+--------+
|      Site Type       |  Used | Fixed | Available  | Util%  |
+----------------------+-------+-------+------------+--------+
| Block RAM Tile       | 130.5 |     0 |        365 | 35.75  |
|   RAMB36/FIFO*       |    13 |     0 |        365 |  3.56  |
|     FIFO36E1 only    |    12 |       |            |        |
|     RAMB36E1 only    |     1 |       |            |        |
|   RAMB18             |   235 |     0 |        730 | 32.19  |
|     FIFO18E1 only    |    31 |       |            |        |
|     RAMB18E1 only    |   204 |       |            |        |
+----------------------+-------+-------+------------+--------+
* Note: Each Block RAM Tile only has one FIFO logic availabl
accommodate a RAMB18E1


4. DSP
------

+-----------------+------+-------+------------+--------+
|    Site Type    | Used | Fixed | Available  | Util%  |
+-----------------+------+-------+------------+--------+
| DSPs            |  600 |     0 |        740 | 81.08  |
|   DSP48E1 only  |  600 |       |            |        |
+-----------------+------+-------+------------+--------+
```

Code available on:

`https://github.com/edgar-rincon-g/DAPHNE_V2a.git`

branch: main

Conclusions

- A self-triggger algorithm using a 16 register multiplication is as reliable, as the the algorithm that uses a 64 register multiplication for the matching filter.
- The 16 register algorithm for detection, consumes less resources from the FPGA, making possible a 40 channels implementation using 600 DSPs(multipliers).
- A self trigger algorithm for 40 channels was successfully integrated into Fermilab's/Jamieson's code.
- DAPHNE V2a firmware is ready to be tested using a 40 channels self-trigger algorithm, based on matching filters.

What is next

- Do more tests on the self-trigger algorithm, and use more data coming from CERN or Milano.
- Another approach is being coded, but not yet finished. It uses combinational logic to implement the multipliers in order to optimize the use of DSPs.
- Continue to study and improve the algorithm. Because its highly dependant on the signal mean computing, during a 320 samples window.


DEEP UNDERGROUND
NEUTRINO EXPERIMENT