Overview of Bottom Drift Electronics (BDE) System

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FD2 BDE Final Design Review
16 May 2023

BERKELEY LAB

DUNE

Thank you for taking time to serve on the FD2 BDE FDR Committee

Your assessments and recommendations are important to us

Goal For this Review

In addition to reviewing the FD2 Bottom Drift Electronics, we are requesting the Committee to approve the following items from the CD-3a (long-lead procurement) scope:

1. Procurement of Frontend Motherboard (FEMB) discrete components for FD1
2. Procurement of Warm Interface Board (WIB) discrete components for FD1
3. Procurement of three long lead items for Power & Timing Card (PTC) for FD1: power monitor chip, DC-DC converter, and Encluster FPGA mezzanine board*

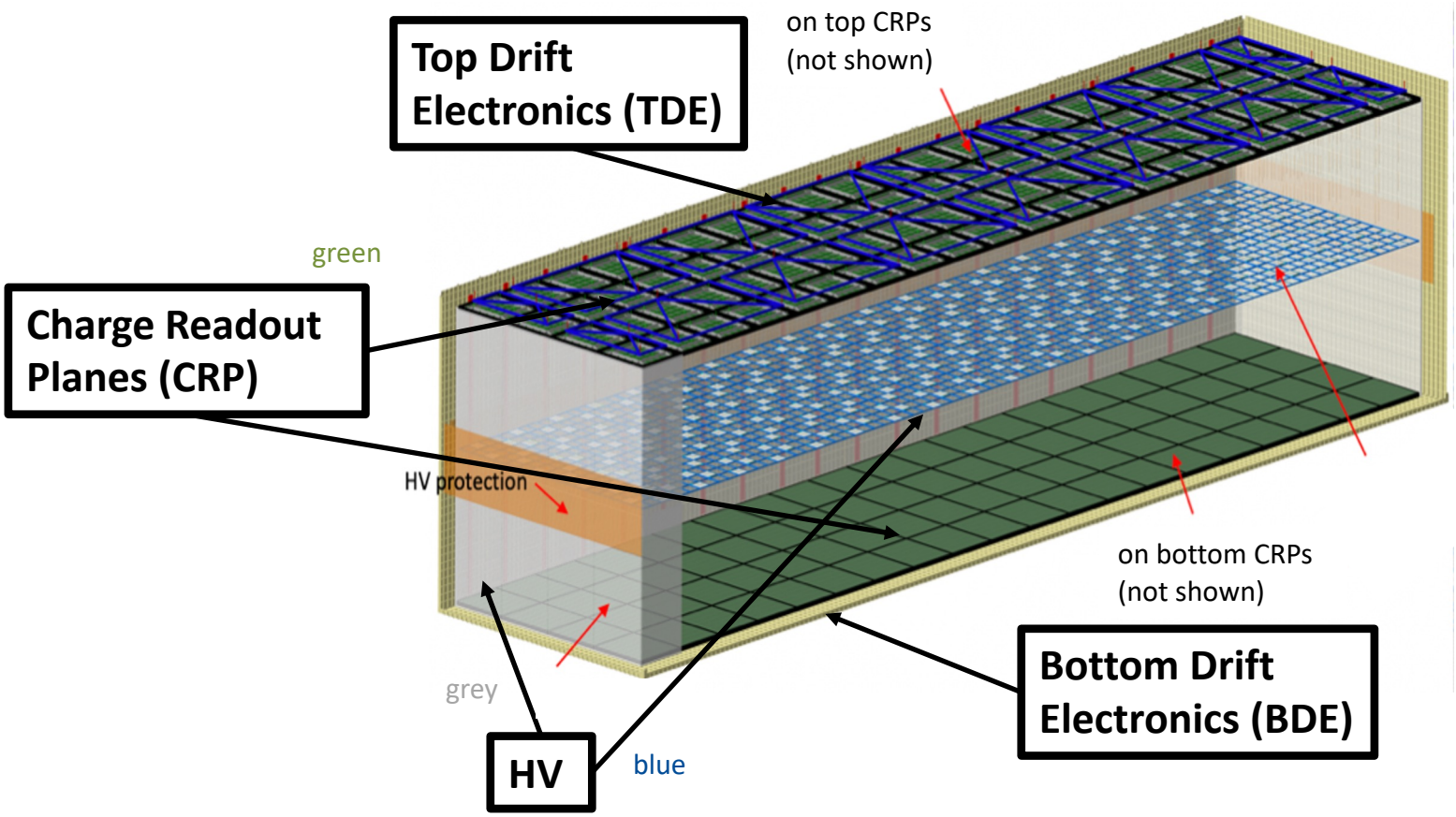
* Will first demonstrate successful integration of PTC at CERN before submitting the FPGA order

Agenda for this Review

https://indico.fnal.gov/event/58968/timetable/

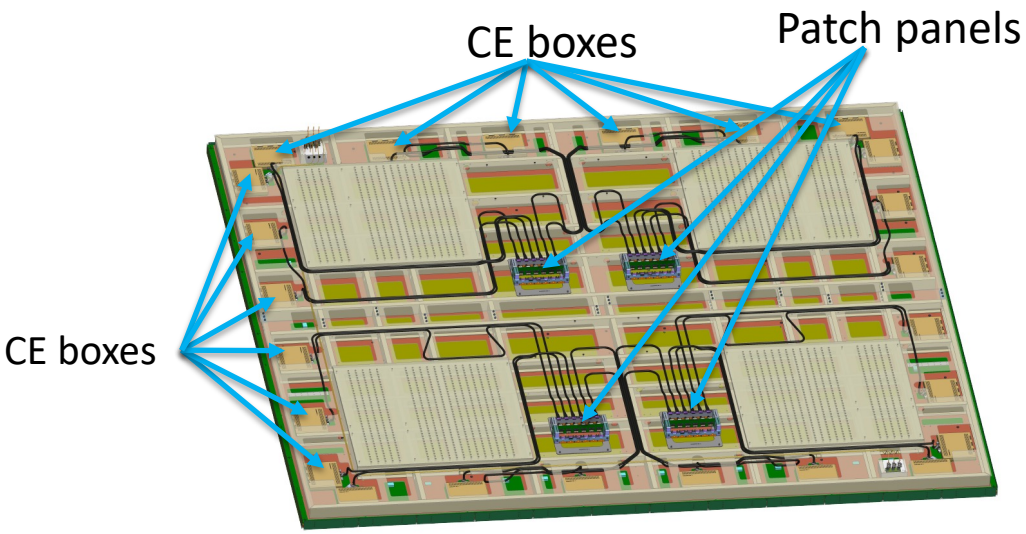
	1 - Executive Session *Zoom, Remote*		07:30 - 08:00
08:00	2 - Overview	Charge questions 3, 11, 14	*Cheng-Ju Lin*
	3 - Review documentation	Charge questions 1, 2, 3, 10, 15	*Vladimir Tishchenko*
	5 - Frontend Motherboard *Zoom, Remote*	Charge questions 3, 6, 7, 10	*Shanshan Gao* 08:35 - 09:05
09:00	6 - Warm Interface Board and Cold Cables	Charge questions 4, 7, 9	*Hucheng Chen*
	7 - Power & Timing Card *Zoom, Remote*	Charge questions 5, 8	*Adrian Nikolica* 09:25 - 09:55
10:00	Break		
	8 - Mechanical Supports	Charge questions 2, 4	*Manhong Zhao*
	9 - CERN cold boxes, NP04, and NP02 Results	Charge questions 4, 9	*Roger Huang*
11:00	10 - QA/QC, ESD, and Database *Zoom, Remote*	Charge questions 10	*Vladimir Tishchenko* 10:50 - 11:15
	11 - SURF Installation, CRP Factory, Cost/Schedule	Charge questions 12, 13, 15, 16	*Cheng-Ju Lin*
	12 - Daily Wrap-up		

DUNE Far Detector #2



Readout electronics for the 80 CRPs on the bottom drift volume are the same as the readout electronics for FD1 with minor modifications

Bottom Drift Electronics

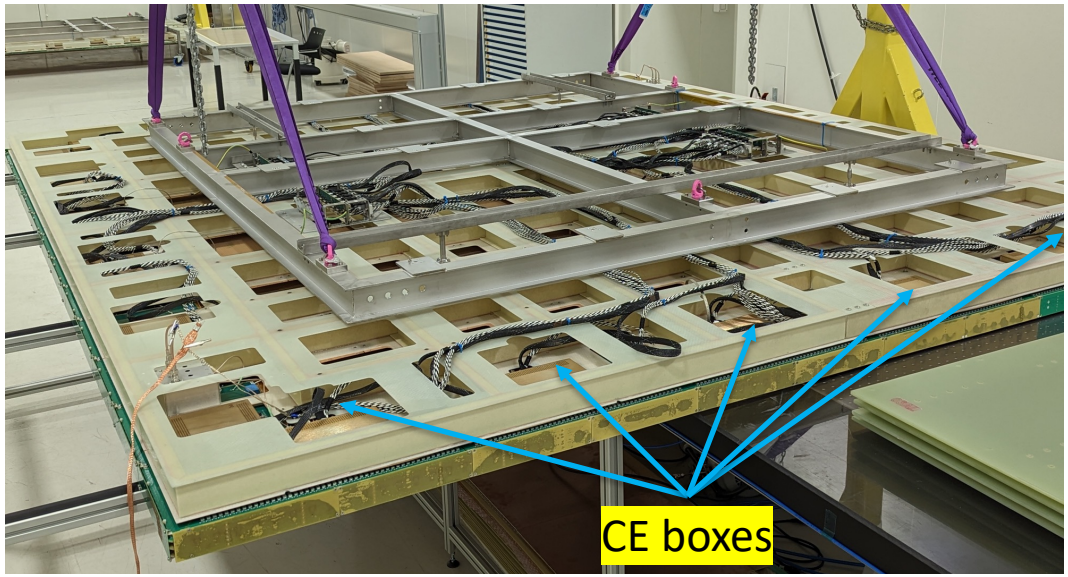


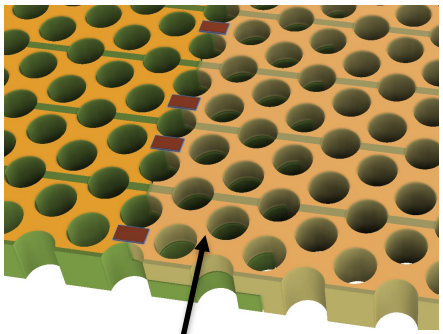
Bottom Drift Electronics are mounted directly on the CRP

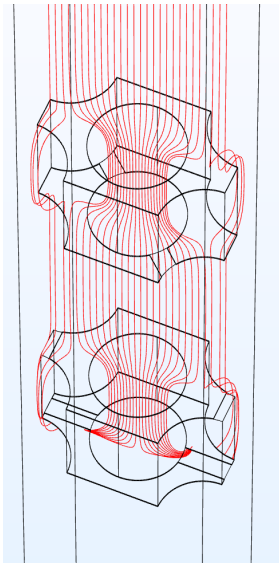
Each CRP (~3 m x 3 m) is instrumented with 24 Frontend Motherboards (FEMB) housed in a metal enclosure (CE Box)

Each CRP has:

- 476 first induction strips
- 476 second induction strips
- 584 collection strips
- Total readout strips of 1,536







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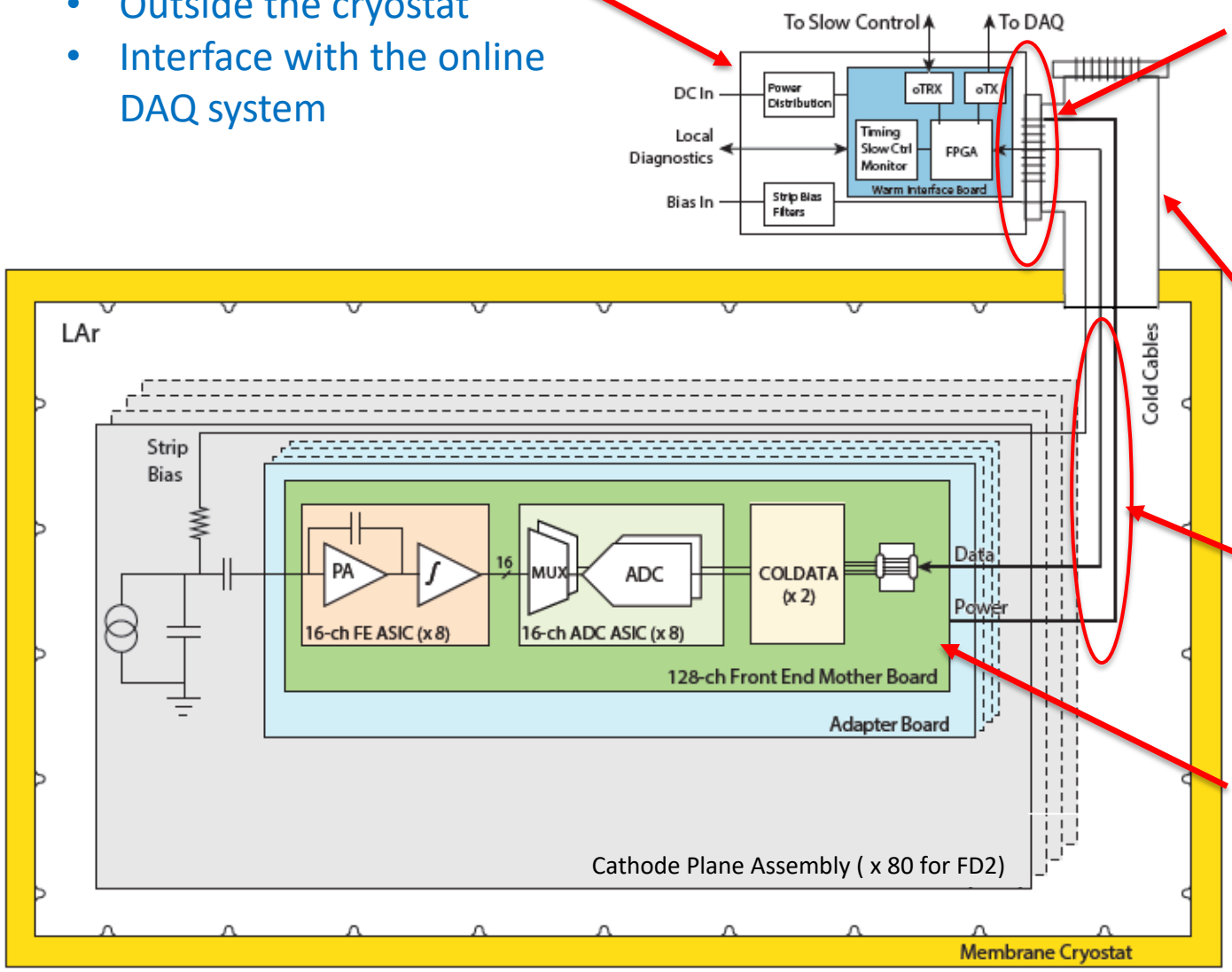
FD2 Bottom Drift Electronics

Warm interface electronics:
- Outside the cryostat
- Interface with the online DAQ system



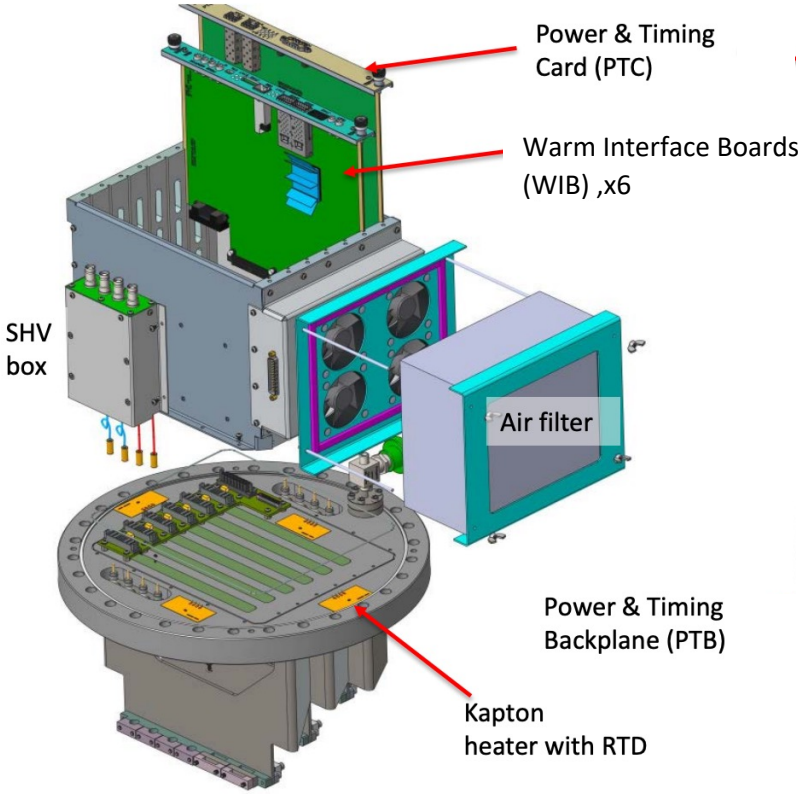
CE Flange:
- On top of the cryostat
- Connect cold cables to the Warm Interface Electronics

Signal feedthrough:
- 14” conflat
- Cable strain relief

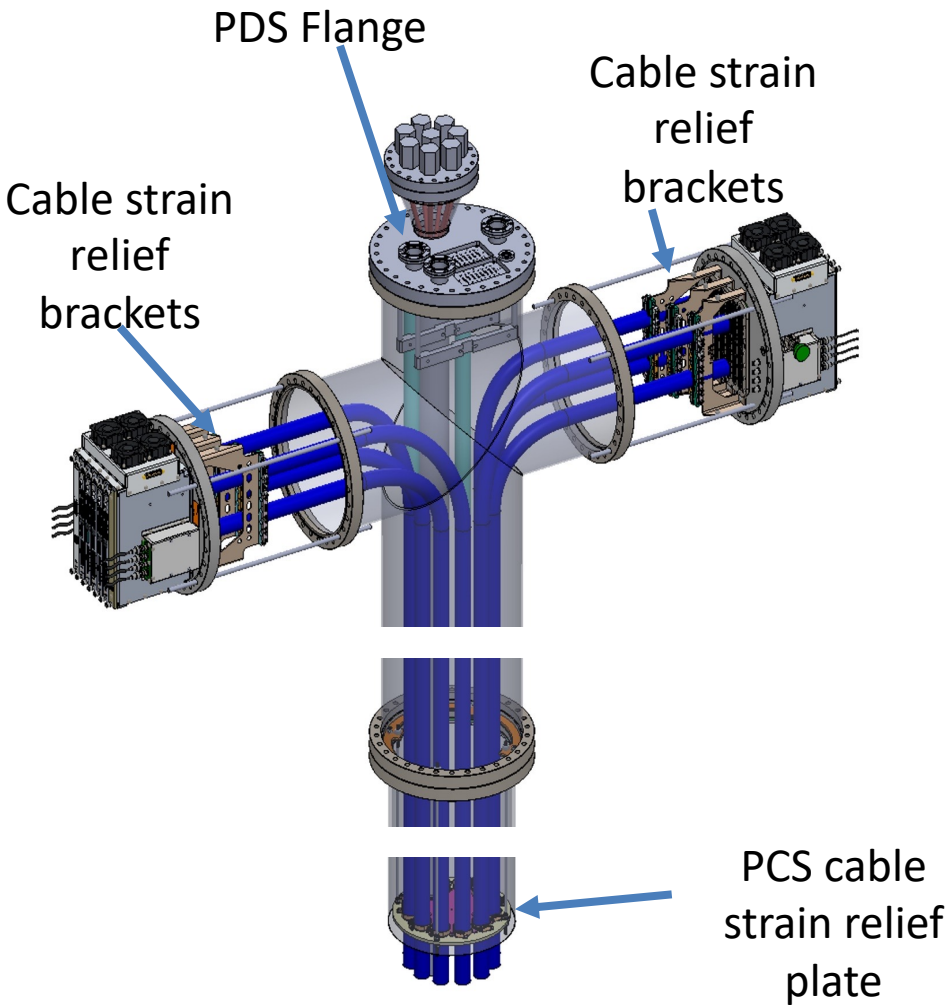
Cold cables: Low voltage and data cable to Frontend motherboard

Frontend Motherboard (FEMB): 128 channels of digitized wire readout enclosed in CE box

Warm Electronics and Cryostat Penetration



FD2: 80 Warm Interface Electronic Crates



FD2: 40 penetrations

Custom ASICs

LArASIC ASICs:

- 16-ch charge amplifier with adjustable shaping time and gain
- PRR in March 2022 https://indico.fnal.gov/event/53072/
- 250 wafers fabricated for FD1, FD2 and spares
- All wafers received by Dec 2022

ColdADC and COLDATA:

- ColdADC → 2 MHz digitizer with 16 ch input
- COLDATA → data serializer and control
- PRR on 8-May-2023 https://indico.fnal.gov/event/59429/
- If receives go-ahead from the Committee, will submit order for 50 wafers in early June for FD1

Changes Since FD2 BDE PDR

Cryostat penetration:

- At PDR, the baseline penetration design was a copy of FD1 design
- We discussed the plan to simplify the penetration design for FD2
- Our baseline now is the new design. Eliminated the CE crossing tube with supporting rods
- Implemented in NP02 for module-0
- Mechanical analysis signed off by the Compliance Office

DAQ Readout:

- Converted from FELIX to Ethernet readout
- Successfully integrated with DAQ using ethernet readout at the CERN vertical slice test-stand
- Converted two of the APAs (NP04 ProtoDUNE-II) to ethernet
- Plan to use ethernet readout for both CRPs for module-0

Changes Since FD2 BDE PDR

Power and Timing Cards:

- At PDR, still using ProtoDUNE-I PTC. Discussed plans to design a new PTC
- New PTC prototype is undergoing testing and debugging at UPenn now
- A second prototype PTC was built and sent to BNL for integration testing in a full crate
- Plan to build a third prototype for integration test at CERN
- See Adrian's talk for more info

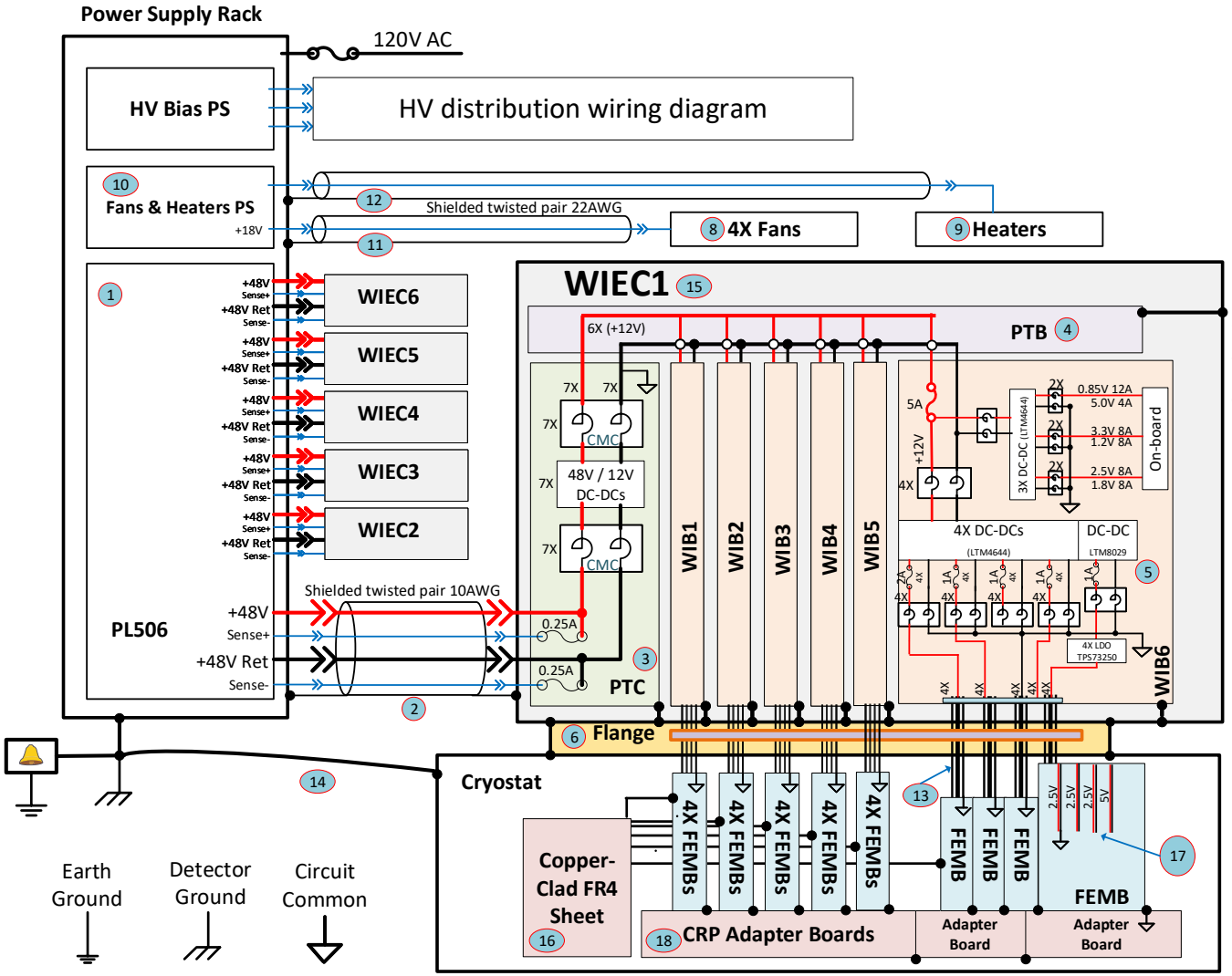
CRP Patch Panel:

- Design finalized and built/tested on CRP4 and CRP5 for module-0
- More detail in Hucheng and Manhong's presentations

Cold cables: length increased from 25 m to 27 m

FD2 BDE Grounding Diagram

Following guidance from the Grounding & Shielding Committee as documented in [EDMS#2095958]



1: Weiner PL506 Power Supply
2: 48V power cable
3: PTC (Power and Timing Card)
0.25A Fuse P/N: 3404.0006.11
Choke P/N: PLT10HH501100PNL
4. PTB (Power and Timing Backplane)
5: WIB (Warm Interface Board Version 3.0)
5A Fuse P/N: 3404.0017.11
2A Fuse P/N: 0468002.NR
1A Fuse P/N: 0468001.NR
Choke P/N: PLT5BPH5013R1SNL
6: Flange Board
7: FEMB (Monolithic Front End Motherboard)
8: Fans box
Fans are electrical isolated from WIEC
9: Heater
Heater is electrical isolated from WIEC
10: Fans & Heater power supply
11: Fans power cable (shielded)
12: Heater power cable
13: 7m cold power cable
14: Grounding cable
15: Warm Interface Electronics Crate (WIEC)
16: Copper sheet underneath the CRP composite frame
17: Voltage measured at FEMB
18: Adapter boards for the FEMBs to plug into
Note: Each adapter board takes 1 or 2 FEMBs, but adjacent boards are electrically and mechanically interconnected

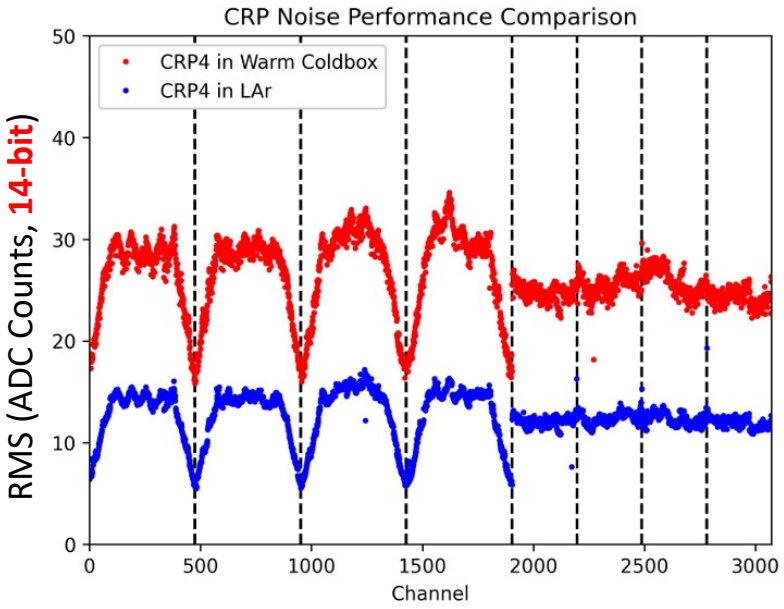
Notes
(1) Fans and heaters are isolated from WIEC
(2) PTB is mounted with the brass standoffs as a grounding connection
(3) The grounding connection between WIBs and WIEC is through front panels and side bars
(4) The grounding connection between PTB and WIEC is through front panels and side bars
(5) Flange (and flange board) is the place that the FEMB circuit common is referenced to the cryostat (detector ground)

- FD2 BDE grounding scheme was reviewed by the Grounding and Safety Committee for PDR. The grounding scheme has not changed
- CRP copper plane was unanimously approved by the FD2 Technical Board early this month. It's now the baseline design
- FD2 and FD1 share the same electrical design. Safety reviews for FD1 are directly applicable for FD2
- Now working with DUNE Compliance Office to work on FD2 specific electrical safety review

Prototyping at CERN

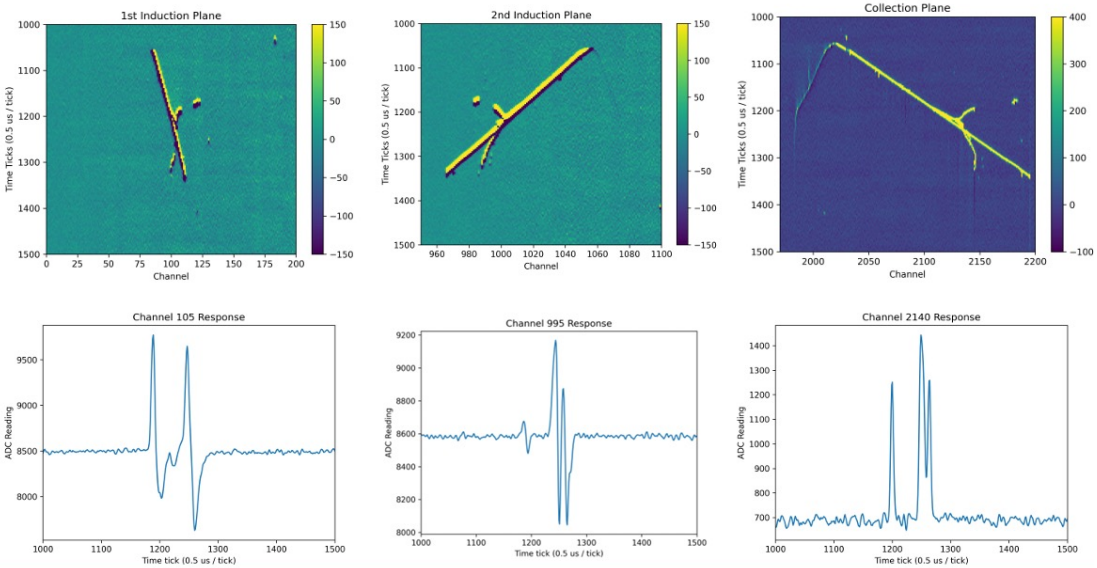
- We had ~ 2 years of operational experience in LAr with ProtoDUNE-I electronics. CE performed very reliably
- A number of FD2 prototype tests have been conducted and ongoing at CERN:
  - CRP1(b), a hybrid TBD-BDE CRP
  - CRP4 using final BDE tested in CERN cold box and now installed inside NP02 cryostat
  - CRP5 also using final BDE just completed the cold box test
  - CRP noise performance is as good as the best noise performance of APA

CRP4 Noise Performance

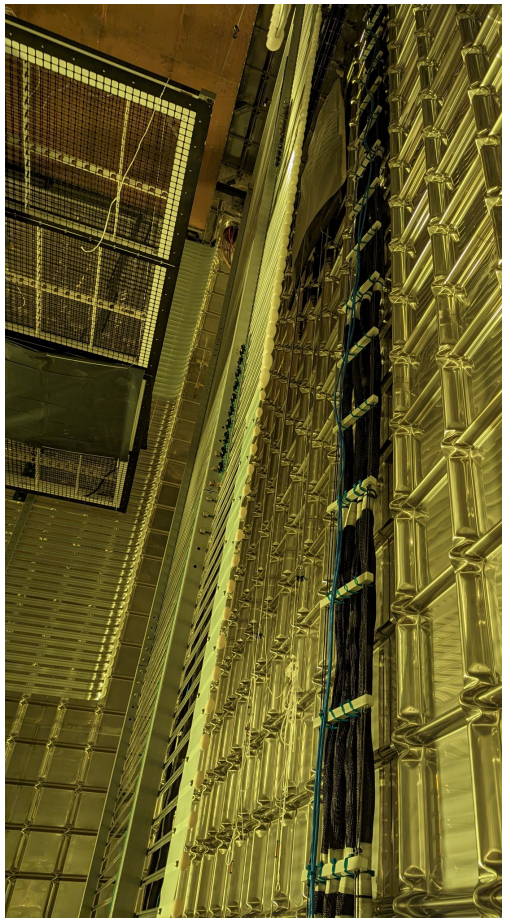


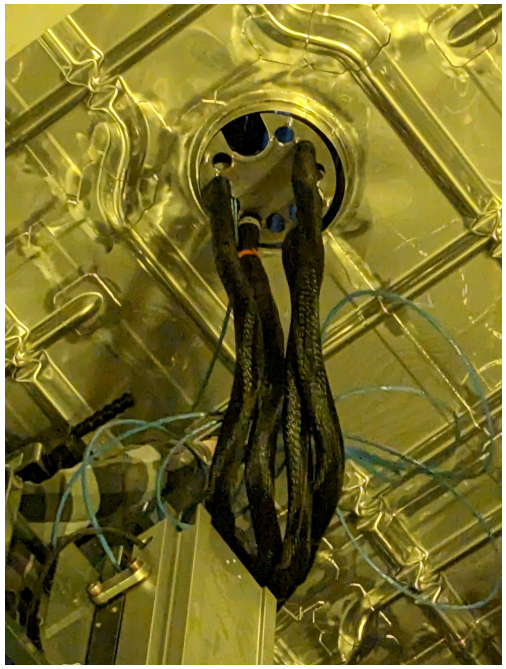
CRP4 Cold Box Run (Cosmic Track)

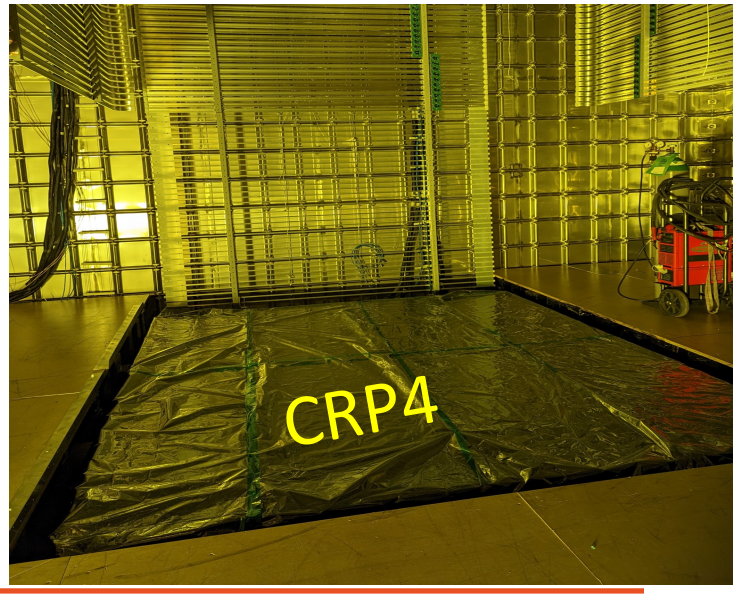
Taken from DAQ trigger tests, run 20472



Module-0







”Rehearsed”
FD2 installation

Recommendations from BDE PDR

FD2 BDE PDR recommendation tracking: https://edms.cern.ch/document/2681913/

Out of 16 recommendations, 12 are closed. The remaining 4 are flagged as for the "future"

Recommendation #1:

"The requirements and interface documents must be finalized. An approval process of these documents on EDMS is to be initiated, i.e. the interface documents need to be agreed and signed off by the respective interfacing Consortia "

All requirements and interface documents are finalized. All interface documents have been signed off by the respective Consortia. A few have already been approved via EDMS and the rest are in "engineering check state". We will close this recommendation when all interface documents are in the approved/released state in EDMS. Expect to close this recommendation before the end of this month

Recommendation #8:

"Reconsider the testing of the ASICS at LN2 temp after ProtoDUNE-2"

Will close this recommendation after ProtoDUNE-2

Recommendations from BDE PDR

Recommendation #10:

"Continue the lifetime studies of the ASICs"

Accelerated aging study of LArASIC (P5B) chip is nearly finished. ColdADC lifetime is completed after 1 year of testing. COLDATA lifetime study is ongoing. Expect to have a lifetime result by this summer. Will close this recommendation at the conclusion of COLDATA lifetime study

Recommendation #11:

"Run lifetime studies of FEMBs"

We plan to keep this recommendation open until the conclusion of the ProtoDUNE-II program

CD-3a Scope

- CD-3a (long-lead procurement) scope includes FD1 FEMB, WIB, PTC discrete components and also PTC FPGA
- Received CD-3a ESAAB from DOE early this year
- Last step is to obtain approval from PRR before submitting orders
- For PTC, we are only requesting 3 items in this review. We will request the rest after completing the full validation of the new PTC

Fully Loaded Costs

Sum of Value Row Labels	Resource ID Name	Column Labels HOURS	DIRECT	F-BDN-AY$
⊟131.FDC.02.09 FD1 TPC Electronics (TPC Elec) CD-3a				
⊞**131.FDC.02.09.01 Front-end ASIC - Production CD-3a**				
⊞**131.FDC.02.09.02 Cold ADC - Production CD-3a**				
⊞**131.FDC.02.09.03 Front-end Motherboards - Production CD-3a**				**640,308**
⊟**131.FDC.02.09.04 Warm Interface Electronics Crate and Boards - Production CD-3a**				
⊟131.FDC.02.09.04 Warm Interface Electronics Crate and Boards - Production CD-3a				
⊟**131.FDC.02.09.04 Warm Interface Electronics Crate and Boards - Production CD-3a**				
⊟131.FDC.02.09.04 Warm Interface Electronics Crate and Boards - Production CD-3a				
⊟**13122.2004.142.274**				
⊞Vendor delivers the discrete components for the PTCs of FD1 – Penn (CD-3a)				**143,773**
⊟**13122.2004.142.276**				
⊞Vendor delivers the FPGA for the PTCs of FD1 – Penn (CD-3a)				**175,046**
⊟**13122.2004.142.284**				
⊞Vendor delivers the discrete components for the WIBs of FD1 – BNL (CD-3a)				**1,339,286**
⊞**13122.2004.142.286**				

Thank You !

BACKUP SLIDE

DUNE Final Design Review Charge
Far Detector 2 Bottom Drift Electronics
16 May 2023

The committee is requested to review the final design of the DUNE far detector (FD2-VD) bottom drift electronics (BDE) system. For reference, the BDE preliminary design report is available at EDMS-2681912.

The committee should assess: Does the design meet the requirements of final design readiness as outlined in the LBNF/DUNE Review Plan (EDMS-2173197) and the required DUNE documents in EDMS- 2493568?

The committee should consider:

1. Are the requirements and interfaces documents finalized and approved?
2. Is the documentation of mechanical specifications complete, including 3D model and the 2D drawings for standard and custom components as well as the Compliance Office evaluation focusing on both safety and the proper application of design codes and standards.
3. Is the documentation of electrical specifications complete, including system schematics, drawings, connections, and grounding details. Has the electrical safety analysis been completed and approved by the Compliance Office.
4. Has the design of the patch panel been finalized, a prototype produced, tested and validated with a CRP?
5. Has the PTC design been finalized, and a prototype tested and validated?
6. Have the lifetime studies of the FEMBs been completed?
7. Can the procurement of the discrete components for the WIBs and the FEMBs be launched?
8. Can the procurement of some PTC components be launched?
9. Have the CRP tests with the FEMBs, miniSas cables and the final patch panel been completed?
10. Has the QC plan document been produced, including a comprehensive ASIC and board ESD handling procedure?
11. Has the grounding and shielding scheme been finalized and reviewed by the DUNE Grounding and Shielding Committee?
12. Has the CRP installation been fully defined with the installation team including connection to the Samtec cables?
13. Are the schedule and risks sufficiently complete for this stage of the project?
14. Has the BDE consortium responded appropriately to recommendations from past reviews (BDE PDR, ASICs FDR, FD1 TPC Electronics FDR)?
15. Is the draft documentation detailing plans for procurement, manufacturing, quality control, and part identifiers at a sufficient level of maturity for this stage of the design?
16. Is the present level of effort appropriate for reaching the PRR and are plans in place to fully staff for production? Based on the MoU Annex and Interface Documents, is the scope of the subsystem complete and the contribution from each funding agency sufficiently well defined?
17. Please assess the technical readiness of the major BDE subsystem elements.

BDE Requirements/Specifications

Executive Board held requirements for FD1-HD are also valid for FD2-VD

TDR ID	Name	Primary Text	Value
SP-FD-2	System noise	The total system noise seen by each wire should be no more than 1000 enc of noise. It is expected that random noise on the FE amplifier will be the dominant contribution to the total system noise.	<1000 electrons
SP-FD-13	Front-end peaking time	The FE peaking time shall be set so as to optimize vertex resolution.	1 microsecond (goal: adjustable to be able to take advantage of lower noise if the noise depends on peaking time)
SP-FD-14	SP signal saturation level	~500,000 electrons	~500,000 electrons (goal: Adjustable so as to see saturation in less than 10% of beam-produced events)
SP-FD-19	ADC sampling frequency	The ADC sampling frequency shall be set so as to extract maximal information without unnecessarily increasing data rate.	~ 2MHz
SP-FD-20	Number of ADC bits	The ADC shall digitize the charge deposited on the wires with 12 bits precision	12 bits
SP-FD-21	SP cold electronics power consumption	The SP CE power consumption shall remain below 50 mW/channel	< 50mW/channel
SP-FD-25	Non-FE noise contributions	All non-FE noise contributions shall be much lower than the targeted system noise level	<< 1000 electrons

BDE Requirements/Specifications

- Most Technical Board held requirements for FD1 TPC Electronics are also valid for FD2 Bottom Drift Electronics
- Combination of requirements, design choice and specifications

TDR ID	Name	Primary Text	Value
SP-ELEC-2	Gain of the SP TPC elec. front-end amplifier	Gain of the front-end amplifier	10 mV/fC (adjustable in the range of 5-25 mV/fC)
SP-ELEC-3	SP TPC elec system synchronization	Maximum time difference between ADC samples on different wires	16 ns
SP-ELEC-4	Number of channels per SP TPC elec front-end motherboard	Number of channels in each front-end motherboard	128
SP-ELEC-5	Number of links between the SP TPC elec FEMB and the WIB	Maximum number and speed of links used for data transmission between the FEMB and the WIB	4 at ~ 1.28 Gbps
SP-ELEC-6	Nunber of SP TPC elec FEMBs per WIB	Number of FEMB connected to each WIB	4
SP-ELEC-7	Data transmission speed between the SP TPC elec WIB and the DAQ backend	Each WIB should transmit data to the DAQ backend at a speed of 10 Gbps	10 Gbps

BDE Requirements/Specifications

- Additional requirements or specifications under consideration at the CE Consortium level
- Listing sample requirements here. See EDMS#2590797 for a complete list
- Data transmission:
  - FEMB can drive signal over cold cable > 25m (open eye diagram)
- ADC linearity requirements: INL, DNL and ENOB
- Warm interface crates, WIB, and PTC requirements:
  - WIB calibration
  - Clock jitter from WIB to FEMB
  - PTC output voltage ripple, etc.
- Power supply requirements:
  - Current and voltage requirements
  - Noise ripple, V/I readback rate, etc.
- Offline physics requirements:
  - ADC overflow logic
  - Double pulse resolution
  - Saturation recovery
  - Channel-to-channel cross talk, etc.