

DUNE FD2 BDE Final Design Review

Frontend Motherboard (FEMB)

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05/16/2023

Charge Questions

3. Is the documentation of electrical specifications complete, including system schematics, drawings, connections, and grounding details. Has the electrical safety analysis been completed and approved by the Compliance Office.

- BDE specification and requirement is documented on EDMS:
 - <https://edms.cern.ch/document/2590797/>
- The electrical safety analysis is not completed yet
 - No power rail related to FEMB exceeds 5V.
 - WIB has 1A/2A fuses for each power rail to FEMB
 - WIB can measure voltage/current of each power rail to FEMB, thus an interlock can also be implemented on WIB side to protect FEMB from abnormal voltage/current.

6. Have the lifetime studies of the FEMBs been completed?

Being finalized.

7. Can the procurement of the discrete components for the WIBs and the FEMBs be launched?

Yes.

Content

- Charge Questions
- **FEMB Requirement and Design**
- FEMB Production Experience
- QA/QC
- Summary

DUNE BDE Requirements related to FEMB

<https://edms.cern.ch/document/2590797/>

Executive Board held requirements for FD1-HD are also valid for FD2-VD

TDR ID	Name	Primary Text	Value	FEMB related
SP-FD-2	System noise	The total system noise seen by each wire should be no more than 1000 enc of noise. It is expected that random noise on the FE amplifier will be the dominant contribution to the total system noise.	<1000 electrons	Yes
SP-FD-13	Front-end peaking time	The FE peaking time shall be set so as to optimize vertex resolution.	1 microsecond (goal: adjustable to be able to take advantage of lower noise if the noise depends on peaking time)	Yes
SP-FD-14	SP signal saturation level	~500,000 electrons	~500,000 electrons (goal: Adjustable so as to see saturation in less than 10% of beam-produced events)	Yes
SP-FD-19	ADC sampling frequency	The ADC sampling frequency shall be set so as to extract maximal information without unnecessarily increasing data rate.	~ 2MHz	Yes 1.9625MHz
SP-FD-20	Number of ADC bits	The ADC shall digitize the charge deposited on the wires with 12 bits precision	12 bits	Yes 14bit
SP-FD-21	SP cold electronics power consumption	The SP CE power consumption shall remain below 50 mW/channel	< 50mW/channel	Yes
SP-FD-25	Non-FE noise contributions	All non-FE noise contributions shall be much lower than the targeted system noise level	<< 1000 electrons	Yes

DUNE BDE Requirements related to FEMB

<https://edms.cern.ch/document/2590797/>

- Most Technical Board held requirements for FD1 TPC Electronics are also valid for FD2 Bottom Drift Electronics
- Combination of requirements, design choice and specifications

TDR ID	Name	Primary Text	Value
SP-ELEC-2	Gain of the SP TPC elec. front-end amplifier	Gain of the front-end amplifier	10 mV/fC (adjustable in the range of 5-25 mV/fC)
SP-ELEC-3	SP TPC elec system synchronization	Maximum time difference between ADC samples on different wires	16 ns
SP-ELEC-4	Number of channels per SP TPC elec front-end motherboard	Number of channels in each front-end motherboard	128
SP-ELEC-5	Number of links between the SP TPC elec FEMB and the WIB	Maximum number and speed of links used for data transmission between the FEMB and the WIB	4 at ~ 1.28 Gbps
SP-ELEC-6	Number of SP TPC elec FEMBs per WIB	Number of FEMB connected to each WIB	4
SP-ELEC-7	Data transmission speed between the SP TPC elec WIB and the DAQ backend	Each WIB should transmit data to the DAQ backend at a speed of 10 Gbps	10 Gbps

FEMB related

Yes

Yes

Yes

Yes (4@1.25Gbps)

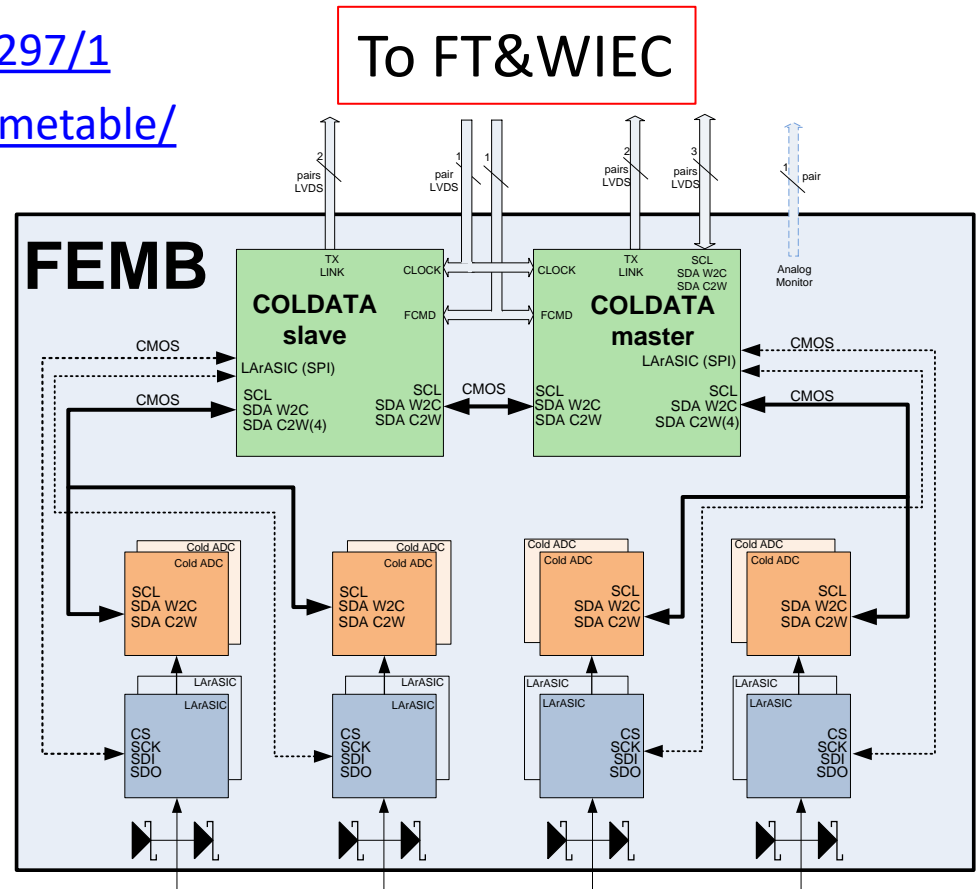
The Monolithic FEMB with 3-ASIC

DUNE FD1-HD TPC Electronics FDR Document and Review

<https://edms.cern.ch/document/2782297/1>

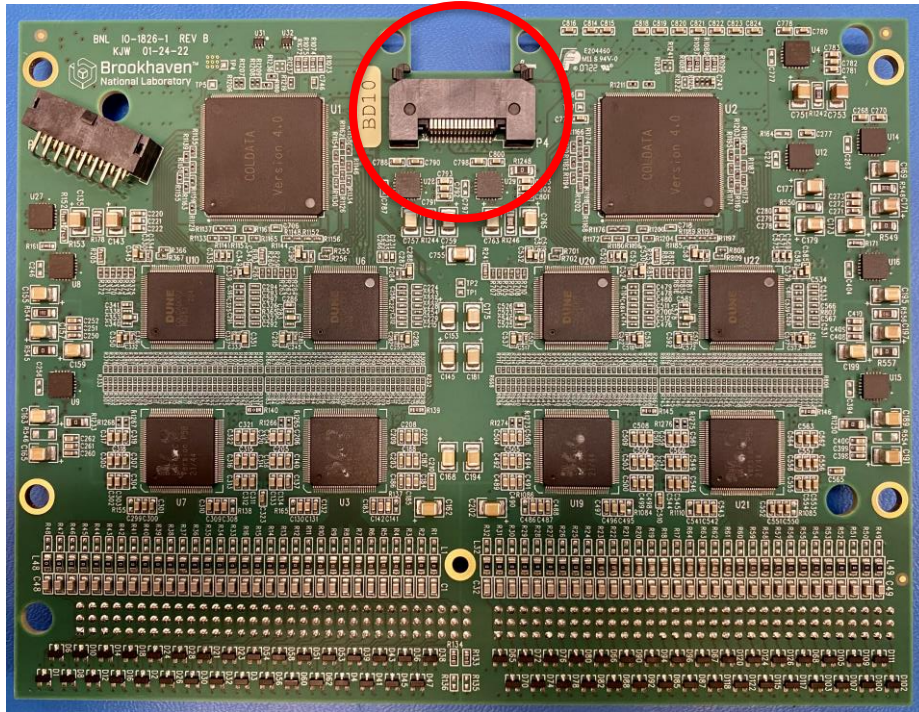
<https://indico.fnal.gov/event/56228/timetable/>

- **Perform digitized readout of 128 TPC electrodes in liquid Argon**
 - 8x LArASIC (P5B)
 - 16-ch programmable charge amplifier
 - Enhanced ESD protection
 - 8x ColdADC (P2)
 - 16-ch, 12-bit, 2 MS/s ADC
 - INL < 5 LSB, DNL < 0.3 LSB
 - 2x COLDATA (P4)
 - Used to be FPGA in ProtoDUNE-I
 - Serializer and controller
 - 2 x 1.25 Gb/s TX data link per chip

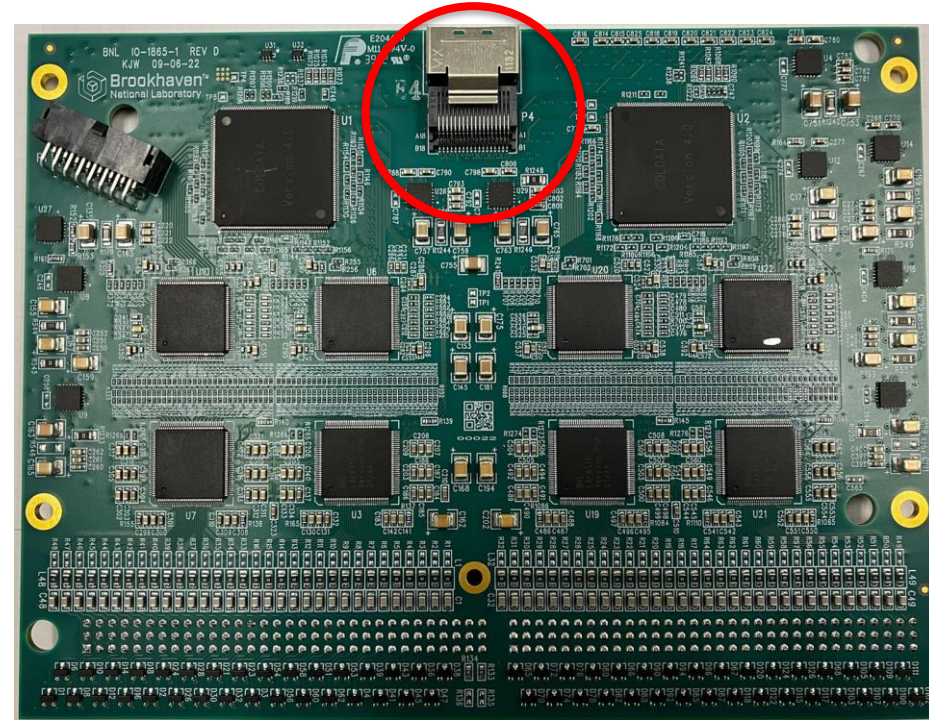


128 CHs FROM Anode planes (APA or CRP)

The Monolithic FEMB-HD and FEMB-VD



IO-1826-1B used in ProtoDUNE-HD
Samtec ASP-191865-03 connector

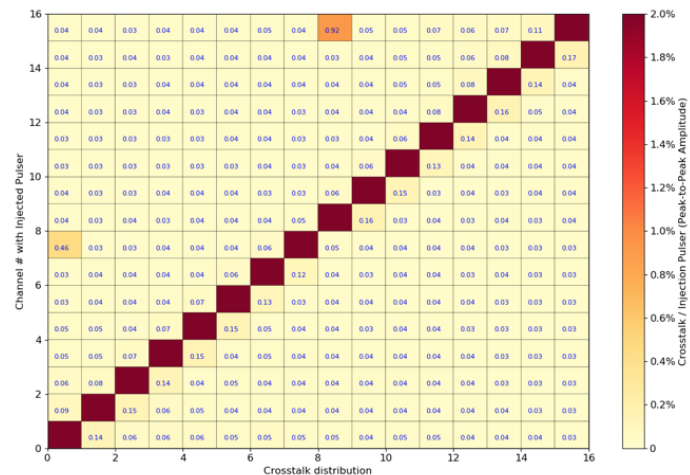
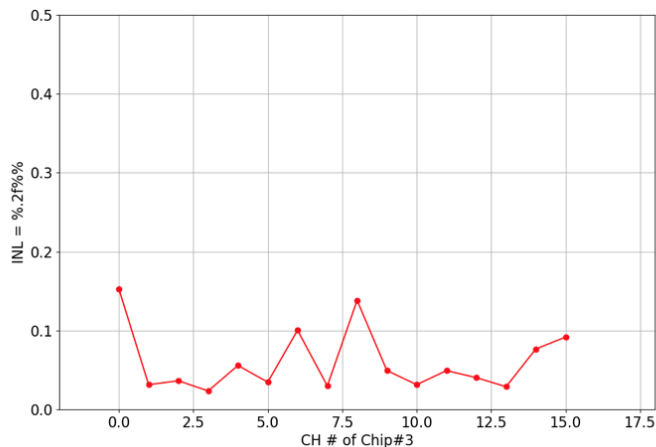
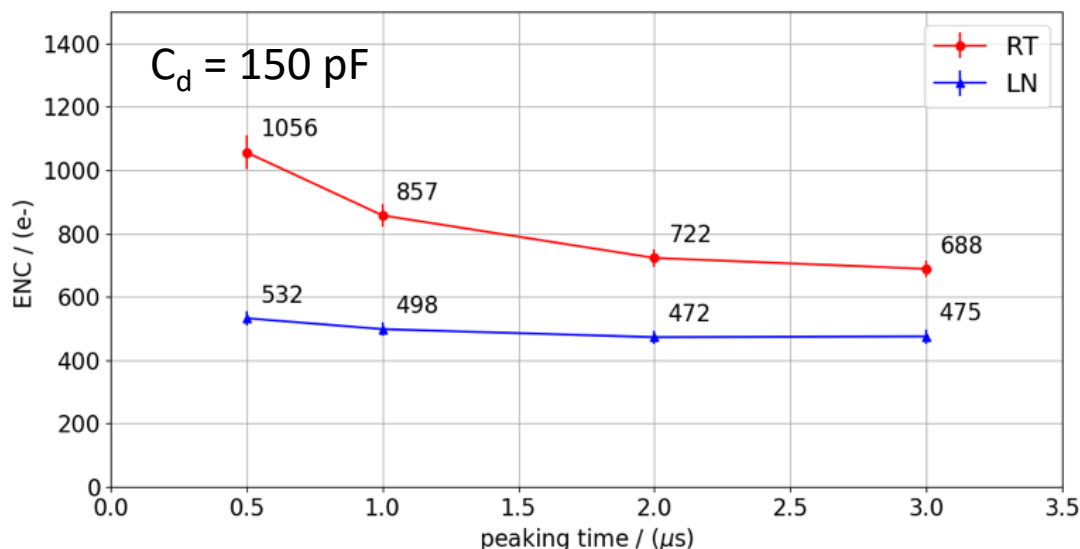


IO-1865-1D used in ProtoDUNE-VD
MiniSAS connector

The only difference between FEMB-HD and FEMB-VD is data cable connector!

FEMB Performance

- FEMB with P5B LArASIC, P2 ColdADC and P4 COLDATA meets DUNE requirement



The overall crosstalk is $< 0.1\%$ at LN2 temperature for both single ended and differential interfaces, except CH0 (affected by CH7) and CH8 (affected by CH15), which are still $< 1\%$.

Integral non-linearity (INL) of 16 channels on the monolithic FEMB at LN2 temperature. The INL $< 0.1\%$ can be achieved for most channels up to the full dynamic range of 80 fC, except CH0 and CH8 have slightly larger non-linearity. Over all the measurements show that the INL of the monolithic FEMB is well below the DUNE requirement of 1%.

FEMB Power Consumption

- Meet < 50 mW/ch requirement
 - The power consumptions of P5 LArASIC, P2 ColdADC and P3 COLDATA have been measured. The power consumption is ~29 mW/ch with single ended output without buffer, and ~34 mW/ch with differential output and SEDC buffer turned on. Taking into account the power consumption in voltage regulators, with ~300 mV voltage drop of voltage regulators, the total power consumption of a monolithic FEMB is **less than ~45 mW/ch**, or a total ~5.8 W

Env	SMU	Current at 900 mV BL (mA)			Current at 200 mV BL (mA)		
		OFF	SE ON	SEDC ON	OFF	SE ON	SEDC ON
RT	VDDP = 1.8V	31.5	31	31.5	31.5	31	31.4
	VDD = 1.8V	20	47	50.6	18.5	43	49.8
	VDDO = 1.8V	0.1	6	12.4	0.1	6	14.2
	Power per ch. (mW)	5.8	9.5	10.6	5.6	9.0	10.7
LN2	VDDP = 1.8V	31.3	31	31.3	31.3	31	31.2
	VDD = 1.8V	17.1	44	50.1	15.5	42	51.4
	VDDO = 1.8V	0.1	6	12	0.1	5	13.2
	Power per ch. (mW)	5.5	9.1	10.5	5.3	8.8	10.8

Power rail / V	RT	LN2
	CMOS Reference	CMOS Reference
	Current / mA	Current / mA
2.25V (VDDA2P5, VDDD2P5)	128.0	132.4
1.1V (VDDD1P2)	1.3	1.2
2.25V (VDDIO)	15.3	14.5
Total Power Consumption /mW	323.9	331.8
mW/CH	20.2	20.7

Measured at RT with the P5 FE + P2 ADC + P3 COLDATA		
Power Rails	Measured Voltage / V	Measured Current / mA for 2x COLDATA chips on board
CD_VDDIO (2.25V)	2.236	111
CD_VDDA (1.20)	1.197	19
CD_VDDD & CD_VDDC (1.1V)	1.095	64
Power Consumption per chip	171 mW	
Power Consumption per CH	2.7 mW	

Integration Test

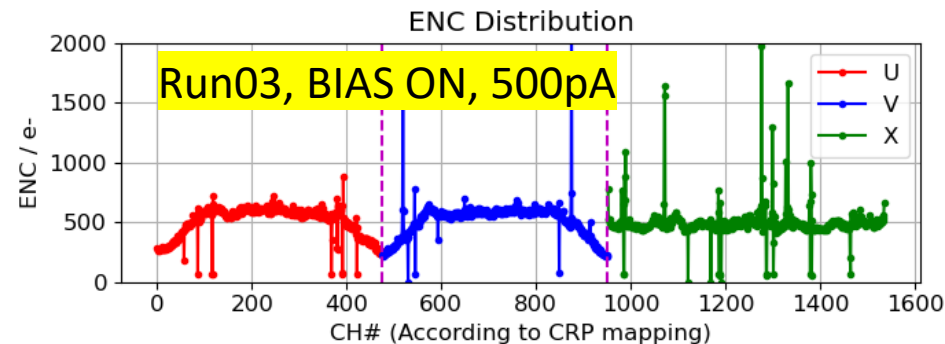
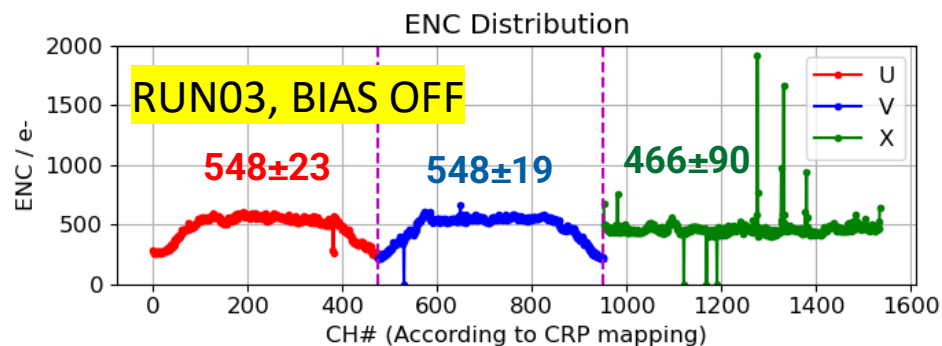
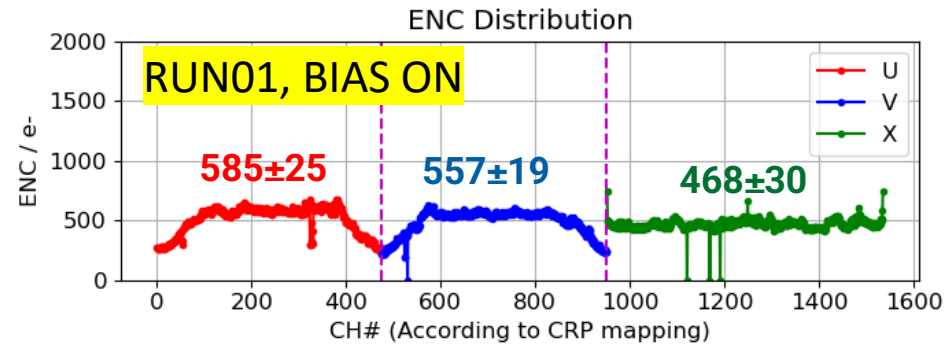
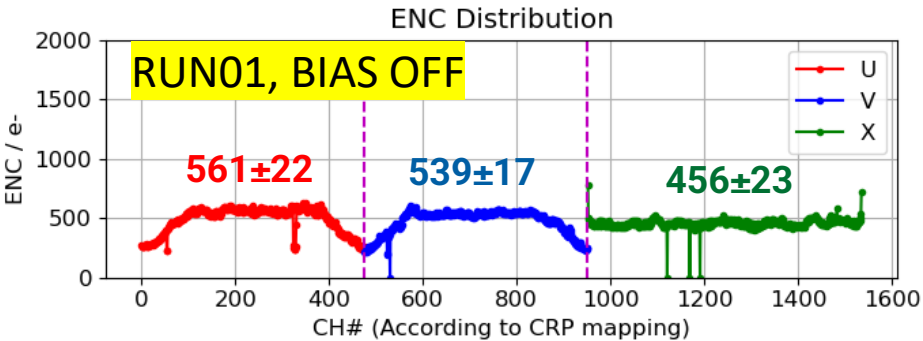
- CERN Cold Box and ProtoDUNE-II
 - Please refer to Roger's talk
- BNL CRP5A Integration Test
 - https://indico.fnal.gov/event/53965/contributions/258136/attachments/163300/216099/CRP5A%20at%20BNL_012_52023.v1.pdf



RUN01: CE face up



RUN03: CE face down



Microphonics observed at CERN as well

FEMB Lifetime at LAr

- Lifetime study for semiconductor devices
 - HCE effect is negligible
 - Projected lifetime of LArASIC: $\sim 1 \times 10^7$ years
 - Projected lifetime of ColdADC: 3.02×10^5
 - Projected lifetime of COLDATA:
 - Not yet completed
 - Should be similar as ColdADC since it uses same 65nm process from the same foundry as ColdADC
 - Projected lifetime of LDO (TPS74201): $> 1 \times 10^7$ years
- ProtoDUNE-I Experience
 - Nearly two years operation in LAr, no significant degradation was observed towards all components on FEMBs
 - LDO (TPS74201), analog switch (TS5A63157DCKR), protection diode (BAV99LT1G) and most passive components are inherited for the DUNE 3-ASIC FEMB
 - No passive components failure was observed
- ProtoDUNE-II
 - Will get more lifetime data from both NP02 and NP04

Content

- Charge Questions
- FEMB Design
- **ProtoDUNE-II FEMB Production Experience**
- QA/QC
- Summary

FEMB Production for ProtoDUNE HD&VD

- Effort is needed to improve yield of FEMB production for DUNE
 - Assembly quality can be improved
 - The latest version removes 0201 resistors which cause 50% of assembly issues
 - 3 ASICs should at least be warm-screened

HD / VD	Assy Batch	FEMB Quantity	Failure Mode (Total / Cold)				
			Assembly	COLDATA ^[1]	ColdADC	LArASIC	Other parts
HD	1B-1	25	0	0	0	0	2 / 1
HD	1B-2	20	2 / 0	2 / 2	3 ^[2] / 2	1 / 1	0
HD	1B-3	65	1 / 0	4 / 0	0	1 ^[3] / 0	2 / 1
VD	1C-1	15	1 / 0	0	1 / 1	1 / 1	0
VD	1D-1	20	4 / 0	2 / 0	0	1 / 1	0
VD	1D-2	40	1 / 0	2 / 0	0	2 / 1	0
Fail / Total boards			9 / 175	10 / 175	4 / 175	6 / 175	4 / 175
Fail / Total chips		/	/	10 / 350 chips	4 / 1400 chips	6 / 1400 chips	/

Note:

[1]: COLDATA chips are untested chips

[2]: HD-1B-2-20-ColdADC, 2 chips failed at cold were only tested at warm

[3]: HD-1B-3-65-LArASIC, QC test report shows the chip already failed at warm. The chip was put in the PASS tray by handing mistake.

[4]: FEMB assembled for debugging is not included in this table

Content

- Charged Questions
- FEMB Design
- FEMB Production Experience
- **FEMB QC Testing**
- Summary

FEMB related Documentation

- Master spreadsheet for the FDR document

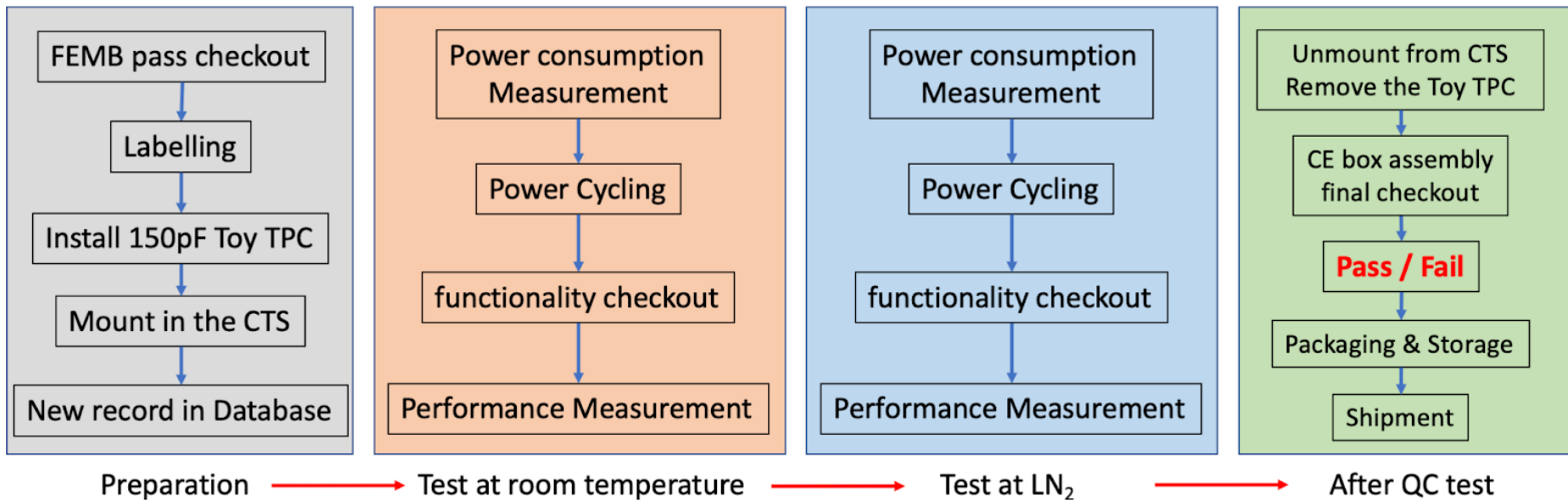
<https://edms.cern.ch/document/2894122/>

Category	Document	EDMS	File Name	Description	Charge questions
Design Documents	Technical Design Reports	2810246	DUNE-FD2-TDR-v2-16Mar2023.pdf	See Chapter 4.4 of FD2 TDR: "Bottom Drift Readout". The BDE are almost identical to the FD1-HD TPC electronics. The differences are summarized in section 4.4.3.10. More details on FD1-HD TPC electronics are given in the following four lines.	
		2892577	DUNE_Doc_CRP_BDE_ColdboxTests_v1.docx	The most recent summary of results of system tests in ProtoDUNE VD	9
Requirements & Specifications	Bottom Drift Electronics	2590797	FD2-VD_CE_Requirements_08May2023.xlsx	Spreadsheet with all the requirements / specifications for BDE from DUNE Executive Board, Technical Board, and TPC Electronics Consortium	1
Interface Documents	CRP	2618995	CRP_BDE_interface_v3.pdf	Interface document between CRP and BDE	1
Grounding	Ground Rules	2729002		Bottom drift electronics power distribution and grounding diagram	3
ASICs	LArASIC	2314428	LArASIC_P5B_Datasheet_V1.pdf	Datasheet for LArASIC (v. P5B).	
	ColdADC	2314429	COLDADC_P2_Datasheet.pdf	Datasheet for ColdADC (v. P2).	
				COLADC_P2_Testing_v3.docx	Measurements of ColdADC P2 performance
	COLDATA	2314430	COLDATA_P3_Datasheet.pdf	Datasheet for COLDATA (v. P3)	
			COLDATA_P3_Testing.docx	Measurements of the COLDATA P3 performance	
Design files	FEMB	2884557	DUNE_Monolithic_FEMB_Minisas_IO-1865-F.pdf	Schematics of the current monolithic FEMB	3
		2884557	io1865-1f.pdf	FEMB PCB	
		2884557	BOM_IO_1865_1F_04192023_draft.xlsx	FEMB BOM	
Engineering analysis documents		2823884	Structural_Analysis_of_DUNE_VD_BDE_Mechanical_System	Structural analysis of BDE mechanical components	2
		2823202	VD_BDE_CO_validation.docx	Report from the Compliance Office	
Production and QC plans	Manufacturing and Procurement Plan	2604783	2604783_ASIC_Production_QC	Document describing the production plans for the ASICs.	15
	QA plan	2606690	Post_TDR_Update_FD1_HD_TPC_Electronics-84.pdf	See section 1.3 in FD1-HD TDR	
	QC plan	2815079	FD1_TPC_Elec-FD2_BDE_QC_Plan_docx_cp.pdf	QC plan	10
Installation Documents		2689089	2023-04-10-FD2_VD_Installation_Plan_Apr_7_2023_docx_cp.pdf	Detector installation plan. Sections related to BDE installation: 5.1 (Installation on cryostat roof), 6.3 (cable installation)	12

QC plan: <https://edms.cern.ch/document/2815079/>

FEMB QC Procedure

- All data from the QC process will be stored in a common database, and the yields of the production will be centrally monitored and compared among different sites.



FEMB QC

- FEMB PCB fabrication confirmation
 - The PCB fabrication house provides a test report of electrical continuity and shorts test
 - Visual inspection for a few bare boards of each production batch
- Post-assembly FEMB checkout
 - A visual inspection should be performed before power on
 - Missing soldering, extra soldering paste on board, extra components on board, insufficient cleaning. ...
 - A FEMB checkout test
 - Power consumption is normal
 - All communication links are good (high-speed links, I2C, fast command, and monitoring)
 - Consistent calibration pulse response of each channel on board
 - Reasonable baseline of each channel
 - Reasonable noise distribution when the input is floating
 - Only a FEMB passes the checkout can be accepted as a qualified unit for the QC testing. A routing QC procedure for a CE box assembly starts from here.
 - The similar checkout procedure will also be necessary later during the reception test of CE box assemblies and cold cables when they arrive at the destination (South Dakota).

Post-Assembly Checkout Report

- Any assembly failure can be figured out during checkout
 - ~1 min data taking for 4 FEMBs on a benchtop test stand

PASS/FAIL criteria implemented in the analysis script

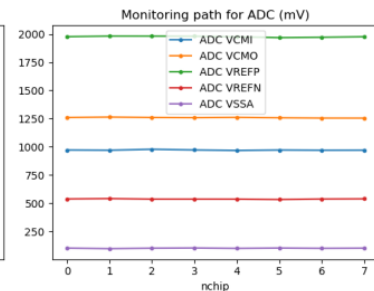
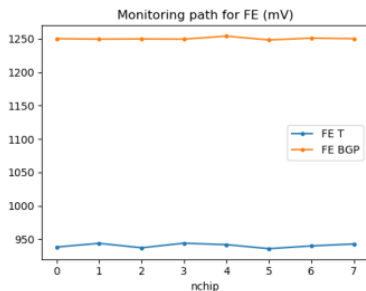
FEMB#6569 Checkout Test Report

Tester: lke
 Temperature: RT
 Note: RTCK
 FEMB configuration: 200mVBL, 14_0mVIC, 2_0us, 500pA, DAC=0x20
 Date: 06_20_2021_08_47_40
 Input Capacitor(Cd): 150pF

Measurement	Result
Power Measurement	Pass
Temperature	Pass
BGP	Pass
RMS	Pass
200mV Baseline	Pass
Pulse_SE	Pass
Pulse_DIFF	Pass
ADC Monitoring	Pass

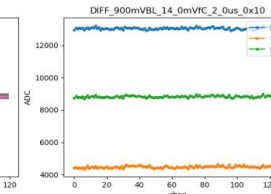
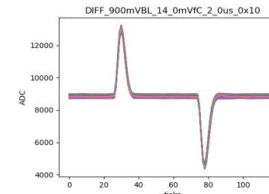
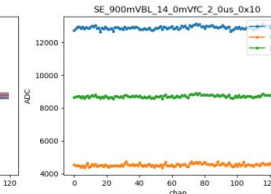
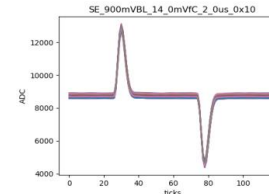
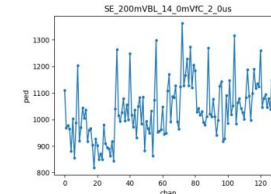
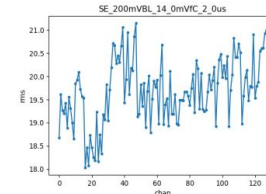
Power Consumption = 7.526 W

name	V_set/V	V_meas/V	I_meas/A	P_meas/W
BIAS	5.0	5.0	0.0	0.0
LArASIC	3.0	2.915	0.424	1.236
ColdDATA	3.0	2.976	0.229	0.682
ColdADC	3.5	3.403	1.648	5.608



Monitoring path for FE-ADC (#mV)

ASIC#	FE T	FE BGP	ADC VCMi	ADC VCmO	ADC VREFP	ADC VREFN	ADC VSSA
0.0	938.2	1250.1	972.6	1260.5	1976.5	539.2	103.8
1.0	943.8	1249.5	970.5	1264.1	1981.5	542.2	98.6
2.0	937.1	1249.8	978.9	1260.6	1981.2	537.5	103.1
3.0	944.0	1249.4	972.9	1259.1	1980.0	537.6	104.9
4.0	941.8	1254.0	968.4	1261.6	1975.6	537.4	101.2
5.0	935.8	1248.2	972.5	1258.0	1968.0	534.1	104.5
6.0	939.9	1251.0	970.4	1255.4	1971.1	538.5	101.6
7.0	942.8	1250.1	971.0	1255.0	1976.2	540.0	103.4



FEMB QC Items

- Preparation Phase
 - Install two 64-channel 150 pF Toy TPC boards on each FEMB
 - **Place FEMB into the CTS/RTS**
 - Up to 4 boards may be tested simultaneously to improve efficiency
 - A new item will be created in the database for each CE box assembly with the initial information, such as date and time, test setup number, CE box serial number, location, name of who performs the test, and so on
- **Phases of tests at room temperature (RT) / liquid nitrogen (LN2)**
 - Power consumption measurement
 - Power cycling test (optional at RT, mandatory at LN2)
 - Functionality checkout
 - Performance measurement
- Phase of post-QC test
 - FEMBs passed the cryogenic test will be installed in the CE box
 - A similar fast checkout test should be performed to finalize the QC test
 - A judge of **pass/fail** CE box assembly thus will be made before packaging

FEMB QC Items (Functionality checkout)

Item	Description	Expected output
Communication links	I2C and FAST command communication between Coldata and WIB I2C communication between ColdADC and Coldata SPI communication between LArASIC and Coldata Data pattern from ColdADC all the way to the WIB	No communication failure or error
Reset	COLDATA can be reset into the default state LArASIC and ColdADC can be reset by COLDATA. After the reset the chips come up in the default state	Pass/Fail
ColdADC reference voltage measurement & scan	Measure the four reference voltages for both the bandgap reference block and the CMOS reference block (the four voltages to be measured are: VREFP, VREFN, VCMI, and VCMO). A few scan points to assure the reference voltages are adjustable	Voltages of references should be in required range and adjustable
LArASIC bandgap & temperature measurement	Measure the bandgap reference voltage Measure the embedded temperature sensor voltage	The values are in the acceptable range
LArASIC DAC measurement	Measure the 6-bit DAC voltages with 64 settings	DNL/INL are in the acceptable range
Pulse response	The FEMB accepts the external calibration pulse from WIB. All channels should have a consistent response. Two combinations will be measured (single-ended or differential interface between LArASIC and ColdADC)	Pass/Fail

FEMB QC Items (Performance measurement)

Item	Description	Expected output
Noise & pedestal measurement	Noise performance will be evaluated with a 150 pF capacitive load. LArASIC will be set to 14 mV/fC gain and 500 pA leakage current with 8 combinations (900mV/200mV baseline, 4 peaking times) The single-ended interface between LArASIC and ColdADC will be in use	Noise & pedestal in the acceptable range
Gain measurement (coarse)	The single-ended interface between LArASIC and ColdADC will be in use Gain measurement is done by the ASIC embedded calibration pulser 32 combinations, a coarse measurement is preferred (4 gains x 4 peaking times x 2 baselines)	Gain under each configuration should be in the acceptable range
Linearity and range measurement	The single-ended interface between LArASIC and ColdADC will be in use Linearity measurement is done by the ASIC embedded calibration pulser. LArASIC is configured with 14mV/fC gain, 2 us peaking time, 200 mV baselined and thus calibrated by 64 charge points generated by ASIC internal DAC.	<1% non-linearity at required linearity range (100 pC)

FEMB QC Report

- The FEMB QC procedure (test script) has implemented
 - Most analysis scripts are nearly completed, plot display to be unified
 - PASS/FAIL criteria is being added into analysis script
 - QC data can save directly to NFS (Network File System)

SE_200mVBL_14_0mVfC_2_0us

Power Consumption = 7.575 W

name	V_set/V	V_meas/V	I_meas/A	P_meas/W
BIAS	5.0	5.0	0.0	0.0
LArASIC	3.0	2.935	0.421	1.236
ColdDATA	3.0	2.974	0.229	0.681
ColdADC	3.5	3.433	1.648	5.658

DIFF_200mVBL_14_0mVfC_2_0us

Power Consumption = 8.352 W

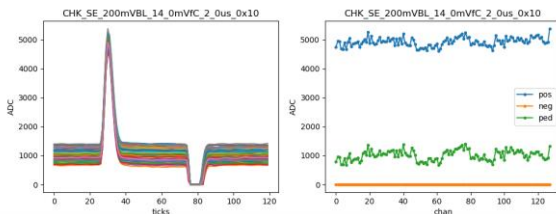
name	V_set/V	V_meas/V	I_meas/A	P_meas/W
BIAS	5.0	5.0	0.0	0.0
LArASIC	3.0	2.871	0.705	2.024
ColdDATA	3.0	2.973	0.226	0.672
ColdADC	3.5	3.432	1.648	5.656

SE_SDF_200mVBL_14_0mVfC_2_0us

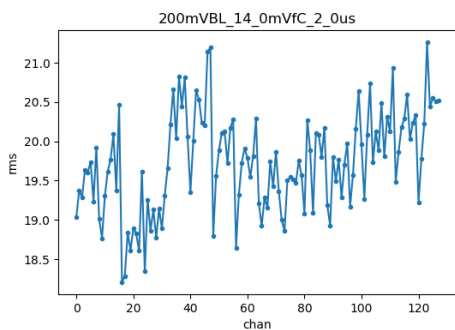
Power Consumption = 8.162 W

name	V_set/V	V_meas/V	I_meas/A	P_meas/W
BIAS	5.0	5.0	0.0	0.0
LArASIC	3.0	2.888	0.632	1.825
ColdDATA	3.0	2.973	0.229	0.681
ColdADC	3.5	3.432	1.648	5.656

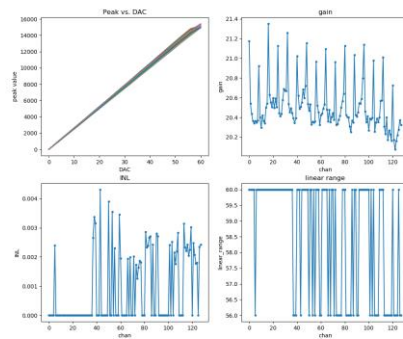
Power consumption for different configurations



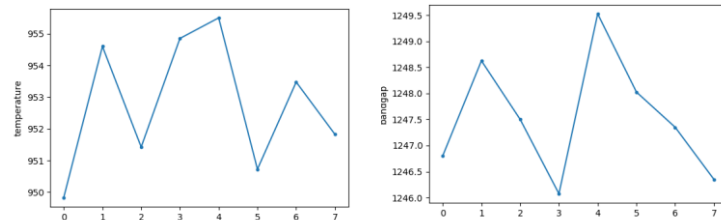
Pulse response (32 combinations, to be extended)



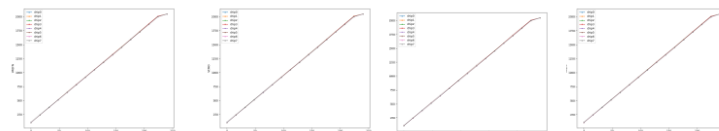
Noise Check (4 x 4 x 2 combinations)



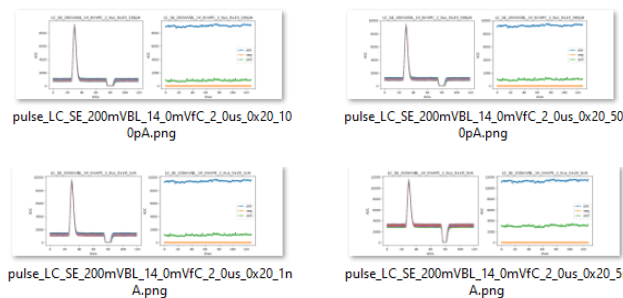
Calibration



LArASIC bandgap / temperature / DAC monitoring



ColaADC V_{REFP} / V_{REFN} / V_{CMI} / V_{CMO} monitoring



LArASIC 100pA / 500pA / 1nA / 5nA leakage current settings

QC Management

- QC activities in all sites will be monitored and led by the TPC electronics consortium
 - Maintain central repo for the testing software
 - Each site admin updates the controlled system deployment in coordination with local operators
- All test sites share use the same hardware setup (both DAT and RTS) and the same QC procedure
- Identifier
 - [EDMS-2505353](#) specifies a scheme for identifying all the detector components
- ASIC/FEMB handling
 - ASIC belongs to MSL level 3
 - Follow Standard IPC/JEDEC J-STD-033
 - Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices
- QC data storage
 - The hardware database is getting close to a useable state
 - Define what data needs achieved to form the component template for the hardware DB. The component template just defines what data is associated with each object.
 - A test summary in a data interchange format (e.g. HDF5, CSV, JSON) will be stored in the central hardware DB
 - All the raw data from testing is achieved locally / Fermilab database

Summary

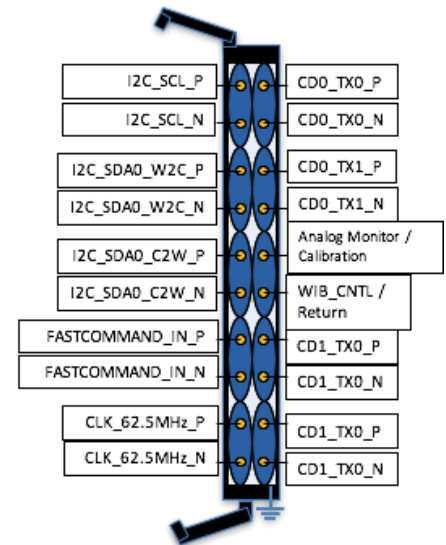
- 3-ASIC FEMB meets DUNE requirements
 - No inactive CE channel before installation
 - ENC < 1000 e⁻
 - Non-linearity < 1%
 - Channel to channel crosstalk < 1%; with a goal of < 0.1 %
 - Power consumption < 50 mW/ch
- The production experience from ProtoDUNE-II HD&VD CE benefits DUNE CE QA/QC
 - Yield of FEMB can be and should be improved towards thousands of FEMB production
- 5-level qualify control is explored
 - **Component:** LArASIC, ColdADC, COLDATA, cold cables, connectors, commercial parts
 - **Board: FEMB (Warm & Cold QC)** , WIB, PTC, PTB, Flange, Patch Panel
 - **Assembly: CE box**, WIEC
 - **Reception**
 - **Integration / Installation / Commissioning**
- QC management and data storage is being detailed in the coming months

backups

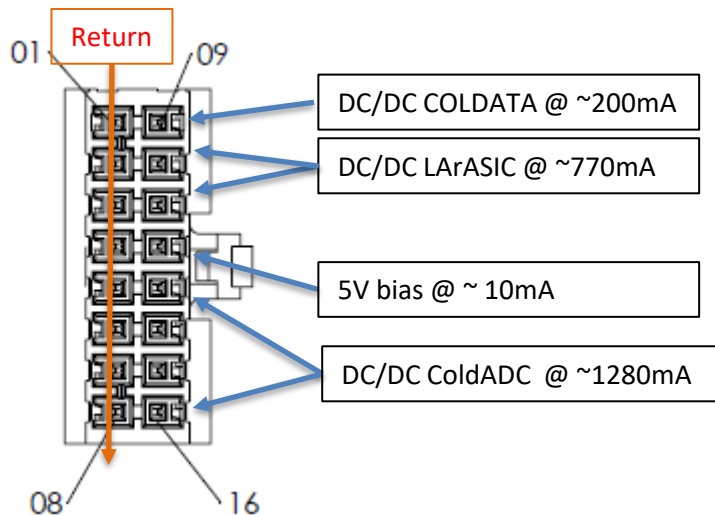
Scheme of Data Interface

- FEMB-HD: Samtec ASP-191865-03 connector
- FEMB-VD: MiniSAS connector
- Assignment
 - 1.25 Gb/s TX data link (4 pairs)
 - 2 pairs for each COLDATA
 - I2C link (3 pairs)
 - SDA_W2C: standard LVDS
 - SDA_C2W: standard LVDS
 - SCL: standard LVDS
 - 62.5MHz clock (1 pair)
 - signal from WIB shared by 2 COLDATA chips
 - FAST COMMAND (1 pair)
 - signal from WIB shared by 2 COLDATA chips
 - Analog monitor/calibration (1 pin)
 - function is selected by FEMB configuration
 - WIB_CNTL/GND (1 pin)
 - The WIB_CNTL signal is used to control a CMOS switch on the FEMB to generate a calibration pulse or it can be tied to ground on the WIB

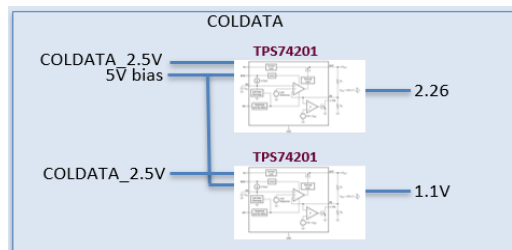
Signal name	Type	# of Pairs	IO Standard
4xData Links	Differential	4	LVDS
I2C_SCL	Differential	1	LVDS
I2C_SDA0_C2W	Differential	1	LVDS
I2C_SDA0_W2C	Differential	1	LVDS
FASTCOMMAND	Differential	1	LVDS
CLK_62.5MHz	Differential	1	LVDS
Analog Monitor / Calibration	Single ended	½	Analog
WIB_CNTL or GND	Single ended	½	1.8V CMOS or Return



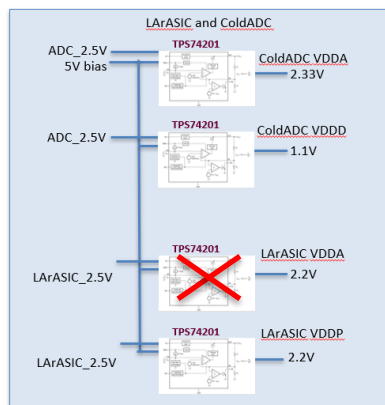
Power Scheme



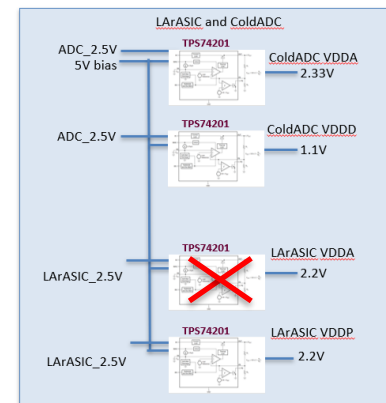
- All regulators share the same bias supply
- RC filters are applied for all LDO outputs
 - Voltage drops are compensated in order to get desired values
- LArASIC VDDA and VDDP are tied together
 - Slightly better noise performance
 - Can be turned ON/OFF by COLDATA IO



Left Side Regulators



Right Side Regulators



FEMB-HD: Findings from post-assembly checkout

- 8 of 100 FEMB-HD didn't not pass post-assembly checkout

IO-1826-1B

Batch	FEMB	Classify	Description
1	12	component defect	L126, L127 use broken 0 Ohm resistors
2	8	ColdADC	CH15 of ColdADC (U26, No. 00123) shows ~k Ohm input impedance (~1 MOhm nominal)
2	11	Assembly	soldering issue, two pins for data transmission shorts
2	7	Assembly	An open pin of Data connector P4
3	51	COLDDATA	U1, no SCL output from U1 (primary COLDDATA) to other chips
3	55	Assembly	U27 (LDO TPS74201) was populated in wrong direction
3	74	component defect	R168 for U12 (LDO) voltage divider was broken
3	78	COLDDATA	VDDD to GND of (U1) ~3 Ohm

Batch1: 25pcs, batch 2: 30 pieces, batch 3: 45 pieces

FEMB-HD: Findings observed from QC

- 10 FEMBs failed in the 1st run of QC shown in the table below

- Total 16 FEMBs didn't pass checkout & QC, and need rework

IO-1826-1B

Batch	FEMB	classify	SN	when observed	description
1	12	LDO TPS740201		LN2 (Cold)	U12 (LDO: TPS70401) can't work at LN2 properly. At warm, it outputs 2.33V as expected. At cold, it outputs 1.85V
2	15	COLDDATA	U1	After a RT-LN2 thermal-cycle	U1 (Primary) SPI failed. Can't configurate itself and other chips, Pin#112 (I2C SCL) of U1 doesn't show clock signals
2	24	COLDDATA	U1	LN2 (Cold)	U1 (Primary) is sensitive to temperature. CONFIG_PLL_BAND – Register 65 (0x41) default value 0x20 can't work at cold. Values good for cold operation: 0x1B ~0x1E, 0x21-0x2B
2	27	LArASIC	625	LN2 (Cold)	CH14 (U3, SN: 625) appears abnormal high RMS noise at cold (except 100pA leak current setting) (<i>Re-visit the chip QC test results, looks fine</i>)
2	19	ColdADC	4-020	LN2 (Cold)	U26 (4-005). It work fine randomly after each power cycle. If it works, then it works until next power cycle. Good at RT
2	26	ColdADC	4-005	LN2 (Cold)	U26 output abnormal data at cold. Good at RT
3	48	LArASIC	1387	RT	CH15 of the ASIC: BL 200mV shows high ADC count, abnormal x2 baseline voltage (<i>The chip QC test found the chip already failed at warm. The chip was put in the PASS tray by handing mistake</i>)
3	55	COLDDATA	U2	RT	U2 (Secondary) is sensitive to temperature, can't output good data at warm. At cold, it works fine.
3	75	COLDDATA	U1	RT	At warm: unstable data. At cold: in order to get ColdADC 0&1 data, Page 5, 0x48 writes 0x00 or 0x01.
3	83	LDO TPS740201		LN2 (Cold)	U12 (LDO: TPS70401) can't work at LN2 properly. At warm, it outputs 2.33V as expected. At cold, it outputs 1.9V

FEMB-VD: FEMB QC Test Results

- 1C FEMB (15 pieces) QC test result

Batch	FEMB	Failure Modes	Observed	Description
1C	103	Assembly	RT	U21(FE) was wrongly populated with ColdADC
1C	106	LArASIC	LN2	One FE channel has high RMS noise
1C	111	ColdADC	LN2	8 channel (a ADC core) output unstable data

- 1D FEMB (60 pieces) Post-assembly checkout

Batch	FEMB	Failure Modes	Description
1	07	Assembly	U20 (ColdADC) has two pins shorted together
1	70	Assembly	FE-ADC CH02: open caused by poorly assembled 0201 resistor
1	22	Assembly	FE-ADC CH83, 84: open caused by poorly assembled 0201 resistor
2	47	Assembly	CH17 (0201 resistor is open)
2	69	COLDDATA	low impedance (< 7 Ohm) was observed in U1 (COLDDATA) pin 110 (VDD_LArASIC)
2	80	COLDDATA	Low impedance (short) observed between power pins to ground pins

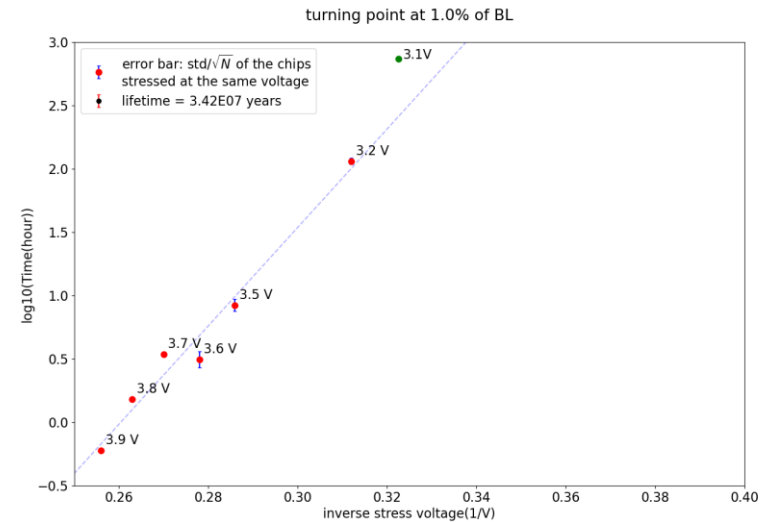
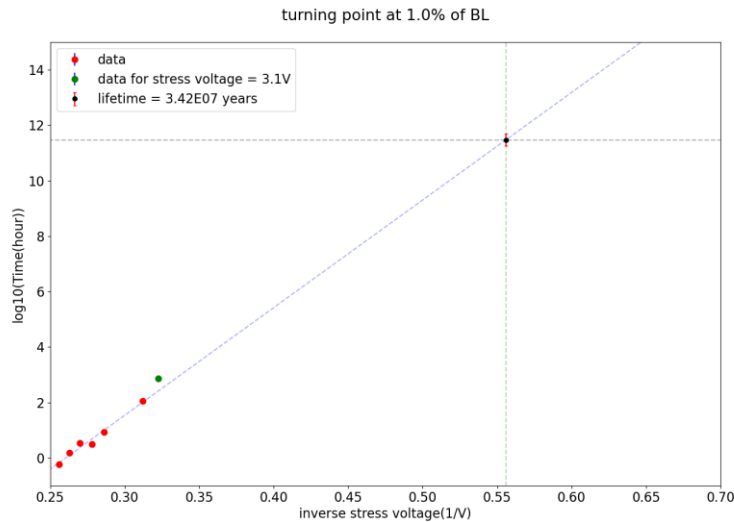
- 1D FEMB (60 pieces) QC results

Batch	FEMB	Failure Modes	Observed	Description
2	17	Assembly	RT	CH108 shows lower pulse amplitude with DIFF interface. Open connection of N caused by 0201 resistor
2	52	LArASIC	LN2	A channel doesn't have pulse response at cold
2	63	LArASIC	RT	U23 (LArASIC) shows noise slightly lower than other chips at both RT and LN2, it should be replaced for checking
1	73	LArASIC	LN2	Baseline/noise of all 16 channels higher than other chips
2	68	COLDDATA	RT	Abnormal data. Sensitive to temperature, can't output good data at warm
2	30	COLDDATA	RT	Unstable data at warm

LArASIC Lifetime Projection

2. Have life-time tests of all ASICs been done?

- LArASIC PRR review on Mar 7-8, 2022 has responded to this question.
 - <https://indico.fnal.gov/event/53072/timetable/#20220307>
 - <https://edms.cern.ch/document/2314428/2>
- LArASIC is designed with HCE tolerance
 - All transistors in LArASIC are well below nominal voltage of 1.8V and at low I_{sub}
 - All n-channel devices are either 270 nm or longer, at voltages 1.5 V or lower
 - Reduce V_{ds} by 6%, for each order of magnitude margin in the lifetime
- Two chips stressed under 3.1 V for over 900 hours
 - No significant degradation observed so far (< 1%), still under stressed
 - 3.1V down to 1.8V, there is over 8 orders of magnitude, predicted lifetime is $\sim 1 \times 10^7$ years
- Oxide damage
 - $\geq 3.2V$ is much higher than the maximum voltage ($\sim 2V$) allowed by TSMC 180 nm process, the degradation could be caused by oxide damage
 - If degradation is caused by oxide damage, LArASIC lifetime will be longer than the below projection plots.

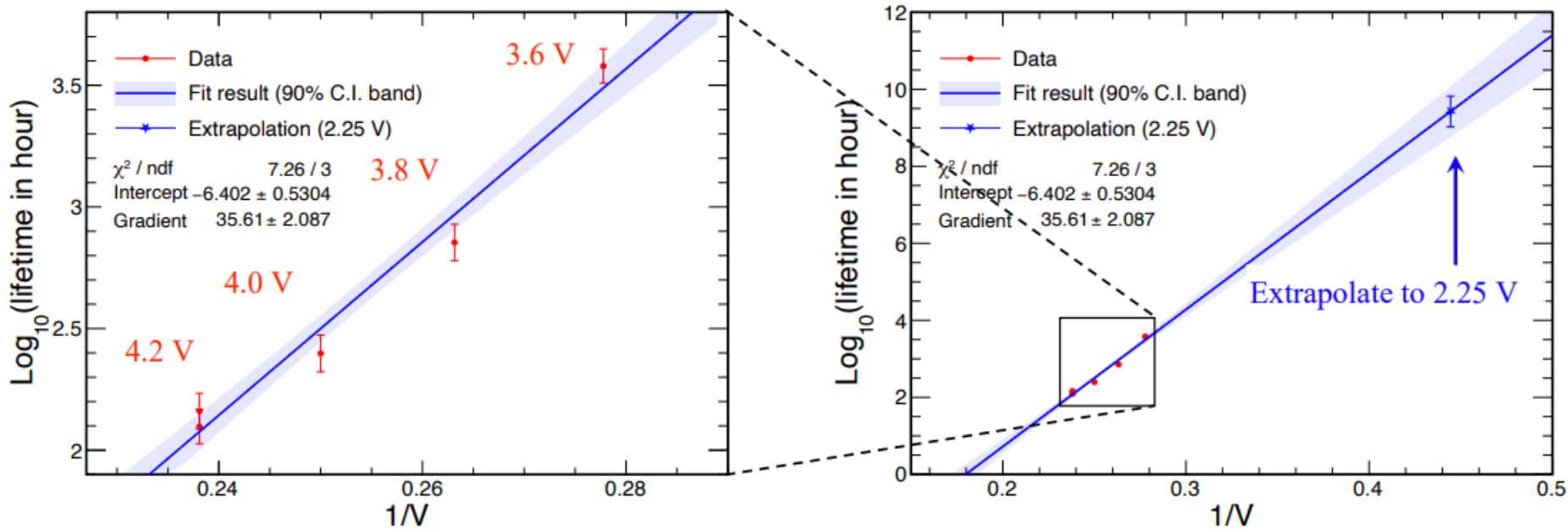


Plotted by Rado Razakamiandra

ColdADC Lifetime Projection

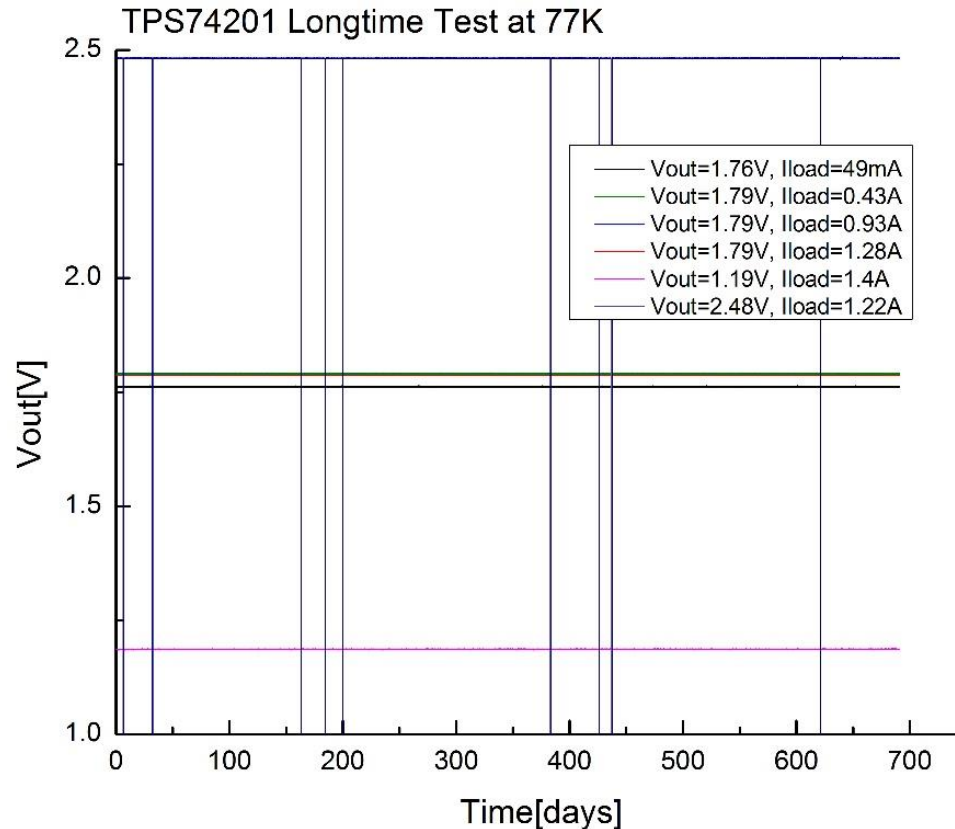
Lifetime

- No obvious degradation of the performance (ENOB, DNL, INL) after hundreds of hours testing
- Given no ADC failed the stress test at the moment, a conservative lower bound on lifetime is extracted by using "current drop of 1%" as the failure threshold (note: ADC performs fine at 1% current drop)
- Use the difference between two measurements stressed at 4.2 V as the uncertainty from chip-to-chip. Use the error output from the fitting as the uncertainty of the measurements. Treat them as uncorrelated
- It gives a lifetime of 3.02×10^5 years at 2.25 V



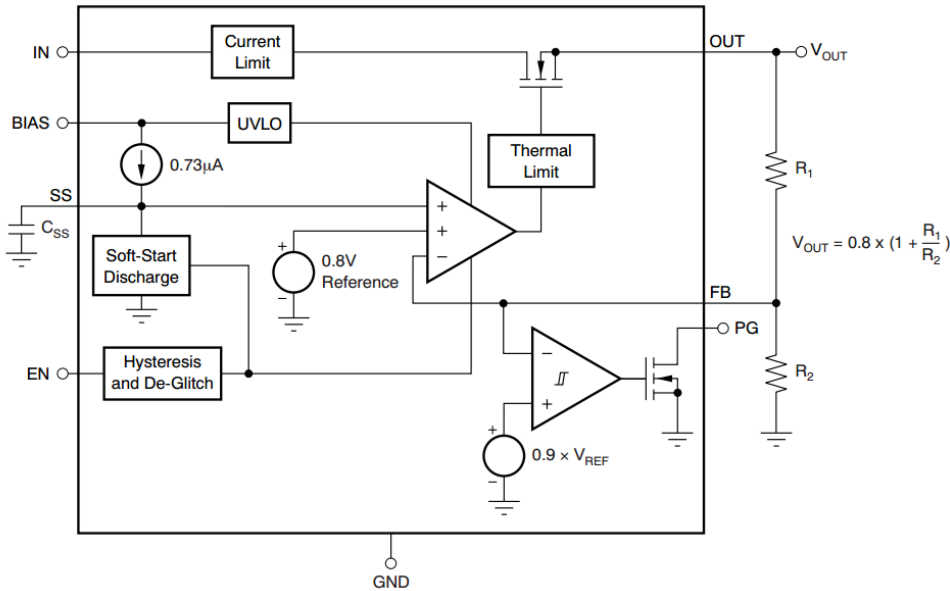
TPS74201 in LN2

Regulator at 77K-Two Year Continuous Non-stress Test

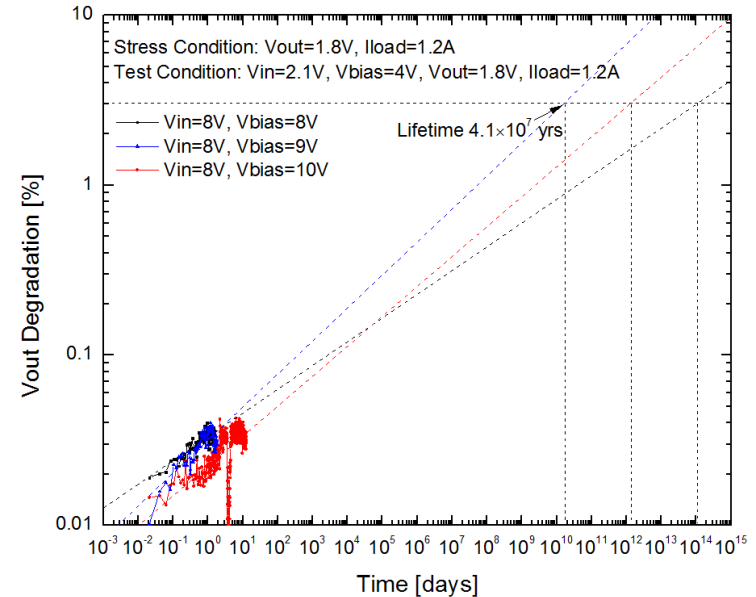


A 2-year continuous non-stress test of six regulators biased at different operating condition has been performed. The output voltage of the regulator is stable over the full range of two years. Voltage drops are due to power glitch (power supply or computer shut down), movement of experiment setup, etc.

Regulator Stress Test



Block diagram of TPS74201 from the datasheet. Pin IN is the input voltage of the regulator while BIAS is the bias voltage for the internal logics. The absolute maximum voltage for both voltages is 6V.



Regulators are stressed under different voltages. For criteria of 3% degradation, the regulator under stress ($V_{in}=V_{bias}=8V$) already exhibits a lifetime of more than 10^7 years. Therefore, the operation of the regulator under normal operation ($V_{in}=2.1V$, $V_{bias}=4V$) at 77K is not of concern.

Quality Assurance (1)

- The QA plan developed here is consistent with the principles discussed in chapter 9 of DUNE far detector technical design report Volume III, DUNE far detector technical coordination
 - The goal of the QA plan is to **maximize the number of functioning readout channels** in the detector that achieve the performance specifications, particularly on noise.
 - Apart from the number of channels, the most important difference between ProtoDUNE-I and DUNE is **the projected lifetime of the detector**.
- Cold Electronics
 - **128-CH Front-End Mother Boards (FEMB) installed on the APAs (FD1-HD) and bottom CRPs (FD2-VD)**
 - Cold cables
 - FD1-HD: Samtec 9 m/22 m data cable, 9 m/22 m power cable
 - FD2-VD: Samtec 27 m data cable, 2.5 m miniSAS cable, 27 m and 2.5 m power cable; CRP cable patch panel
 - Feed-through assembly
 - Flange assembly
 - Warm Interface Electronics Crate
 - Warm Interface Board (WIB)
 - Power and Timing Card (PTC)
 - Power and Timing Backplane (PTB)

Quality Assurance (2)

- Design files assurance
 - All **FEMB design** files, including schematics, layout, BOM, and other relevant files, must be **finalized and uploaded to CERN EDMS before the production phase begins**.
 - An initial design validation should be performed to confirm the correctness.
 - After that, the design files should be locked, and any modification should be reviewed and approved by the CE consortium.
- **The main design files include**
 - ASIC design documentations (design specifications, production records, datasheets, user manuals)
 - Original schematics files and schematics in pdf format
 - Original layout files
 - PCB fabrication package, including but not limited to gerber and drill files
 - Assembly package, including but not limited to gerber, BOM and position files
 - Mechanical drawings, including cold cables, flange, crate, and etc.
 - BOM and assembly note (requirement)
 - Other relevant files like a list of substitutes, assembly quote or PCB fabrication quotes

Quality Assurance (3)

- Procurement of parts
 - The production of FEMBs requires many large procurements that must **be carefully planned to avoid delays**. The procurement of ASICs (LArASIC, ColdADC and COLDATA) is included in the ASIC QA/QC plan (<https://edms.cern.ch/document/2604783/1>). For all other components, several vendors will bid on the same package. Depending on the requirements of the funding agency and of the responsible institution, this may require a lengthy selection process. **Vendors must be certified to meet a certain quality standards** required by the responsible institution.
 - For example, a BNL-QA-101 form is applied to all vendors if the purchase order is made by BNL Procurement & Property Management Division (PPM).
 - PCB fabrication and assembly will be performed by external companies that **meet the quality standard** required by DUNE and the responsible institution. **A trial run of a small amount should be performed before the large purchase.**

Quality Assurance (4)

- QC activities in all sites will be monitored and led by the TPC electronics consortium
 - Maintain central repo for the testing software
 - Each site admin updates the controlled system deployment in coordination with local operators
- All test sites share use the same hardware setup (both DAT and RTS) and the same QC procedure
 - All ASICs to have a unique identifier on the package, COLDATA chips will also have E-fuses burnt during the QC process
 - Plan on testing all ASICs both at room temperature and in LN2 prior to installing them on the FEMBs
 - All ASICs to be place into sockets by pick and place robotic system
 - Test board design is inspired by FEMB design and by test boards used for ProtoDUNE and for initial testing of ASICs during their development