

DUNE FDR: FD2 Bottom Drift Electronics WIB and Cold Cables

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Brookhaven National Laboratory

05/16/2023

Outline

[Charge Question: #4, 7, 9]

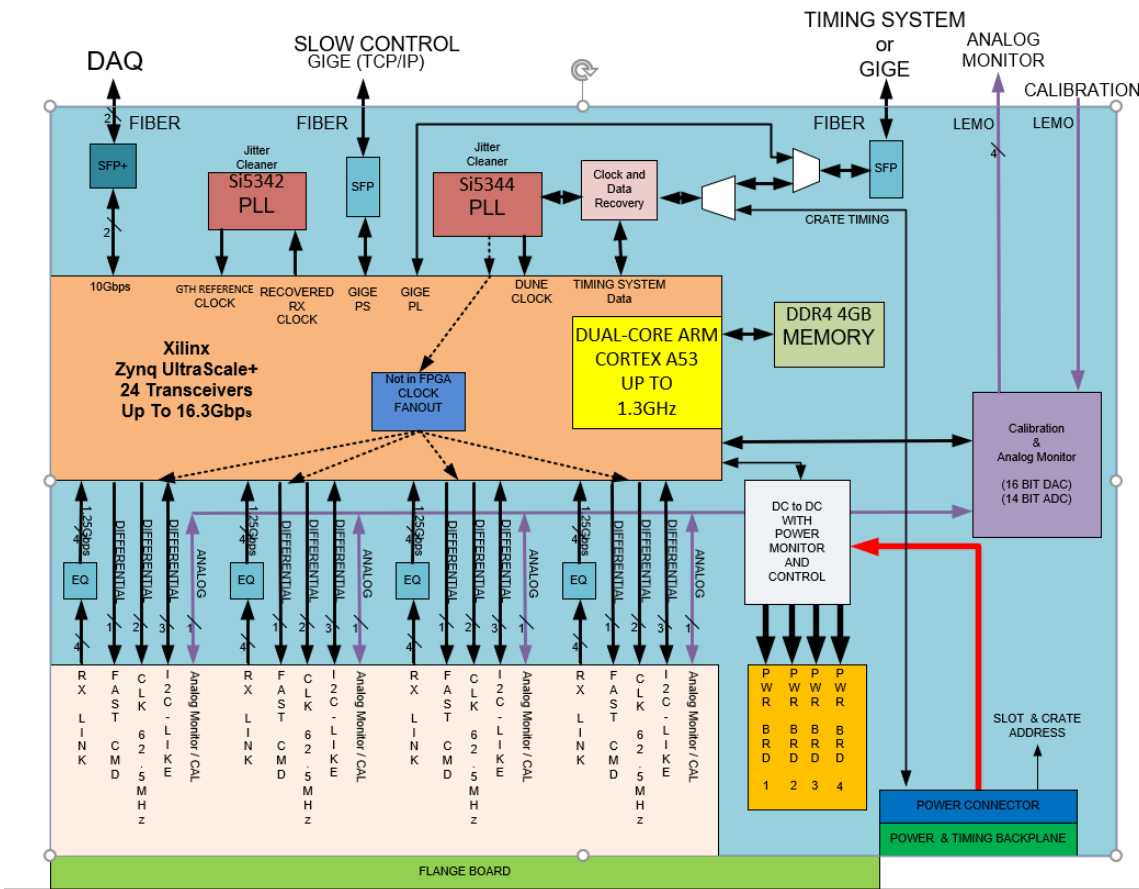
- Introduction
- Warm Interface Board
 - Final Design
 - QC Test and Operational Experience
- PTB, Flange Board, **CRP Patch Panel** (FD2-VD specific)
 - Final Design
 - Operational Experience
- **Cold Cables** (FD2-VD specific)
 - Final Design
 - QC Test and Operational Experience
- Response to Charge Question

Introduction

- FD2-VD BDE design is mostly based on the FD1-HD TPC electronics design, with few exceptions
 - FEMB has a different data connector
 - Please see Shanshan's talk for more details
 - Cold cables have different length plus a CRP patch panel
 - Well motivated by the fact
 - BDE installation will take place in CRP factory
 - APA cold electronics installation will take place at SURF
- The support document for FD1 TPC Electronics FDR on September 29, 2022 is a good reference
 - <https://edms.cern.ch/document/2782297/>

Warm Interface Board

- WIB requirements are documented
 - <https://edms.cern.ch/document/2341138/>
 - Both hardware and firmware documents

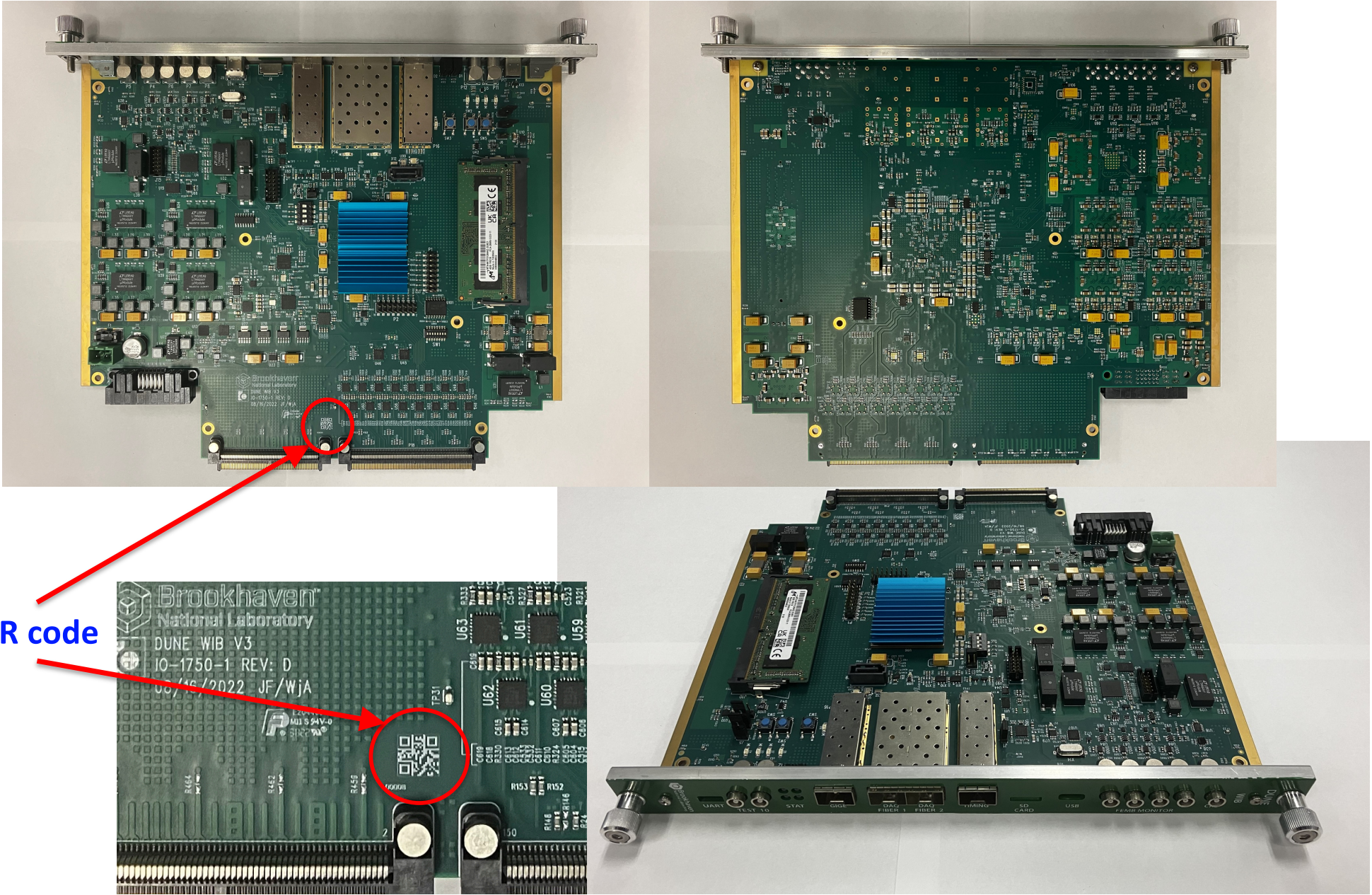


- Receive data 4 FEMBs through cold cables
- Send data to DAQ system through fiber optical links
- Receive power and timing information from PTC through PTB
- Distribute power, timing and control to 4 FEMBs through cold cables
- Slow control interface through GbE
- Monitoring and calibration interface for diagnostic

WIB Design Evolution

- The WIB with Zynq UltraScale+ MPSoC ZU6CG has been developed since 2019
- Prototype design ([WIBv2: IO-1750-1/-1A](#)) in 2019/2020 has been tested extensively
 - Bench test and integration test at BNL
 - Firmware development at Florida and Penn
 - Integration test with ICEBERG at Fermilab
- Final design ([WIBv3: IO-1750-1B/-1C/-1D](#)) in 2022 for APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN
 - Design changes from WIBv2 to WIBv3 described in the FDR support document (<https://edms.cern.ch/document/2782297/>)
 - Final design files: <https://edms.cern.ch/document/2712914/>
 - Minor updates of WIBv3 to address few cosmetic issues
 - IO-1750-1C: Micro-USB to USB-C; MicroSD socket and location
 - IO-1750-1D: QR code; current monitoring
 - Discussion of options to support powering off individual WIB by adding I2C buffer
 - Minor revision is foreseen before PRR
- **FPGA firmware is fully compatible among WIBv3 boards**

WIBv3 IO-1750-1D



QR code

WIB QC Test

- QC plan is documented
 - <https://edms.cern.ch/document/2815079/>
- WIB QC test procedure has been developed
 - WIBv3, 4x FEMB and a WIB adapter board form the QC test stand
 - Test of 1 WIB takes about half hour to go through the full QC procedure
 - QC test script is being optimized to improve the efficiency
- QC test of 15 WIBs recently
 - 10 boards passed the first QC
 - 5 passed QC after assembly issues and defective chip are fixed

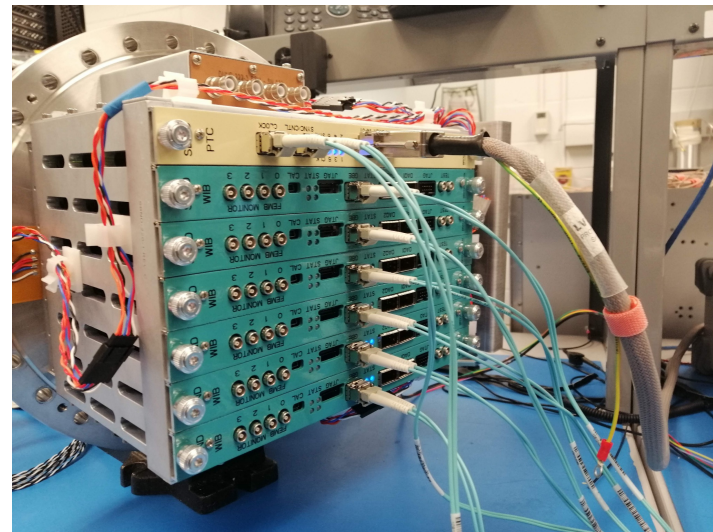
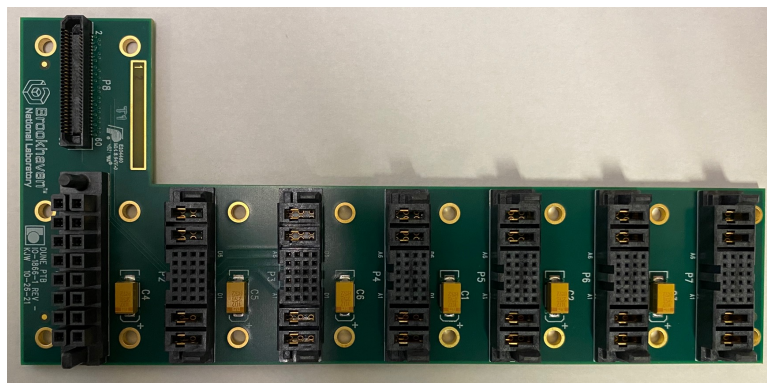
WIB_QC_test						
	Initial Check	Power Rail	General Interfaces	FEMB Control	Timing	SFP IBERT
	Power Measurement	Initial Ports <ul style="list-style-type: none"> Disconnect the power Connect the LT controller Check Pin Value 	SD Boot	Overview of the whole interface	SI5344 Configuration	IBERT
	Power Record		Operations <ul style="list-style-type: none"> Go_Online PCROM RAM_NVM 	Slow Control <ul style="list-style-type: none"> 1.25 Gbps SFP channel Uart 		FEMB_PWR
	Jumper & adjust SW4			Network <ul style="list-style-type: none"> Anaconda Putty 	FEMB_MON_CAL	1.25 Gbps SFP channel
		Record and Compare Result	Uart <ul style="list-style-type: none"> Standard Port Bond rate: 115200 	Check_FEMB_Channel	Power On Record	

WIB Operational Experience

- WIBv3 has been used extensively for APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN
 - 5 WIBs for APA cold box test
 - 20 WIBs for ProtoDUNE-II-HD
 - 6 WIBs for CRP cold box test
 - 12 WIBs for ProtoDUNE-II-VD
 - Spare WIBs for VST
- ProtoDUNE-II-HD has been read out by WIBv3 through FELIX successfully since 2022
 - APA cold box test has been read out by WIBv3 through FELIX since 2022
 - CRP cold box test has been read out by WIBv3 through FELIX since 2022
 - VST is being used to test WIBv3 Ethernet readout, later to be deployed for ProtoDUNE-II-HD/VD
 - Please see Roger's talk for more details

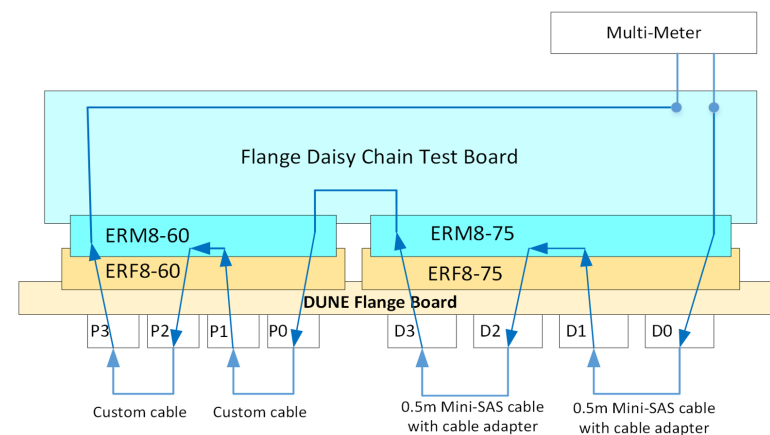
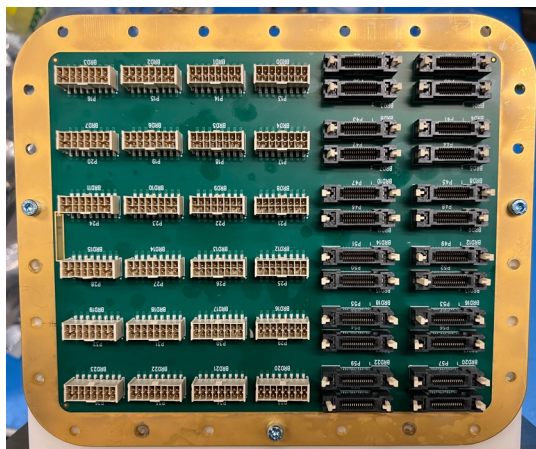
PTB

- Final design of PTB in 2021 for APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN
 - Final design described in the FDR support document (<https://edms.cern.ch/document/2782297/>)
 - Final design files: <https://edms.cern.ch/document/2712915/>
 - Minor design changes from preliminary design for ProtoDUNE-I to support 8 address bits to identify a unique crate address of WIEC in FD
- PTB QC test
 - PTB is a simple board with only passive components, visual inspection is required before it is installed in the WIEC
 - The connectivity of PTB is verified during the final walk-through QC test of the feed-through and WIEC assembly before the shipment
- PTB operational experience
 - PTB assembled in WIEC has been used extensively for APA (1)/CRP (1) cold box tests and ProtoDUNE-II HD (4)/VD (2) at CERN



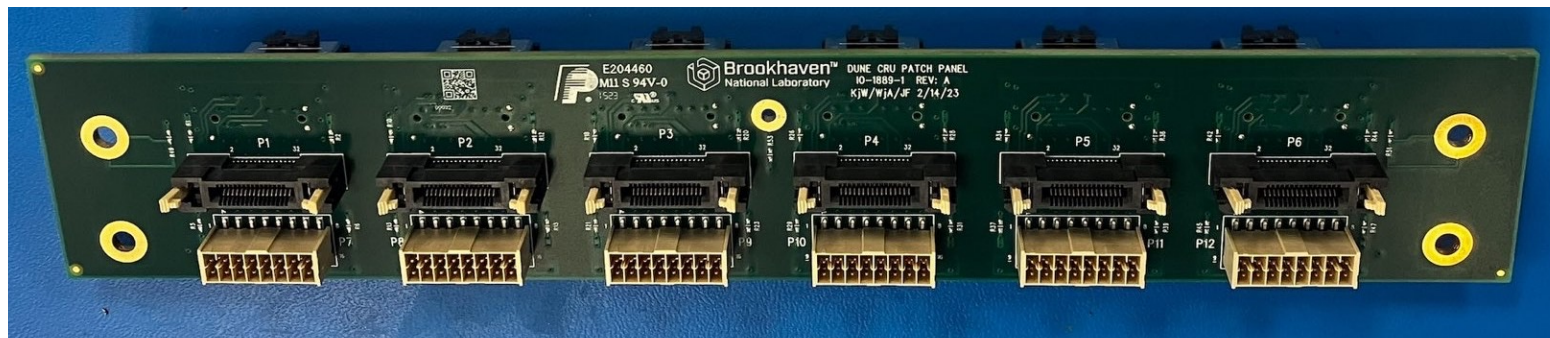
Flange Board

- Final design of flange board in 2021 for APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN
 - Final design described in the FDR support document (<https://edms.cern.ch/document/2782297/>)
 - Final design files: <https://edms.cern.ch/document/2712916/>
 - Design changes to accommodate new cold cable connectors, and adjustment of locations for WIB connectors
- Flange board QC test
 - After the visual inspection, each flange board will perform the continuity test with a DUNE flange daisy chain test board (IO-1869-1) before it is installed on the flange
 - The connectivity of flange board is verified during the final walk-through QC test of the feed-through and WIEC assembly before the shipment
- Flange board operational experience
 - Flange board assembled in WIEC has been used extensively for APA (1)/CRP (1) cold box tests and ProtoDUNE-II HD (4)/VD (2) at CERN



CRP Patch Panel

- Final design of CRP patch panel in 2022 for CRP cold box tests and ProtoDUNE-II VD at CERN
 - Final design files: <https://edms.cern.ch/project/CERN-0000242190>
- Patch panel QC test
 - Patch panel is a simple board with only passive components, visual inspection is required as the first step
 - The connectivity of patch panel is verified before and after thermal cycles in LN2
- Patch panel operational experience
 - 8 panel panels have been mounted on CRP4/5 and used extensively for CRP cold box tests at CERN
- Please see Manhong's talk for mechanical assemblies of WIEC with flange and CRP patch panel



Cold Cables

- BDE cold cables have 2 segments
 - 2.5 m cables from FEMB to CRP patch panel
 - 27 m cables from CRP patch panel to signal feed-through flange
- FEMBs, 2.5 m cables and panel panels will be mounted on CRP and tested in CRP factory, before the full CRP assembly is shipped to SURF
- 27 m data cable and 27 m power cable drawings are shown below
 - Data cable is made by Samtec without mounting tabs on connector as FD1-HD
 - Power cable is assembled by a local vendor with extrusions from Allied Wire

REVISION

1	ISSUE	FORWARD
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HDR SETUP OPTION:
ECCDP-01 BANK

THIS PRODUCT MANUFACTURED WITH LEAD-FREE PROCESSING

TABLE 1

PART #	"A"	"B"	"C" #2	ITEM 3
HDR-227794-01	884.25 (25.000.0)	884.89 (25.016.2)	78 (19.84 (504.0))	SUB-COS-199713-05-03-01-TB
HDR-227794-02	1023.02 (26.000.0)	1028.26 (26.016.2)	81 (20.34 (514.0))	SUB-COS-199713-05-04-01-TB
HDR-227794-03	1082.99 (27.000.0)	1083.63 (27.016.2)	84 (20.83 (524.0))	SUB-COS-199713-05-05-01-TB

NOTES:

- ROCK CARBON ASSEMBLY IS NOT STANDARD.
- REPRESENTS A CRITICAL DIMENSION.
- PARTS TO BE PROCESSED PER SAMTEC HDR WORKMANSHIP STANDARD.
- ALL ASSEMBLIES TO BE 100% ELECTRICALLY TESTED.
- ALL ASSEMBLIES TO BE 100% PREP TESTED AT 200V.
- ITEM 5 TO BE PLACED ON ITEM 3 AS SHOWN. ITEM 5 TO CONTAIN: LINE 2 - PART NUMBER "XXXXXXXXXX" LINE 3 - SHOP ORDER NUMBER "XXXXXX"
- FOR SUB-ASSEMBLY AND FINISHED GOOD PACKAGING REQUIREMENTS, REFERENCE SAMTEC PACKAGING MANUAL.
- REFER TO PREP SPEC PDF FOR CABLE PREP DIMENSIONS.
- ASSEMBLY USES PREP SPEC: 000-000-000 PREP.

ACCEPTANCE DRAWING LISTED

ITEM NO.	PART NUMBER	DESCRIPTION	QUANTITY	MATERIAL
1	S-PCB-112432-HDR-01	SUB ASSEMBLY	2	SUB ASSEMBLY
2	SUB-COS-199713-05-XX-01-TB	TWNA X CABLE	2	SUB ASSEMBLY
3	CCS-147886-02-PP	CLOTH TAPE	2' X 2' EA	ACETATE CLOTH
4	HDRL-11	LABEL	2	SELF LAMINATING VINYL
5	CCS-193086-01	EPOXY	4 PLCS	EPOXY

DO NOT SCALE DRAWING SHEET SCALE: 1:1

DESCRIPTION: CUSTOM HDR CABLE ASSEMBLY

DATE: HDR-227794-XX-ECCDP

BY: ANDREW C 6/10/2022 SHEET 1 OF 2

REV	REV NO.	DESCRIPTION	BY	DATE	CHK	APP
---	---	INITIAL RELEASE (based on DCCB102_25M REV.C)	JF	3/30/2023	MZ	MZ

PAIRS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
WIRE	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK
WIRE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE
WIRE	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK
WIRE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE
WIRE	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK	BLACK
WIRE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE	WHITE

DETAIL A SCALE 4:1

NOTES: Unless otherwise specified:

- 5 PARTS TO BE PACKAGED IN BUBBLE BAGS.
- ASSEMBLY TO BE ELECTRICAL TESTED INCLUDING HI-POT TEST @ 1000 VOLTS DC.
- REFER TO CRIMP SPECIFICATIONS PRINT FOR CRIMP AND STRIP DIMENSIONS, TOLERANCES, TOOLING, AND ITS REQUIREMENTS.
- ACETATE CLOTH TAPE TO BE APPLIED EVERY 0.66 m (1.87'). SEE DRAWING.
- TWISTED PAIR CABLE ASSEMBLY LENGTH: 27 m (88.42') -0.1/+2%

REVISIONS:

REV	REV NO.	DESCRIPTION	BY	DATE	CHK	APP
1	1	INITIAL RELEASE (based on DCCB102_25M REV.C)	JF	3/30/2023	MZ	MZ

ITEM 3

ITEM	QTY	PART NAME / DESCRIPTION	TYPE	MATERIAL	MASS (kg)	HEIGHT (mm)	DRAWING / PART NUMBER
4	59	ACETATE CLOTH ELECTRICAL TAPE	PART	SI RUBBER	0.001	0.002	DigitKey_3M158303-ND
3	2	HOUSING WIRE SCKT-IPD1-08-D-X	PART	ZYTEL-NYLON	0.001	0.002	SAMTEC-IPD1-08-D-X
2	8	WIRE-2 CRIMP CONTACTS-BLK-27M	ASSEMBLY		0.191	0.421	SEE NOTES 6 & 7
1	8	WIRE-2 CRIMP CONTACTS-WHT-27M	ASSEMBLY		0.191	0.421	SEE NOTES 6 & 7

APPROVALS:

DESIGNED BY	DESIGNED DATE	DESIGNED FOR	DESIGNED BY	DESIGNED DATE	DESIGNED FOR
ANDREW C	6/10/2022	CUSTOM HDR CABLE ASSEMBLY	ANDREW C	6/10/2022	CUSTOM HDR CABLE ASSEMBLY

APPROVALS:

APPROVED BY	APPROVED DATE	APPROVED FOR	APPROVED BY	APPROVED DATE	APPROVED FOR
ANDREW C	6/10/2022	CUSTOM HDR CABLE ASSEMBLY	ANDREW C	6/10/2022	CUSTOM HDR CABLE ASSEMBLY

DO NOT SCALE DRAWING

APPLICATION: DUNE CE POWER CABLE ASSY 27M

DC ASSEMBLY 1

DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT

DC ASSEMBLY 1

DUNE CE POWER CABLE ASSY 27M

DCCB102_27M

REV: 1.3

DATE: 3/11/23

BY: MZ

CHK: MZ

APP: MZ

SCALE: 2:1

MASS: 6.863

HEIGHT: 1.171

REV: 1.3

DATE: 3/11/23

BY: MZ

CHK: MZ

APP: MZ

SCALE: 2:1

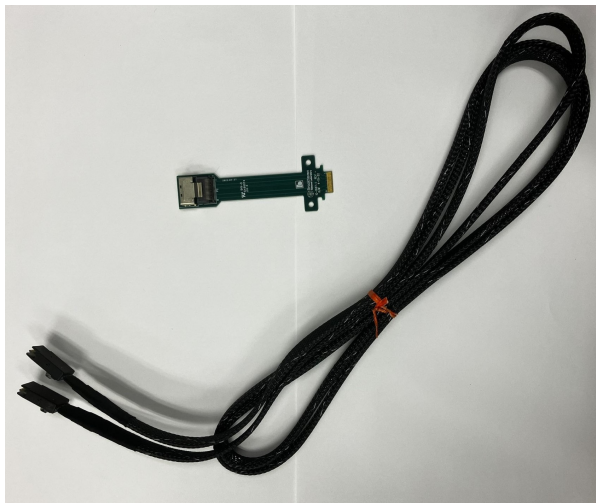
MASS: 6.863

HEIGHT: 1.171

Produced with PTC Creo Parametric 7.0

Cold Cables – QC Test and Operational Experience

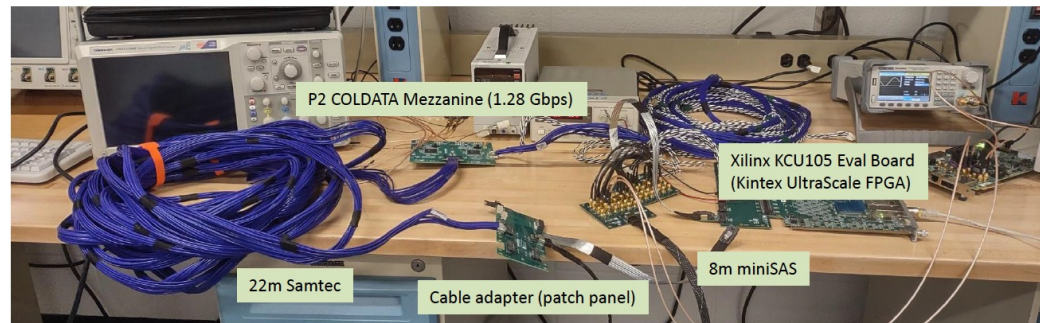
- 2.5 m data cable and 2.5 m power cable pictures are shown below
 - Data cable is MiniSAS cable made by 3M with non-conductive sleeve assembled in house
 - Power cable is assembled by a local vendor with extrusions from Allied Wire
- Cold cables QC test
 - All cables have been QC tested by manufacturer with test reports available
 - 5% cold cables will be sample tested in LN2 from each delivery batch
- Cold cables operational experience
 - CRP4 (24 sets of 2.5 m/25 m cold cables) has been tested in the cold box at CERN
 - CRP5 (24 sets of 2.5 m/25 m power cables, 24 sets of 25 m Samtec cables, 12 sets of 2.5 m/3 m MiniSAS cables) has been tested in the cold box at CERN



Cold Cables – Length

- Recent cable routing studies show 27 m cables are required for FD2-VD
 - Please see Manhong’s talk for details of cable routing
- Baseline is to use 27 m cables for all 80 bottom drift CRPs
 - 27 m cables have been ordered and will be delivered by the end of May, following by the cold box test at CERN
 - BER test in the lab has demonstrated reliable data transmission for 29 m Samtec cables and 8 m MiniSAS cable
 - CRP4/5 cold box tests at CERN have demonstrated reliable data transmission for 25 m Samtec cable and 2.5/3 m MiniSAS cable

BER Test (without Equalizer)



Length	Combination (1.28 Gbps)	BER	RX Pattern
30m	CM + 22m Samtec + ADT + 8m mini-SAS + KCU105	1.073E-14	PRBS 15-bit
29m	CM + 22m Samtec + ADT + 7m Samtec + KCU105	9.555E-15	PRBS 15-bit
37m	CM + 22m Samtec + ADT + 7m Samtec + ADT + 8m mini-SAS + KCU105	2.368E-15	PRBS 15-bit

Note: there is 1m SMA cable that is not taken into account for total length

➤ BER test was done at room temperature, expect to see better performance at cold temperature

Charge Question

- 4. Has the design of the patch panel been finalized, a prototype produced, tested and validated with a CRP?
 - Yes
 - Patch panels have been tested in CRP4/5 cold box tests at CERN successfully
- 7. Can the procurement of the discrete components for the WIBs and the FEMBs be launched?
 - Yes
 - FPGA procurement for WIB has been launched and reviewed in the PRR last week
 - <https://indico.fnal.gov/event/59429/contributions/265863/attachments/166685/222105/WIB-FPGA.20230508.pdf>
 - BOMs for discrete components of WIB and FEMB have been stable since 2022
 - Procurement of discrete components will be handled at BNL, same as the WIB FPGA procurement
- 9. Have the CRP tests with the FEMBs, miniSas cables and the final patch panel been completed?
 - Yes
 - FEMBs, MiniSAS cable and patch panel have been tested in CRP4/5 cold box tests at CERN successfully

Backup Slides

Warm Interface Board

- WIB for ProtoDUNE-I
 - Intel/ALTERA Arria V FPGA 5AGTFD3H3F35I5N
 - 30 WIBs were installed in 6 WIECs to read out 6 APAs for ProtoDUNE-I operation from 2018 to 2020 successfully
- WIB for ProtoDUNE-II HD & VD
 - AMD/Xilinx Zynq UltraScale+ MPSoC XCZU6CG-1FFVB1156E
 - 20 WIBs were installed in 4 WIECs to read out 4 APAs for ProtoDUNE-II-HD in 2022
 - 12 WIBs are being installed in 2 WIECs to read out 2 CRPs for ProtoDUNE-II-VD in 2023
- WIB for DUNE FD1-HD & FD2-VD
 - AMD/Xilinx Zynq UltraScale+ MPSoC XCZU6CG-1FFVB1156E
 - 750 WIBs will be installed in 150 WIECs to read out 150 APAs for FD1-HD
 - 480 WIBs will be installed in 80 WIECs to read out 80 bottom CRPs for FD2-VD

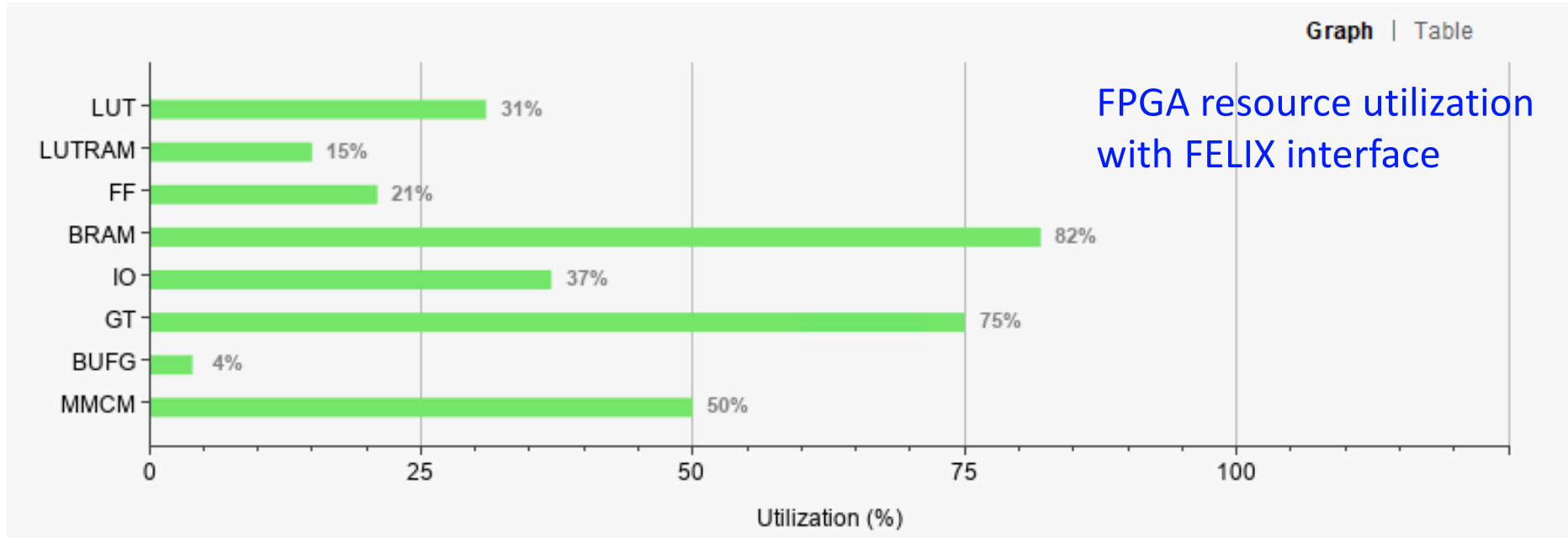
FPGA Selection

- A market survey was carried out after ProtoDUNE-I construction to identify a proper FPGA for DUNE far detector WIB design
- This was discussed during the DUNE collaboration meeting at CERN in January 2019
 - https://indico.fnal.gov/event/16764/contributions/39509/attachments/24693/30763/BN_LCEUpdate.20190129.pdf
- The MPSoC XCZU6CG offers a cost effective alternative, with additional features, e.g. ARM processor, TCP/IP etc.

	WIB	WIB	WIB	WIB	WIB	WIB	WIB
Manufactures	Intel/Altera	Intel/Altera	Intel/Altera	Xilinx	Xilinx	Xilinx	Xilinx
Series	Arria V	Arria 10 GX	Arria 10 GX	Kintex UltraScale	Kintex UltraScale+	Kintex UltraScale+	Zynq UltraScale+
FPGA	5AGTFD3H3F35I5N	10AX032H4F34E3SG	10AX048H4F34E3SG	XCKU040-1FFVA1156I	XCKU9P-1FFVE900E	XCKU11P-1FFVA1156E	XCZU6CG-1FFVB1156E
LEs (K)	362	320	480	530	600	653	469
M10K/M20K	17.26 (M10K)	17.82 (M20K)	28.62 (M20K)	-	-	-	-
Memory Blocks	-	-	-	-	-	-	-
MLAB memory (K)	2	2.7	4.2	-	-	-	-
Max. Distributed RAM (Mb)	-	-	-	7	8.8	9.1	6.9
Total Block RAM (Mb)	-	-	-	21	32.1	21.1	25.1
UltraRAM(Mb)	-	-	-	-	0	22.5	-
DSP	1045	985	1368	1920	2520	2928	1973
GPIO(3.3V/HR/H D+)	544 + 0	48 + 336	48 + 444	104 + 416	96 + 208	48 + 416	120 + 208 + 214
XCVR	24 (10 Gb/s)	24(17.4 Gb/s)	24(17.4 Gb/s)	20 (12.5 Gb/s)	28 (12.5 Gb/s)	20 (12.5 Gb/s) + 8 (25 Gb/s)	24 (12.5 Gb/s)
Size (mmxmm)	35 x35 (F1152)	35 x35 (F1152)	35 x35 (F1152)	35 x35 (A1156)	31x31 (E900)	35 x35 (A1156)	35 x35 (B1156)
Price(\$)	1360.6 for 744-1000 pcs quote	\$1016.00 for 100-1000 pcs	\$1550.00 for 100-1000 pcs	\$1010.14 for 51-300 pcs quote and \$769.45 for 301-1000 pcs	\$1000.04 for 51-300 pcs quote and \$760.84 for 301-1000 pcs	\$1410.97 for 1-499 pcs and \$1074.57 for 500-1000 pcs	\$1050.88 for 36-249 pcs quote and \$799.77 for 250-1000 pcs

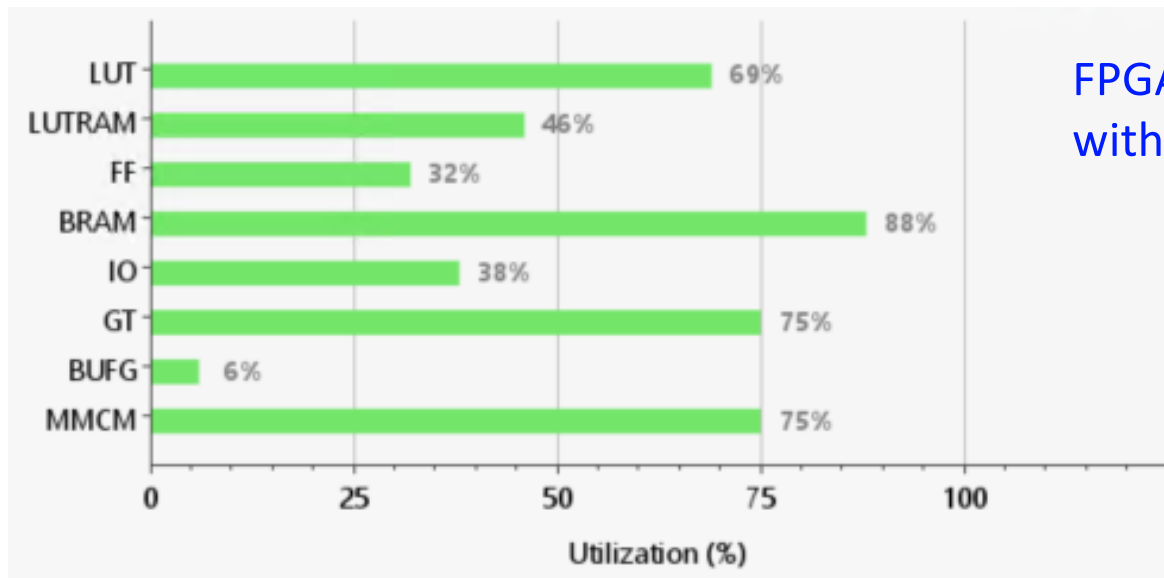
Technical Justification for CD-3A Procurement (1)

- WIB firmware used in ProtoDUNE-II so far has the interface for the FELIX readout, which has been working reliably since 2022
 - The FPGA resource utilization of WIB firmware is quite reasonable, with < 35% LUT usage
 - The usage of BRAM is relatively high, which is due to the ILA cores for debug purposes in the current firmware build



Technical Justification for CD-3A Procurement (2)

- The DUNE DAQ system is migrating to Ethernet based readout in 2023. A preliminary build of the WIB firmware with Ethernet interface is being tested
 - The FPGA resource utilization of WIB firmware is quite reasonable, with < 70% LUT usage
 - The LUT usage can be further optimized with improved design of the data alignment module if necessary
 - The usage of BRAM is relatively high, which is due to the ILA cores for debug purposes in the current firmware build
- **WIB FPGA ZU6CG has sufficient resources for the production needs of DUNE far detector cold electronics readout system.**



FPGA resource utilization with Ethernet interface

FPGA Procurement Plan

- The quote of XCZU6CG-1FFVB1156E was updated in early 2023 by Avnet
 - Step 2 price of \$1,322.31 each (up to 125 pieces)
 - Step 3 price of \$444.92 each (after 125 pieces)
 - 23 pieces will be consumed in Step 2 before unit price moves to Step 3
- For CD-3A procurement for FD1-HD, a total 800 WIB FPGAs will be ordered
 - The total cost will be $23 \times \$1,322.31 + 777 \times \$444.92 = \$376,115.97$
- The order was processed at BNL with expected **long lead time**
 - Initial delivery date is December 2023, has been updated to August 2023