DEEP UNDERGROUND NEUTRINO EXPERIMENT

Penn
University of Pennsylvania

PTCv4 Final Design Review

[charge questions #5 and #8]

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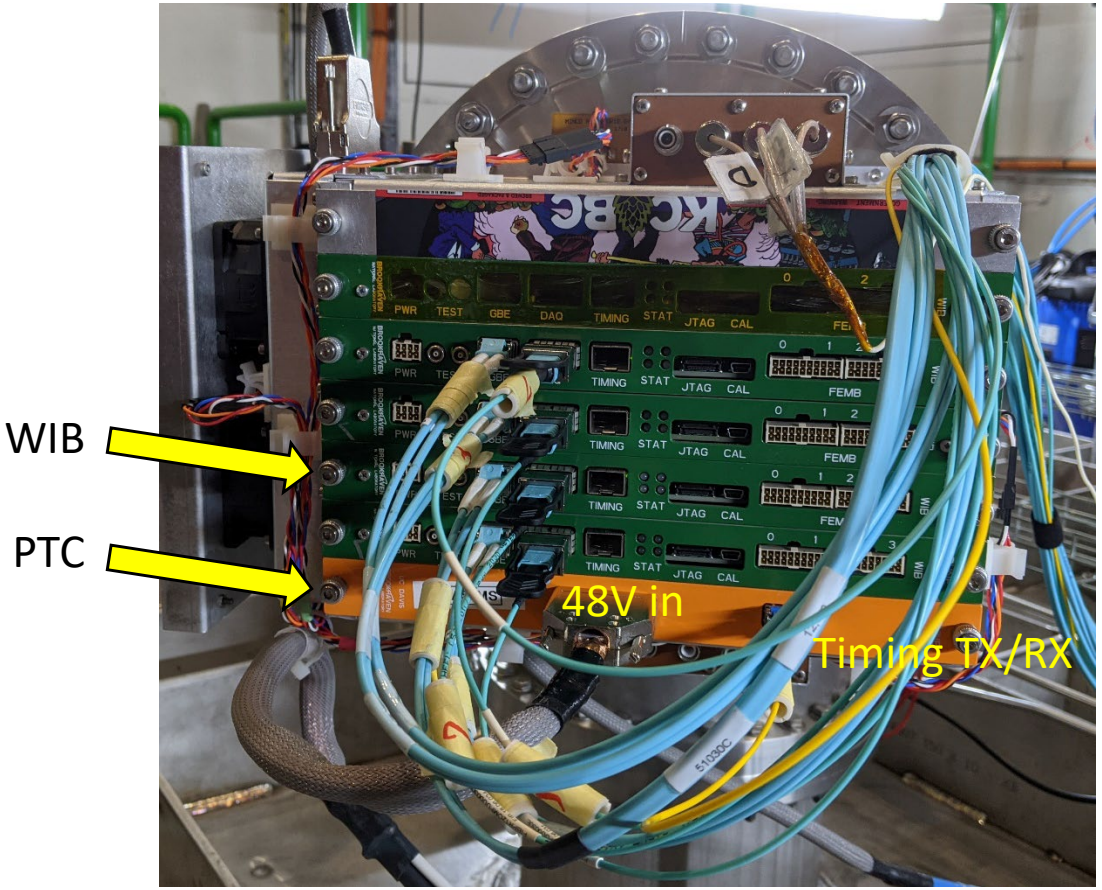
16 May 2023

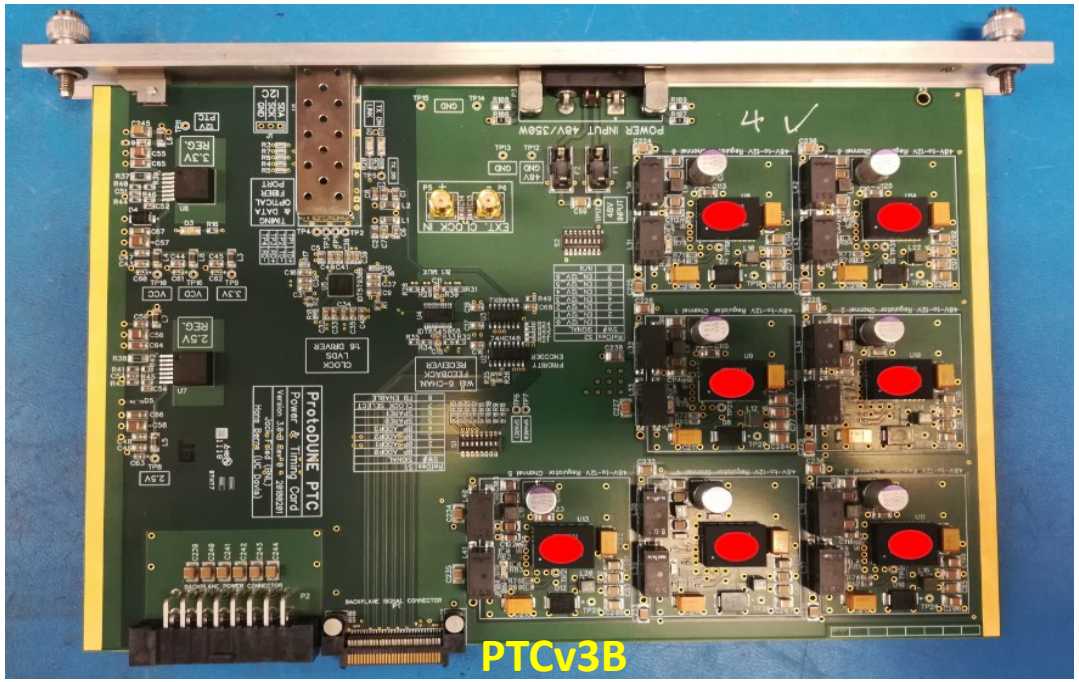
What is PTC?

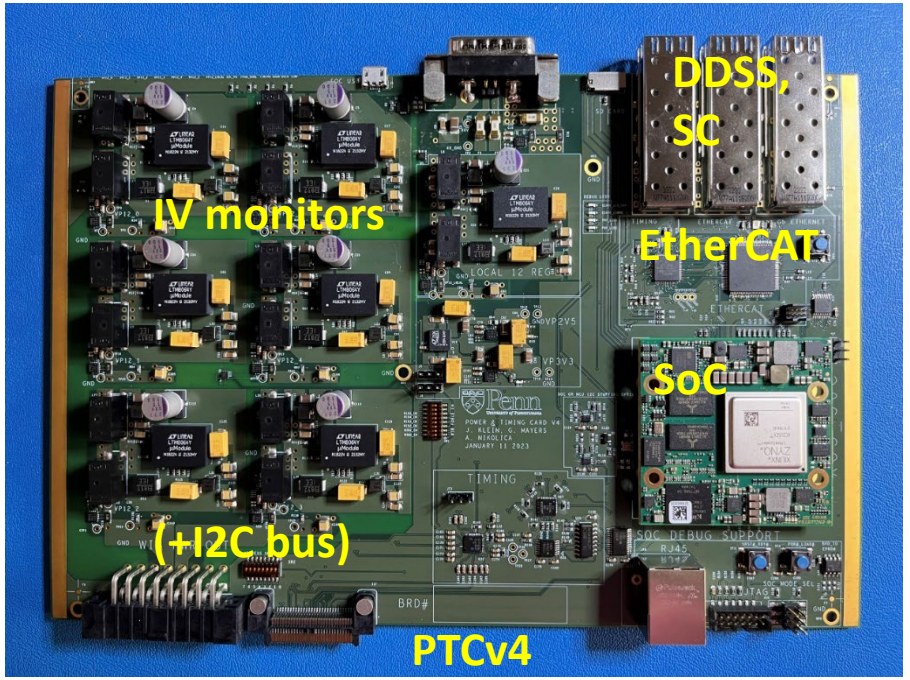
- Power and Timing Card
  - Provides Warm Interface Boards (WIBs) with 12V power on backplane (Power and Timing Backplane, or PTB)
  - Distributes DUNE timing master clock and data (62.5MHz) to WIB over PTB
  - Priority encodes WIB transmission back to timing master (one WIB at a time)



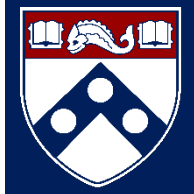
Introduction

- Reasons for re-designing the PTC:
  - Monitoring of local voltages and temperatures
  - Slow Control (SC) interface
  - DUNE Detector Safety System (DDSS) interface
  - Individual WIB control* and/or communications





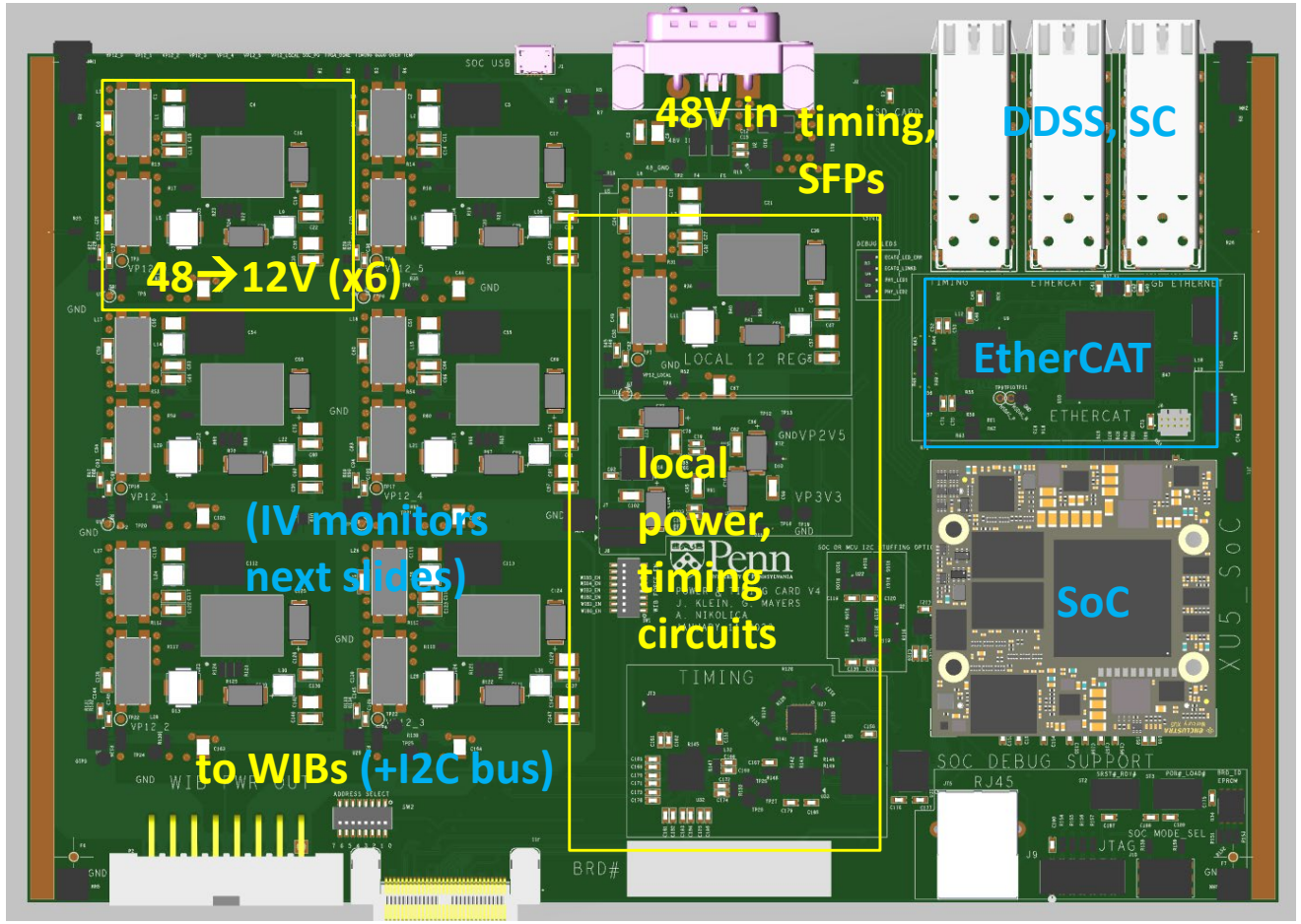
**Existing WIBv3 not able to be powered down in a crate with PTCv4 without affecting some data lines – details later in this presentation*



Requirements and Design

PTCv4: external interfaces

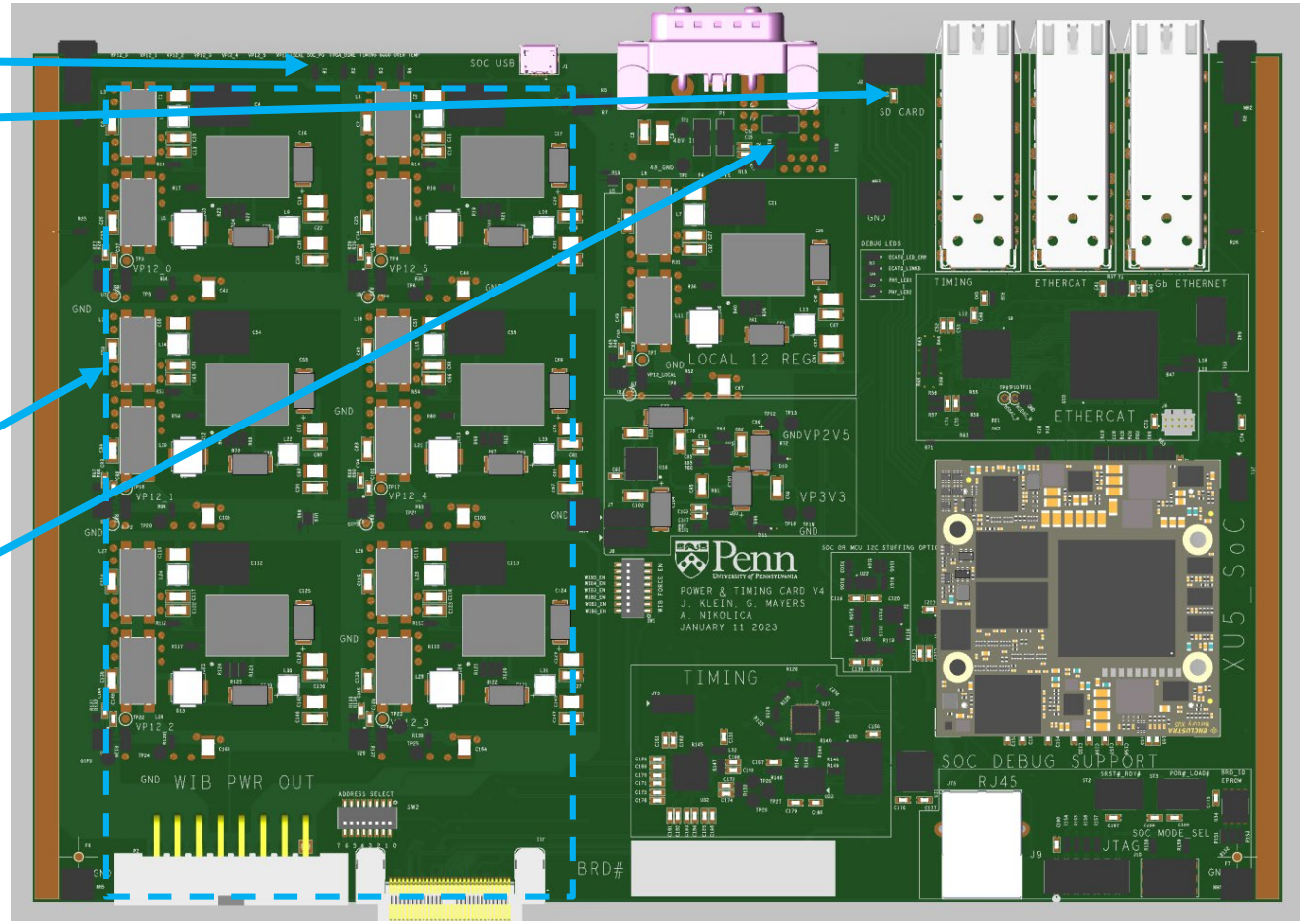
- 48V in
- Bristol timing system via 1000Base-BX SFP
- Slow Control via Ethernet over 1000Base-LX SFP
- DDSS via EtherCAT over 100Base-FX SFP
- WIB Interfaces
  - 12V out to WIB
  - Timing clock and data out to WIB
  - Timing transmit from WIB
  - I2C to/from WIB



PCB image exported from Cadence (populated)
NOTE: **BLUE** = new feature

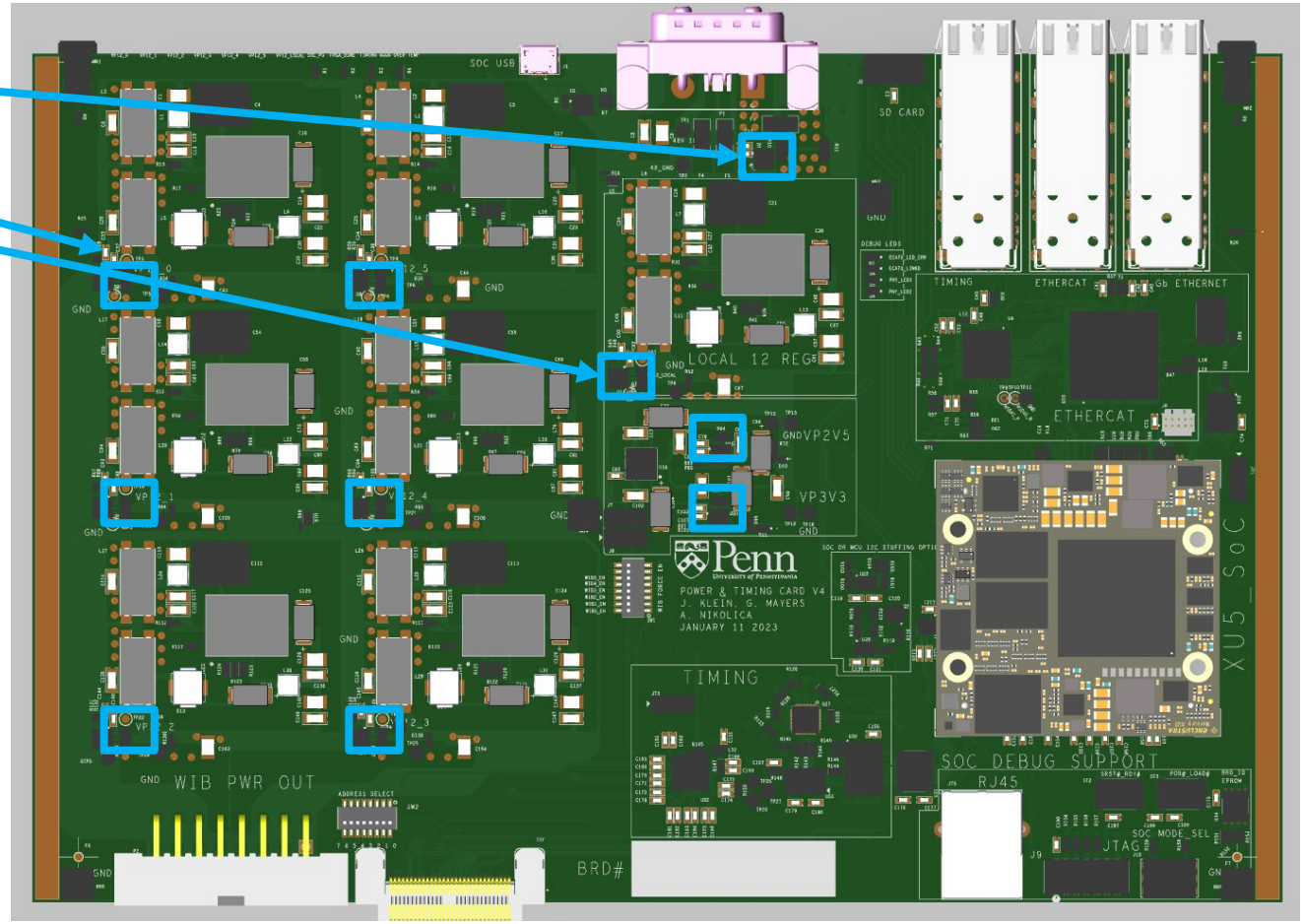
Mechanical and layout features

- Front panel additions
  - Many status LEDs added
  - SD card and UART (for SoC)
- Regulators layed out as modules
  - Moved to other side so SoC does not intrude on power plane
- Power plane isolation
  - Individual WIB power regulator ground isolation preserved and improved
  - Timing and other digital signals routed away from power section
- On-board fusing added



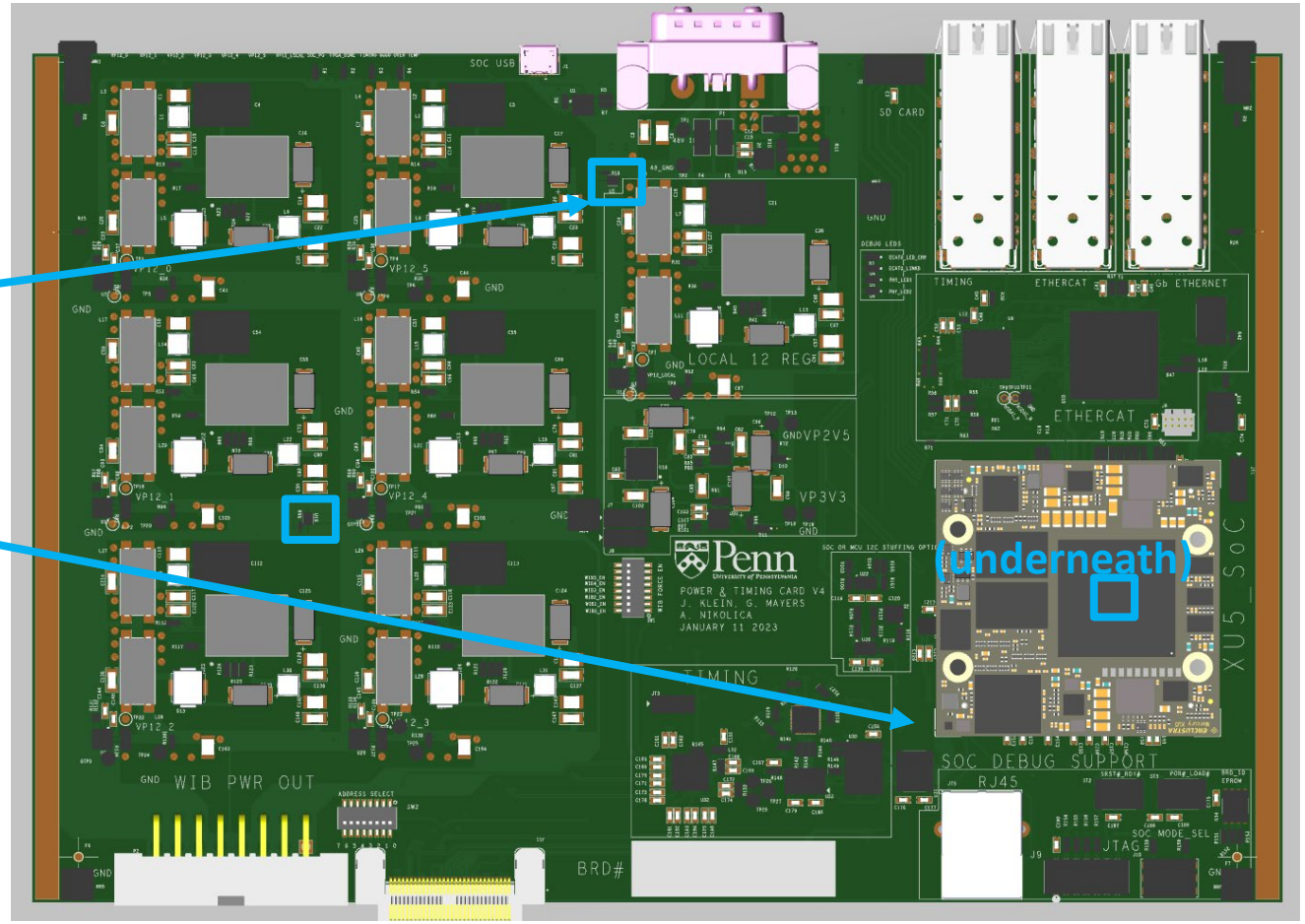
Monitored quantities

- Voltages and currents (using LTC2945):
  - 48V input
  - All 6x WIB 12V rails
  - Local 12V (3.3V and 2.5V optional)



Monitored quantities

- Voltages and currents (using LTC2945):
  - 48V input
  - All 6x WIB 12V rails
  - Local 12V (3.3V and 2.5V optional)
- Temperatures (using TMP117)
  - 3x locations on board
  - SoC can monitor its own FPGA internal temperature



Monitored quantities

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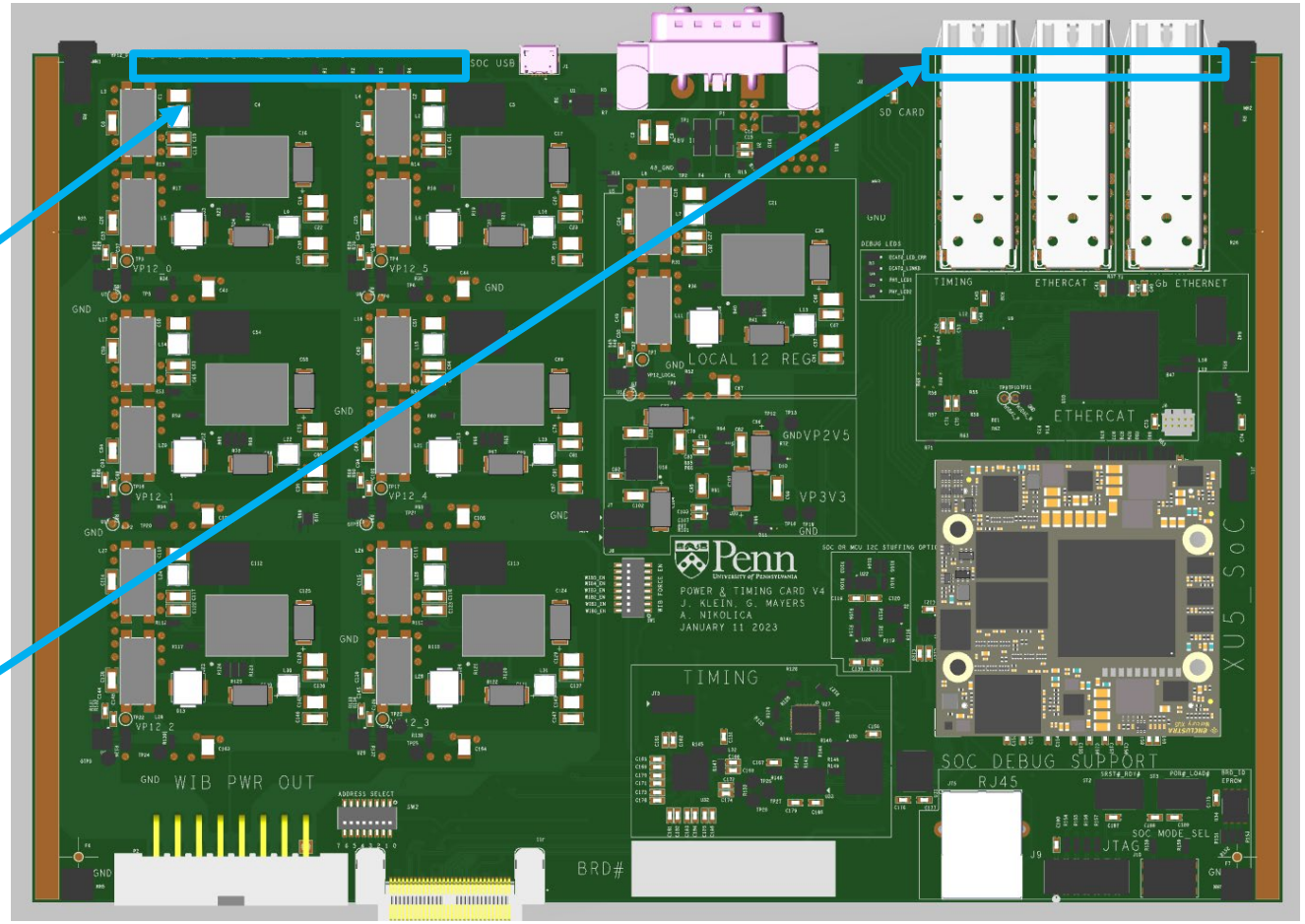
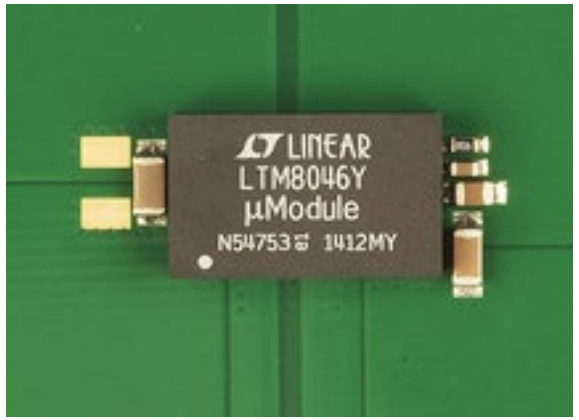
  - 48V input
  - All 6x WIB 12V rails
  - Local 12V (3.3V and 2.5V optional)
- Temperatures (using TMP117)
  - 3x locations on board
  - SoC can monitor its own FPGA internal temperature
- LEDs
  - 6x WIB power indicators
  - Over temperature (FPGA programmable)
  - SoC: power good, and FPGA done
  - Timing signal okay (decoded by FPGA)
  - SFP LEDs:
    - 3x loss of signal (LOS)
    - Timing: WIB transmit back indicator
    - DDSS: EtherCAT link active
  - (Other debug LEDs for bench only)

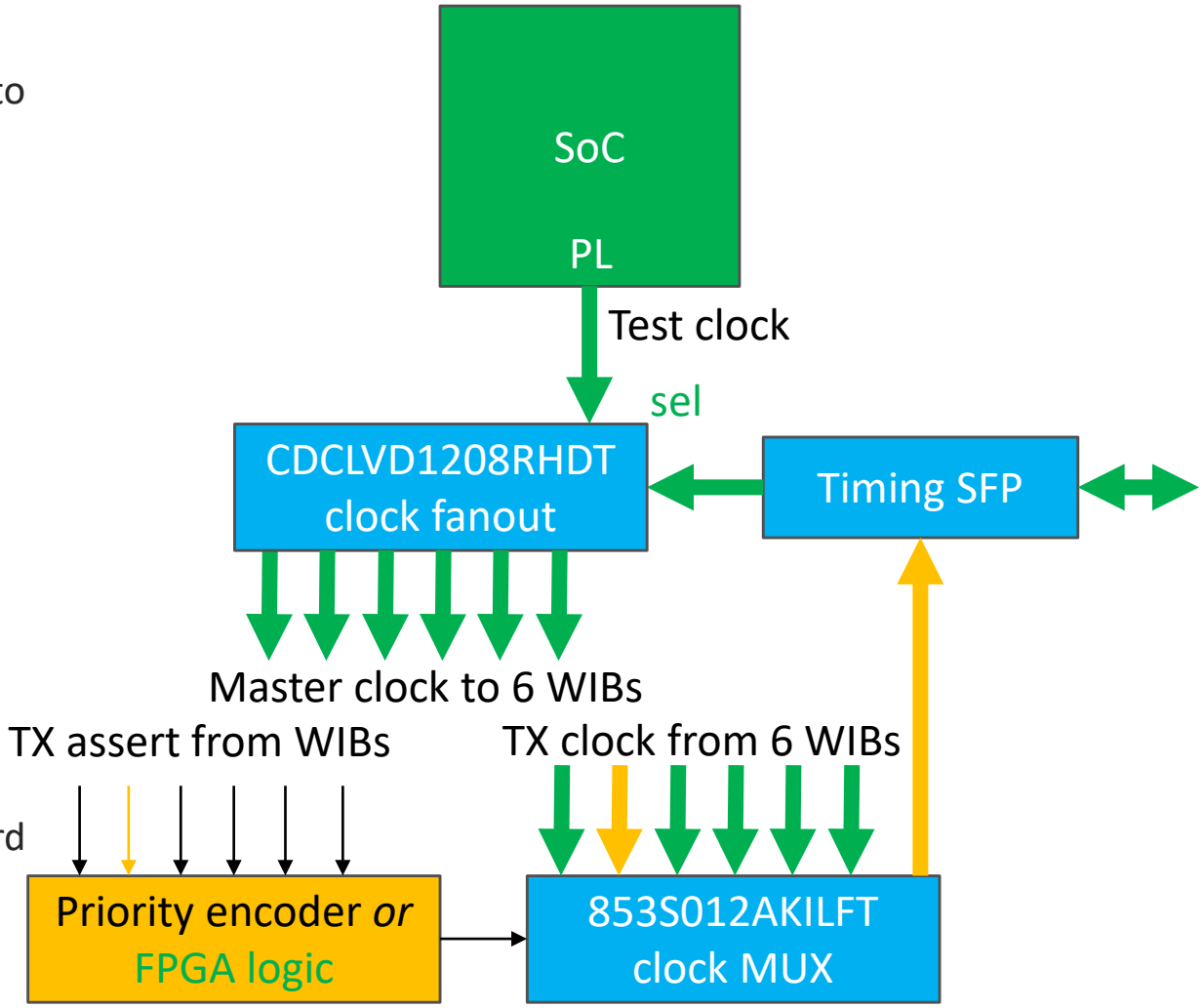


Design: power and timing

- Power regulators
  - Use same LTCM8064 48V -> 12V DC-DC converters as PTCv3B
  - Set to 970kHz switching frequency, but have option to use SYNC to drive out of phase
  - LTM4622 DC-DC for 3.3V and 2.5V local electronics

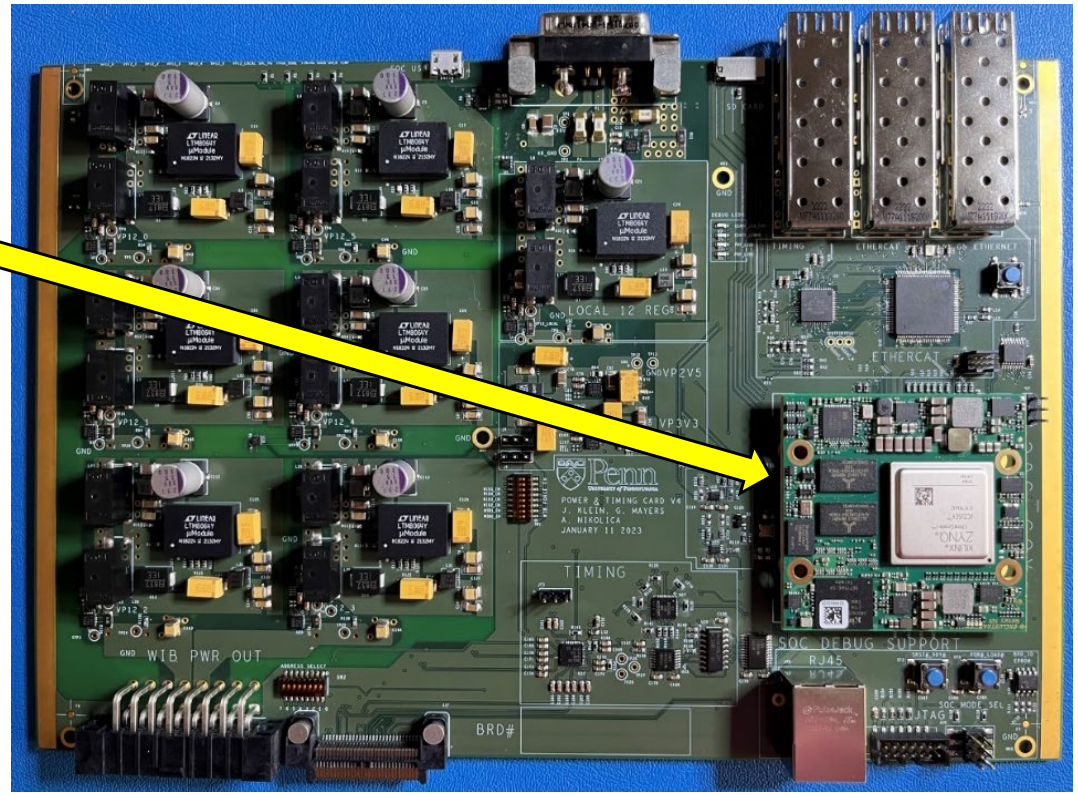


- Timing system:
  - Timing information is only passed through in hardware (existing functionality)
  - Option to control priority encoder with FPGA to guard against hang-up on WIB



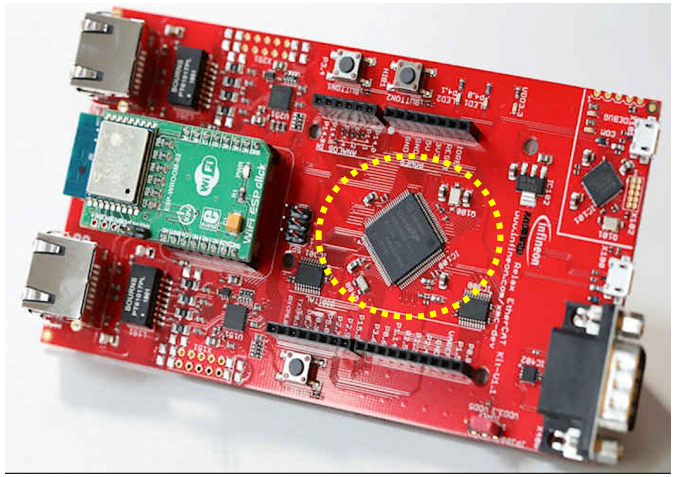
Design: FPGA

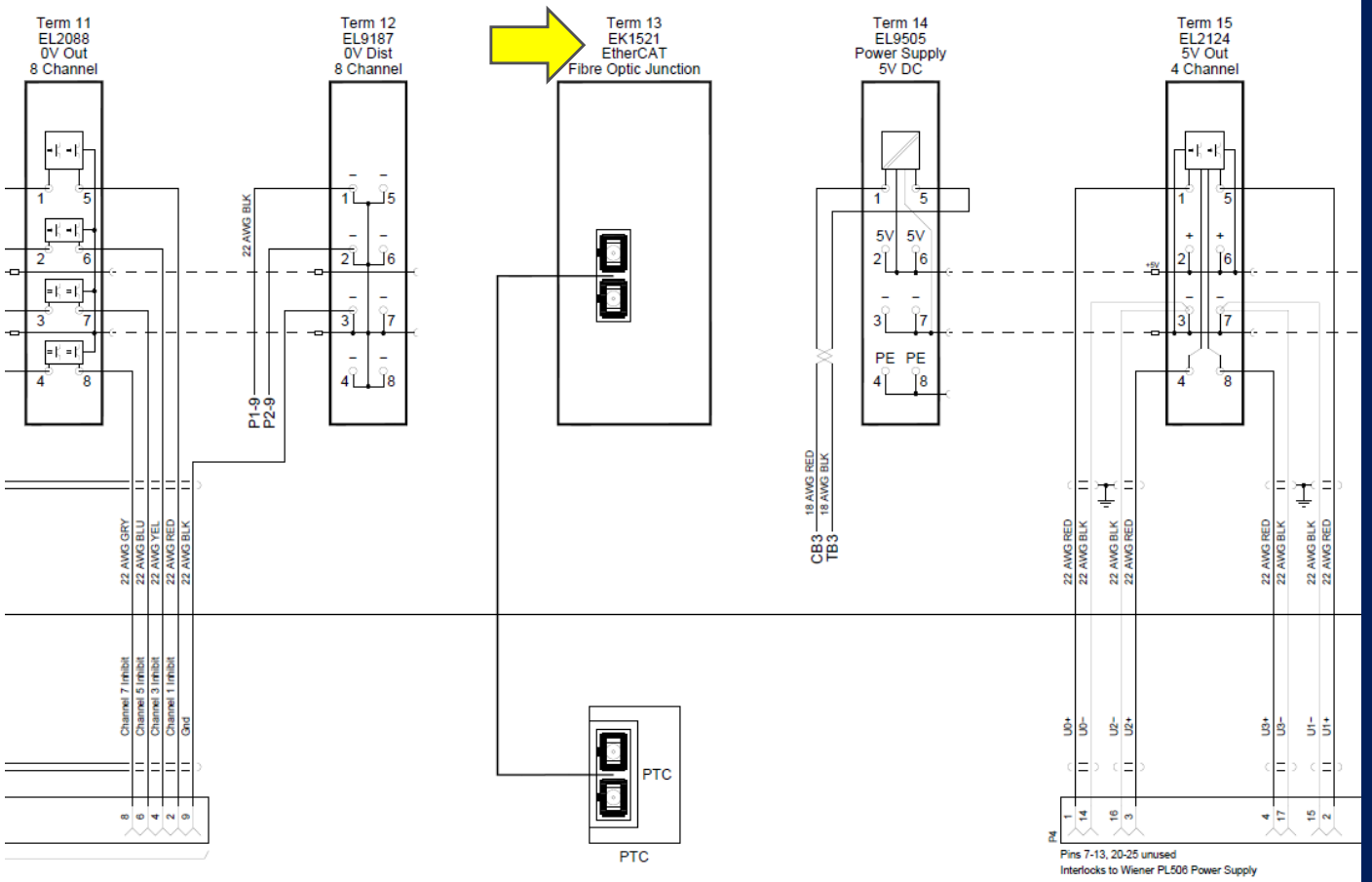
- SoC mezzanine
  - Enclustra ME-XU5-5EV-2I-D12E (prototypes)
  - Same Xilinx Zynq UltraScale+ FPGA family as WIB
  - Simple to design with, upgradeable during detector life
- SoC functions:
  - Power sequencing and control
  - GbE to SC
  - UART communications to EtherCAT microcontroller
  - I2C power monitoring (local, and WIB)
  - Minimal timing endpoint interface



Design: EtherCAT

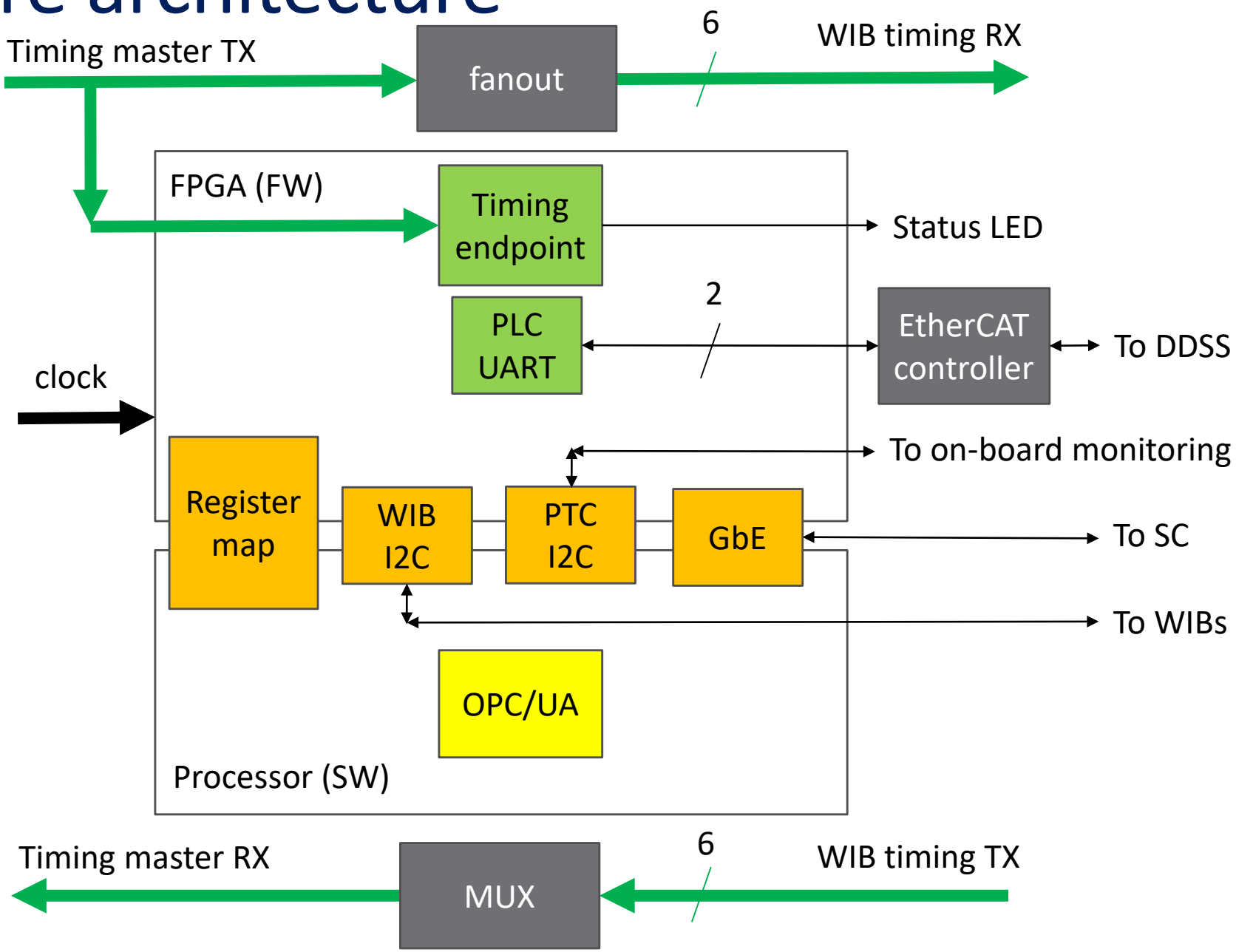
- EtherCAT interface is required for DDSS connection (already designed)
- Implemented with an Infineon XMC4300 EtherCAT-capable microcontroller
  - Beckhoff firmware solution was prohibitively expensive





(Section of DDSS design -- link in backup slides)

Firmware architecture

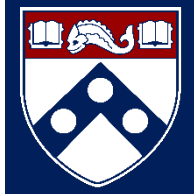


Architectural questions

- Powered-off WIBs
  - It was confirmed in conversation with Jack Fried in July 2022 that there is no way to permanently power off a WIB in a crate with PTCv4 without affecting functionality of shared IO lines to other WIBs
  - This is because WIBs have no IO buffering for the following signals: timing TX enables, crate addresses, spare IOs
  - This means a powered off WIB's FPGA can pull down a line (confirmed with measurement)
  - **There are two solutions, for prototypes ONLY:**
    - **Do not power off WIB for the first prototypes; only power cycle if needed, or remove from crate**
    - Re-spin the PTB (power and timing backplane) to include buffers powered by local WIB and PTC 2.5V
  - For the long term, the **WIB will be re-spun with additional buffers added**
- IO bandwidth
  - I2C bus @ 400kHz will limit local BW
  - ~90 quantities that can be monitored
  - EtherCAT 100Mbps is also a hard limit total BW
  - Really only need 1-2Hz for a lot of these power and temp measurements – much more reasonable
- Is PTC an independent OPC/UA endpoint, or the OPC/UA endpoint for all WIBs in a crate, or not an OPC/UA endpoint at all?
  - PTCv4 can do any / all options

Requirements and design summary

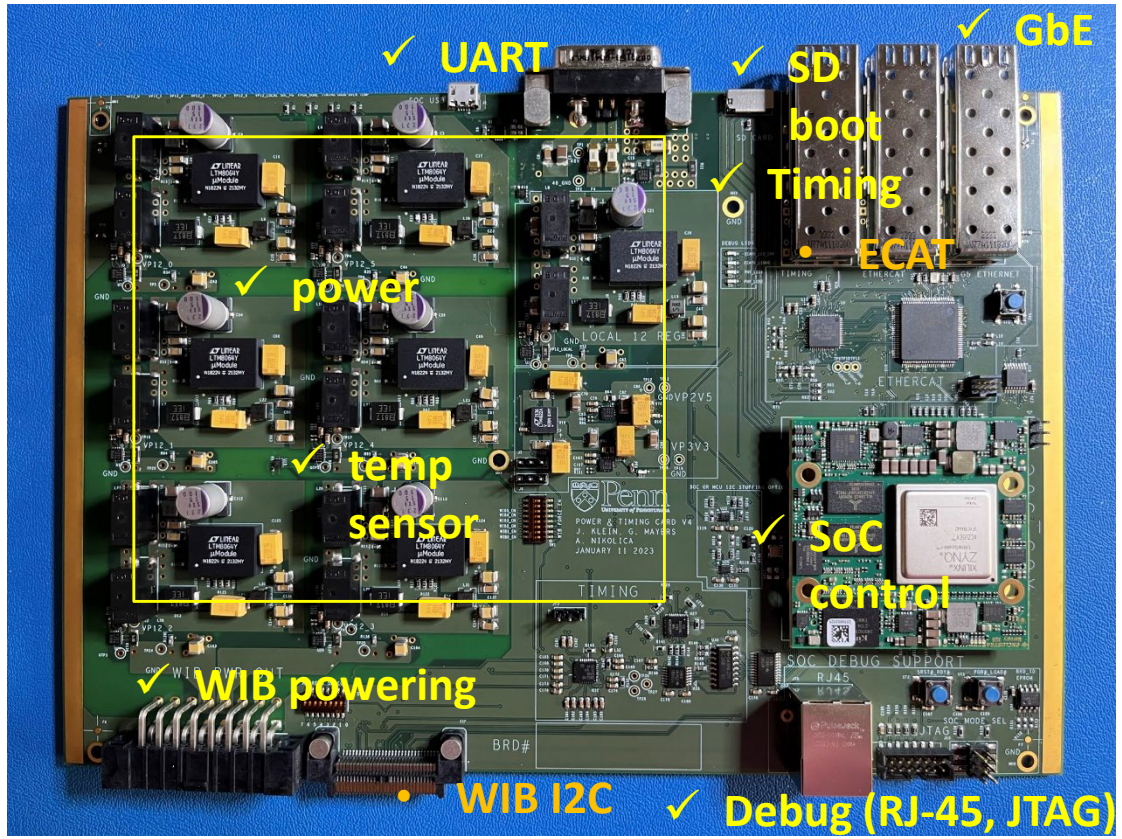
- Power scheme the same v3B->v4, except for minor layout changes
- Timing scheme the same v3B->v4, except for minor part variant changes
- Added:
  - Monitoring of local voltages and temperatures
  - Slow Control (SC) interface
  - DUNE Detector Safety System (DDSS) interface
  - Individual WIB control and communications



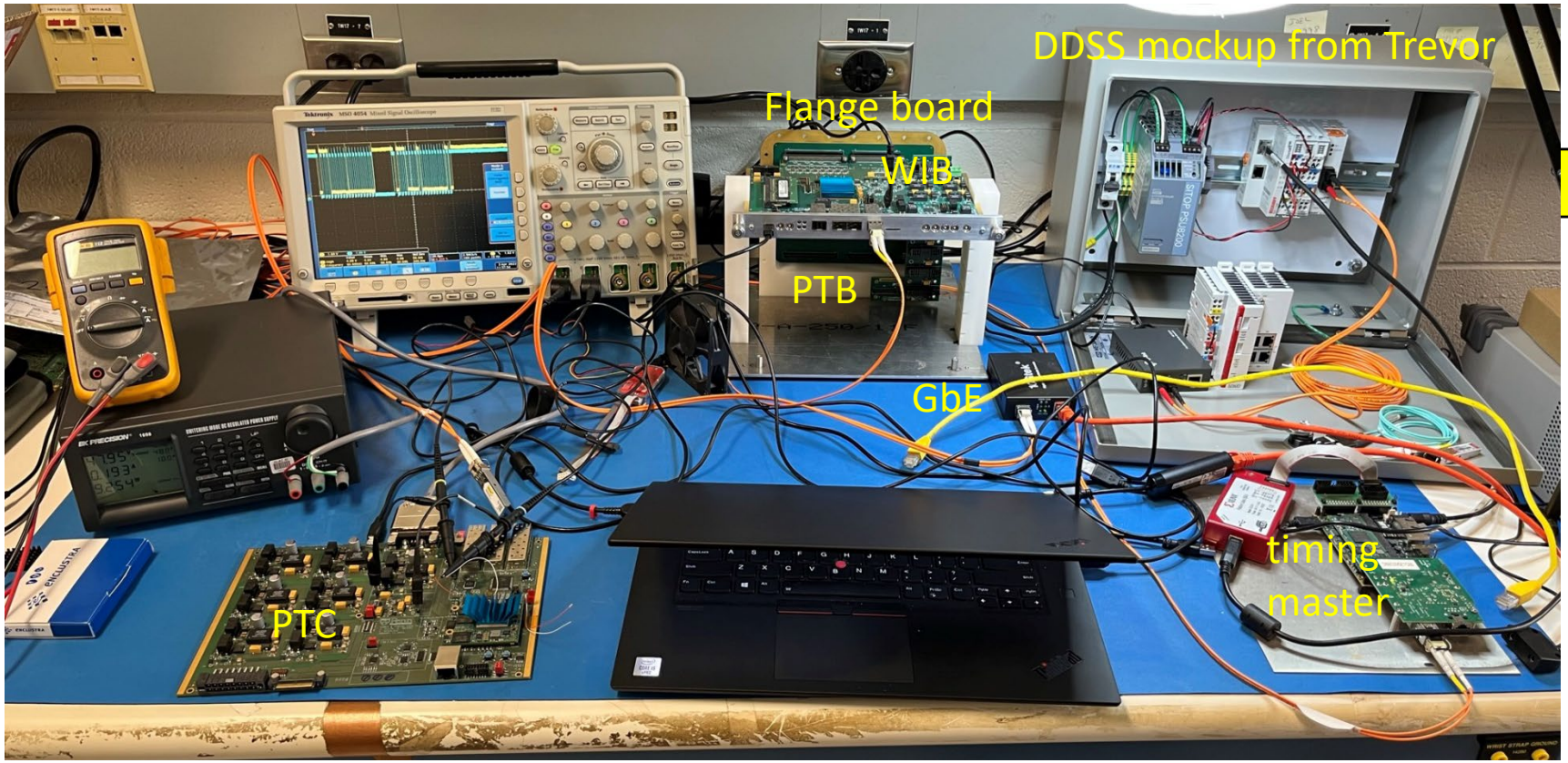
Testing

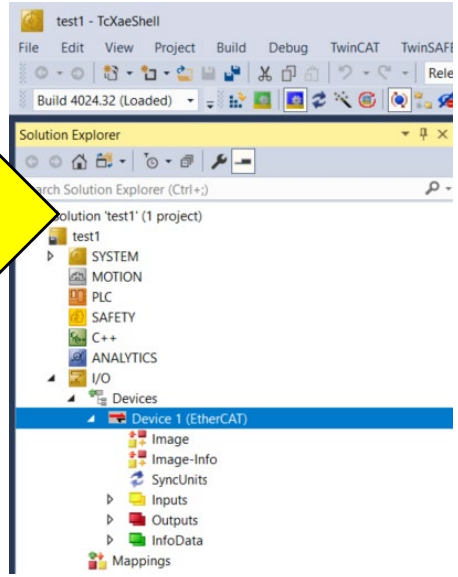
Testing summary

- ✓ All six 12V regulators power up, can be enabled via FPGA register bit
- ✓ Local 12V, 3.3V, 2.5V power all ICs with no excessive current
- ✓ Enclustra Mercury XU5 mezznanine (Zynq 5EV Ultrascale+):
  - ✓ Boots via SD card
  - ✓ Front panel UART, debug RJ-45, and JTAG work
  - ✓ SFP status signals can be read in via FPGA register bits
  - ✓ Can talk to temperature sensors
  - ✓ Can talk to LTC2945 (and LTC2945-1 backup variant)
- ✓ Can power WIBs (one tested, full WEIC at BNL)
- ✓ Timing distribution test (TX and RX) work on bench
- ✓ GbE can talk over front panel
- ✓ WIB I2C electrically tested (more WIB FW needed)
- EtherCAT – in progress, shows initial signs of life (identification of PTC on EtherCAT bus)
- Errata:
  - ✓ One minor footprint error on reset pushbuttons – already worked around on prototypes
  - ✓ Wrong part purchased for IV monitor – not a design issue; mitigation works
  - ✓ Component change for a level translator – works
  - ✓ Minor signal polarity corrections



Penn test stand

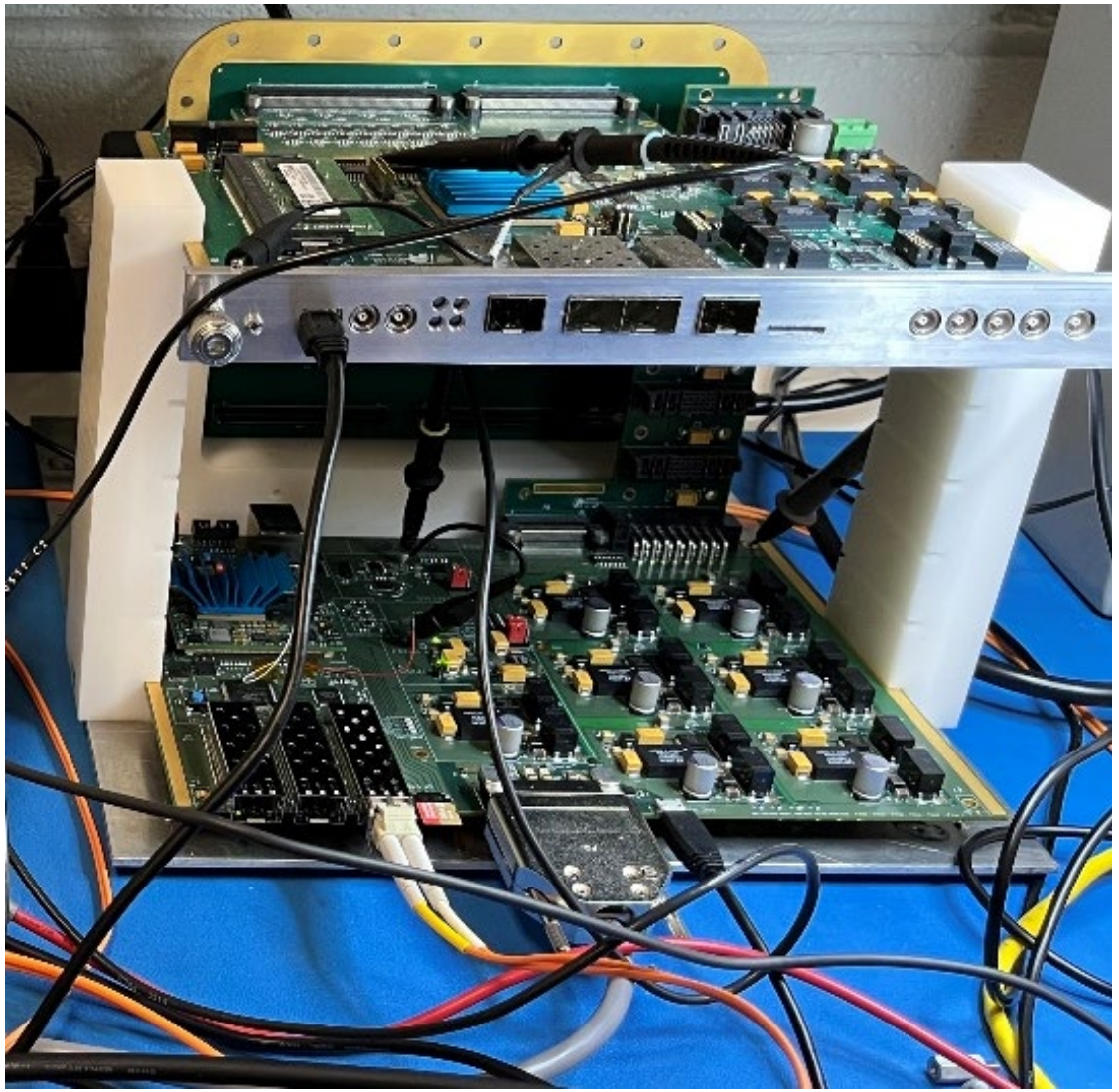




Beckhoff TwinCAT
EtherCAT software master

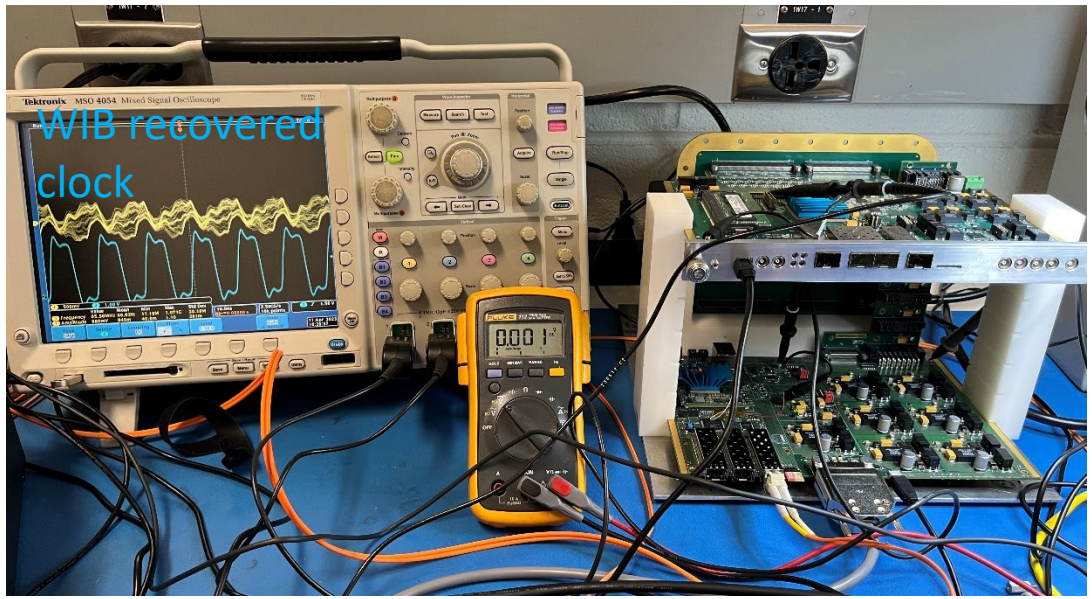
Powering a WIB

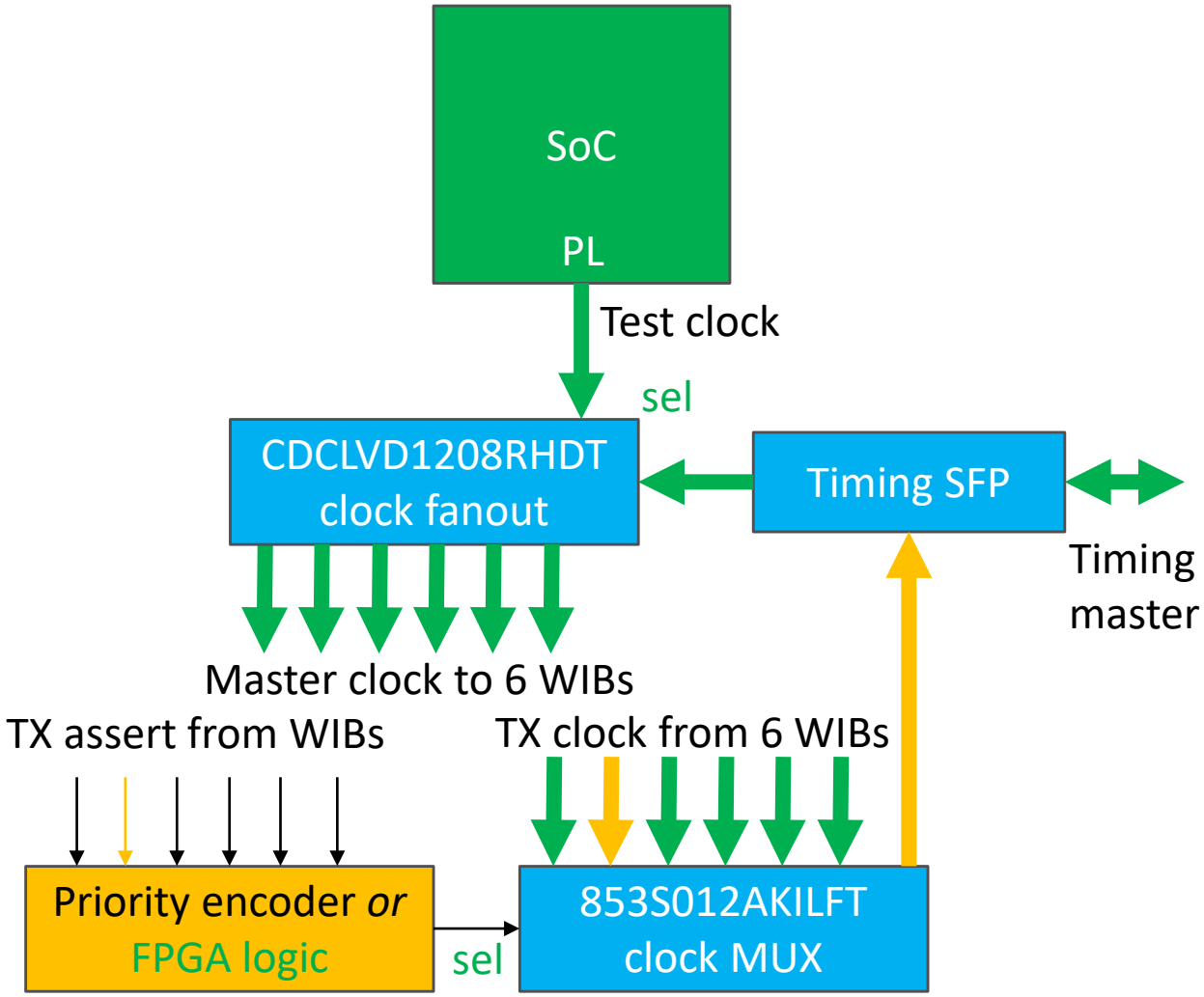
- Carefully checked new interfaces
  - Level translation on backplane addressing and timing priority encode
  - Power sequencing
- Powering works, expected current consumption measured
- “Noise” test being conducted at BNL



Timing tests

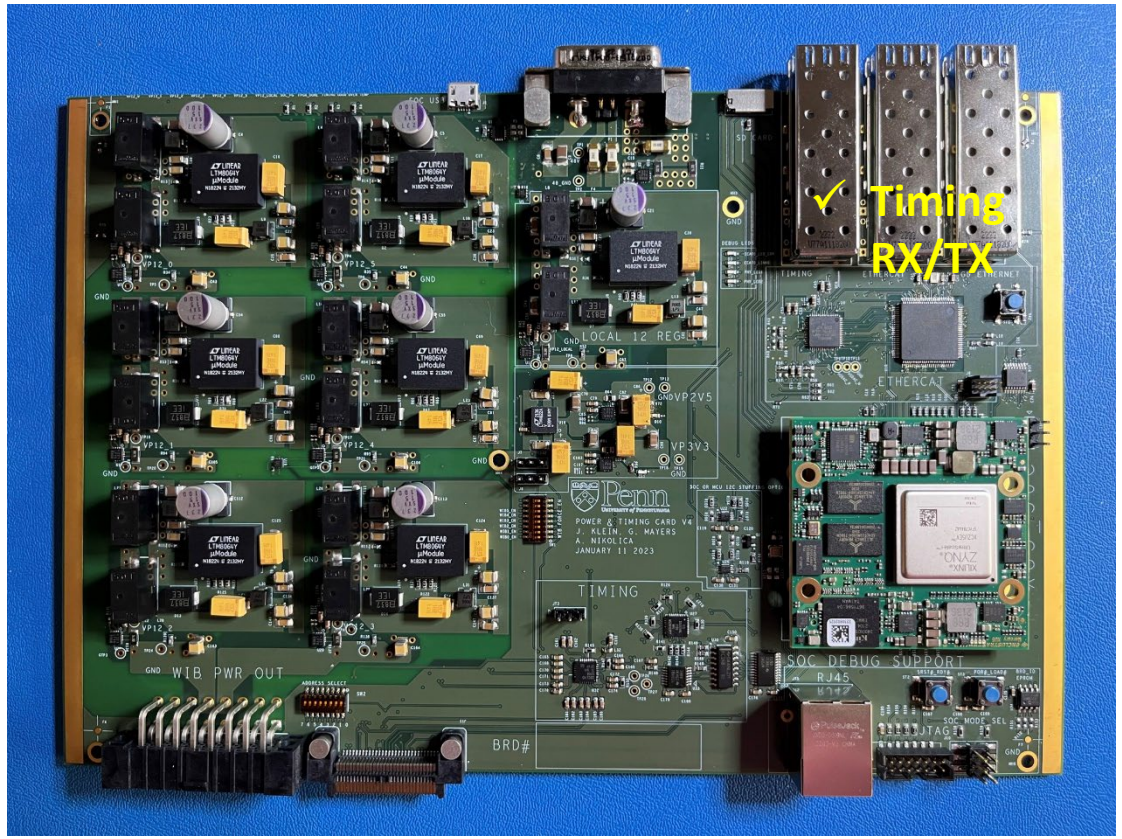
- PTC timing distribution:
  - Have the ability to generate a test clock
  - Or use the fiber connection from timing master for DCSK stream
- Transmission back to timing master:
  - Timing information is only passed through in hardware, and hardware priority encoder used to MUX
  - Can also use FPGA-controlled MUX





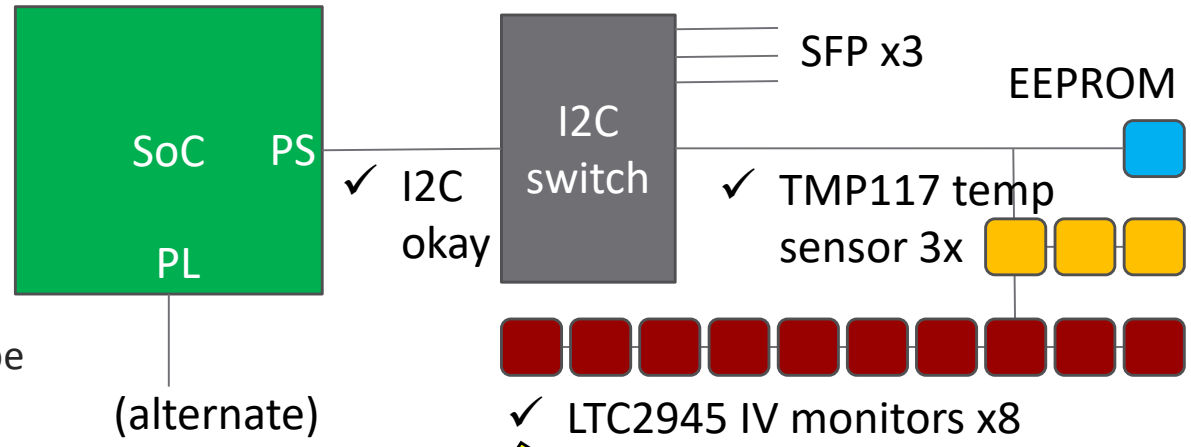
Power and timing conclusion

- Powering a WIB has had no major issues
  - Pending results of BNL test
- Components on PTCv4 work:
  - TI fanout
  - Resesas MUX
  - TI priority encoder
  - (new) TI level translator
  - LTM8064 DC-DC converters
- Small WIB firmware fix needed to account for combinations of hardware (backup slides)



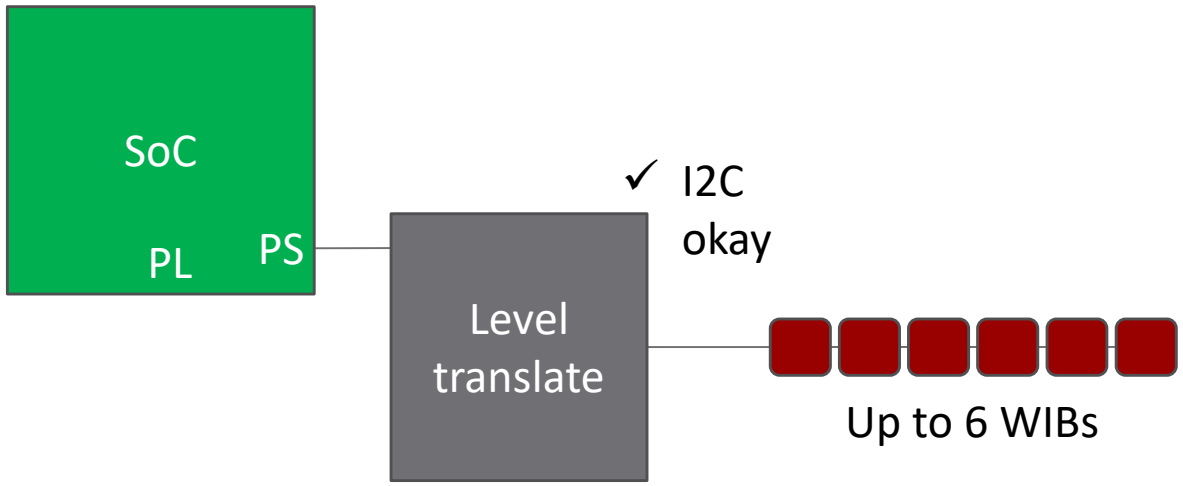
I2C tests to PTC sensors

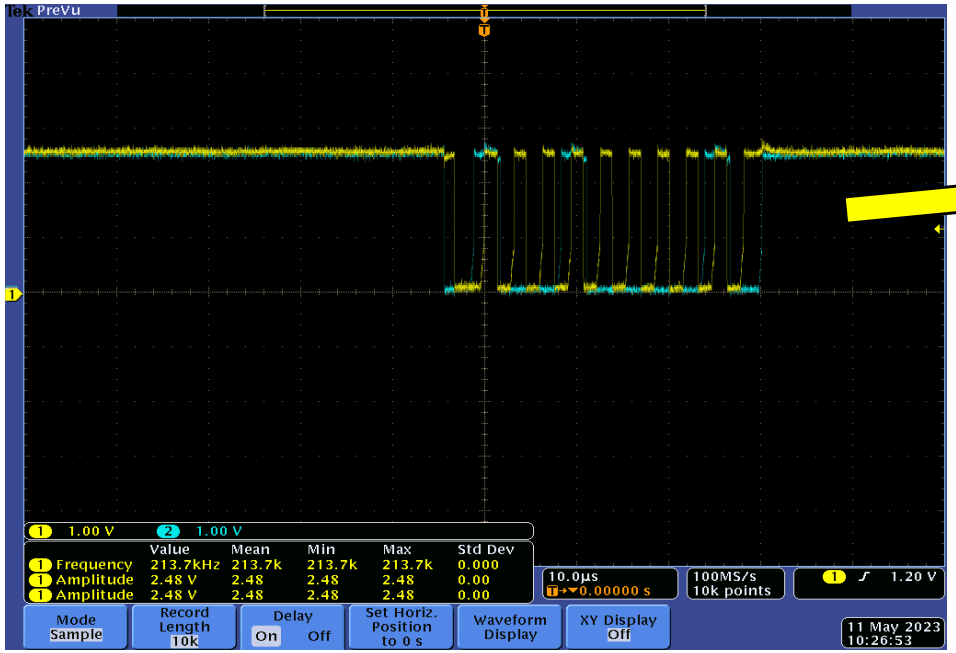
- I2C from Zynq PS through I2C switch to temperature sensors works
- Main current monitor parts are long lead time
  - Current lead times for LTC2945 are up to 52 weeks
  - We have a small stock of these for prototypes
  - LTC2945 “-1” variant with inverted output logic can be used with some board rework. We have a large number of these. Mitigation in backup slides.

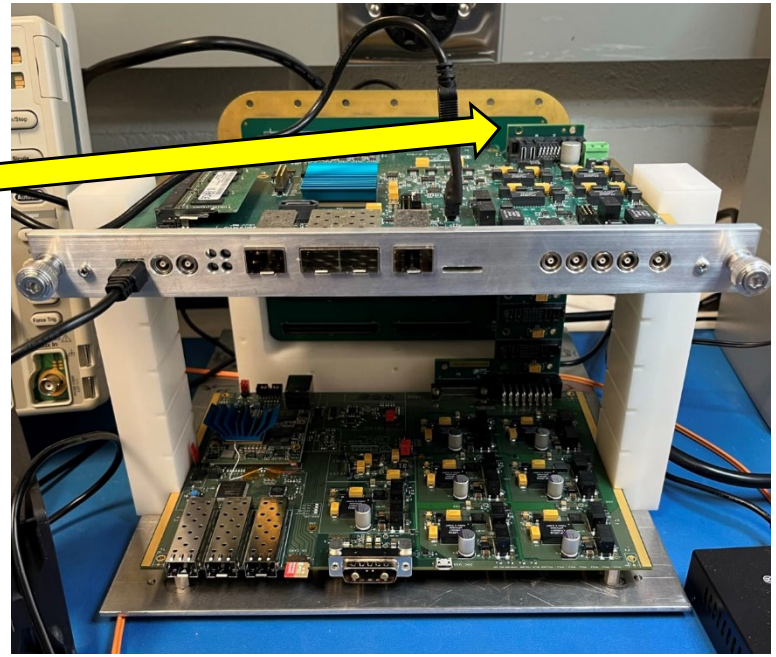


I2C tests to WIB

- I2C from Zynq PS through level translator to WIB has been electrically tested
  - Need some more FW work on WIB

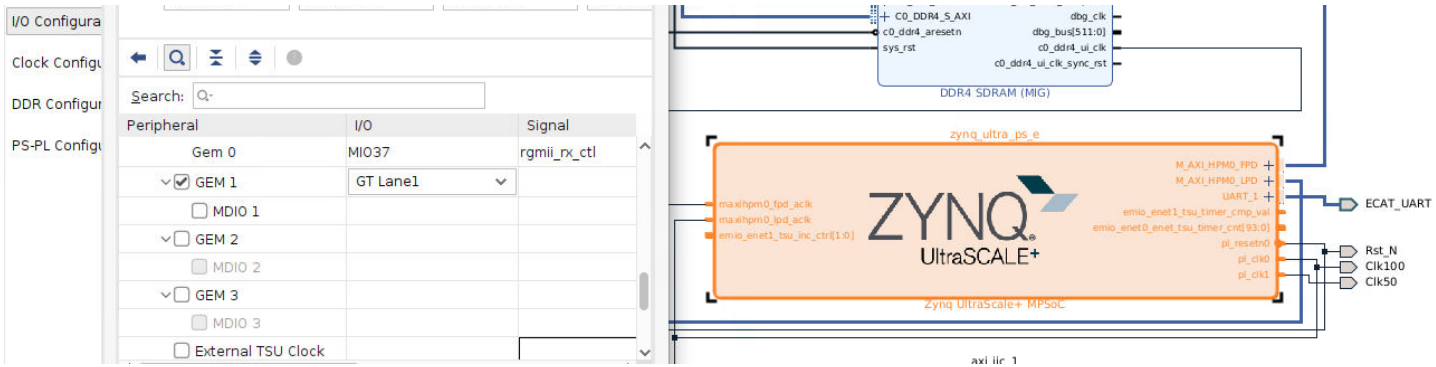






GbE to SC

- SC GbE is on front panel SFP
- Configured in Zynq settings
  - PS transceivers
  - Same HW/config as WIB
  - Verified reference clock is okay
  - Need to write one Zynq register config to bring up interface (same as WIB)
- Using 10GTek A7S2-33-1GX1GT-SFP/GT3 fiber-to-copper converter
  - Same exact HW as WIB test stand

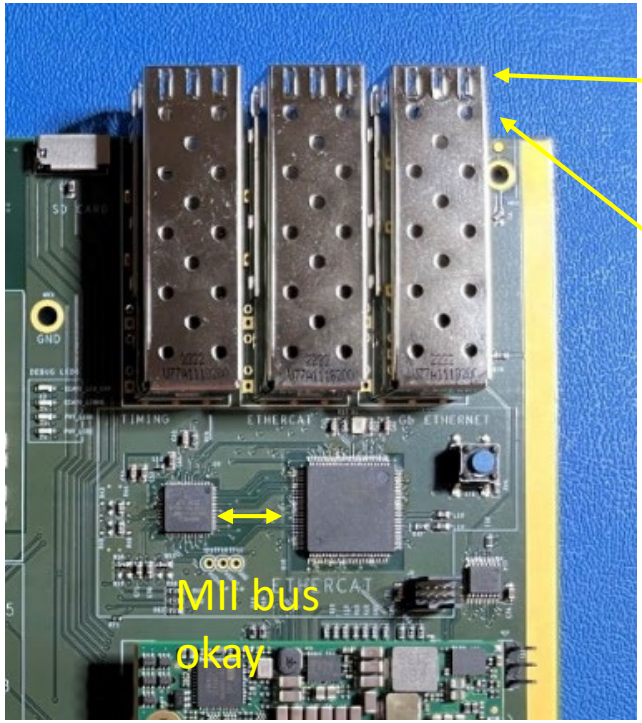


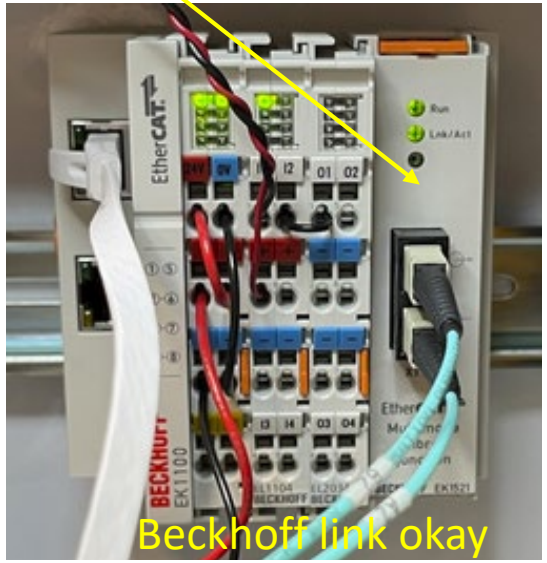

```
root@ptc:~# ifconfig
eth0      Link encap:Ethernet  HWaddr C6:10:4A:82:8C:13
          inet6 addr: fe80::c410:4aff:fe82:8c13/64 Scope:Link
          UP BROADCAST MULTICAST  MTU:1500  Metric:1
          RX packets:118 errors:0 dropped:0 overruns:0 frame:0
          TX packets:51 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:13135 (12.8 KiB)  TX bytes:8082 (7.8 KiB)
          Interrupt:38

eth1      Link encap:Ethernet  HWaddr 00:0A:35:00:22:01
          inet addr:192.168.200.12  Bcast:192.168.200.255  Mask:255.255.255.0
          inet6 addr: fe80::20a:35ff:fe00:2201/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:44 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:8609 (8.4 KiB)
          Interrupt:39

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:80 errors:0 dropped:0 overruns:0 frame:0
          TX packets:80 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:6080 (5.9 KiB)  TX bytes:6080 (5.9 KiB)
```

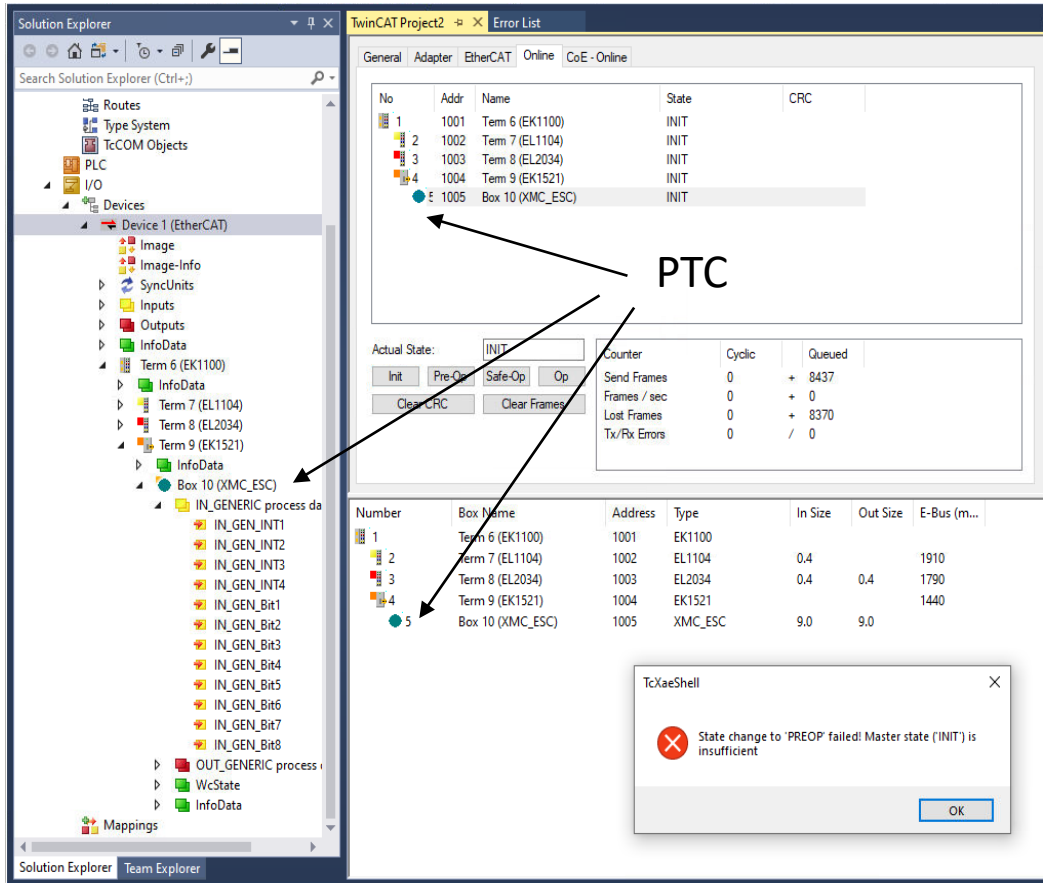
EtherCAT tests

Initial signs of PTC being recognized in TwinCAT.

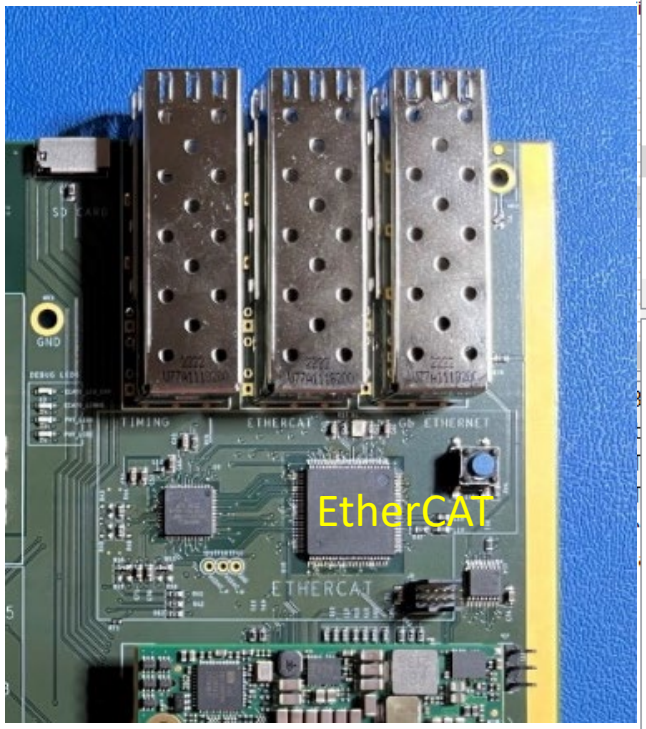
Currently debugging full data exchange.







EtherCAT tests



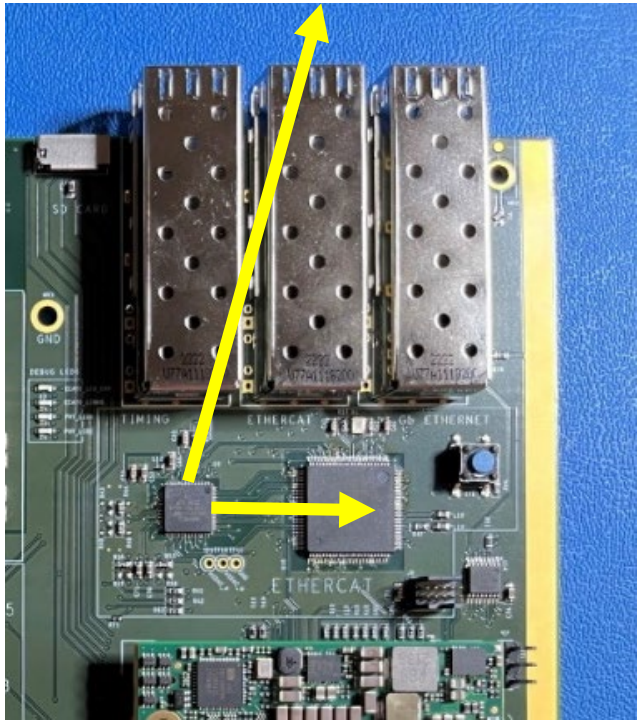
Wireshark captured packets

No.	Time	Source	Destination	Protocol	Length	Info
294	11.564816	Beckhoff_01:00:00	02:00:00:00:00:00	ECAT	60	'BRD': Len: 2, Adp 0x1, Ado 0x130, Wc 1
295	11.564819	00:00:00_00:00:00	Beckhoff_01:00:00	ECAT	30	'BRD': Len: 2, Adp 0x0, Ado 0x130, Wc 0
296	11.566804	00:00:00_00:00:00	Beckhoff_01:00:00	ECAT	43	2 Cmds, 'APWR': len 1, 'BRD': len 2
297	11.566811	Beckhoff_01:00:00	02:00:00:00:00:00	ECAT	60	'BRD': Len: 2, Adp 0x1, Ado 0x130, Wc 1
298	11.566814	Beckhoff_01:00:00	02:00:00:00:00:00	ECAT	60	'BRD': Len: 2, Adp 0x1, Ado 0x130, Wc 1
299	11.566817	00:00:00_00:00:00	Beckhoff_01:00:00	ECAT	30	'BRD': Len: 2, Adp 0x0, Ado 0x130, Wc 0
300	11.568766	Beckhoff_01:00:00	02:00:00:00:00:00	ECAT	60	2 Cmds, 'APWR': len 1, 'BRD': len 2
301	11.667536	00:00:00_00:00:00	Beckhoff_01:00:00	ECAT	30	'BRD': Len: 2, Adp 0x0, Ado 0x130, Wc 0
305	11.768226	00:00:00_00:00:00	Beckhoff_01:00:00	ECAT	30	'BRD': Len: 2, Adp 0x0, Ado 0x130, Wc 0
306	11.867113	00:00:00_00:00:00	Beckhoff_01:00:00	ECAT	30	'BRD': Len: 2, Adp 0x0, Ado 0x130, Wc 0

```
> Ethernet II, Src: Beckhoff_01:00:00 (01:01:05:01:00:00), Dst: 02:00:00:00:00:00 (02:00:00:00:00:00)
> EtherCAT frame header
v EtherCAT datagram(s): 2 Cmds, 'APWR': len 1, 'BRD': len 2
  v EtherCAT datagram: Cmd: 'APWR' (2), Len: 1, Adp 0x1, Ado 0x101, Cnt 1
    v Header
        Cmd        : 2 (Auto Increment Physical Write)
        Index: 0xa4
        Slave Addr: 0x0001
        Offset Addr: 0x0101
      > Length     : 1 (0x1) - No Roundtrip - More Follows...
        Interrupt: 0x0000
    v ESC Ctrl (0x101): 0xf4, Port 0: Auto loop, Port 1: Auto close only, Port 2: Loop closed, Port 3: Loop closed
        .... ..00 = Port 0: Auto loop (0x0)
        .... 01.. = Port 1: Auto close only (0x1)
        ..11 .... = Port 2: Loop closed (0x3)
        11.. .... = Port 3: Loop closed (0x3)
      Working Cnt: 1
  v EtherCAT datagram: Cmd: 'BRD' (7), Len: 2, Adp 0x1, Ado 0x130, Cnt 1
```

Some responses from PTC

EtherCAT tests

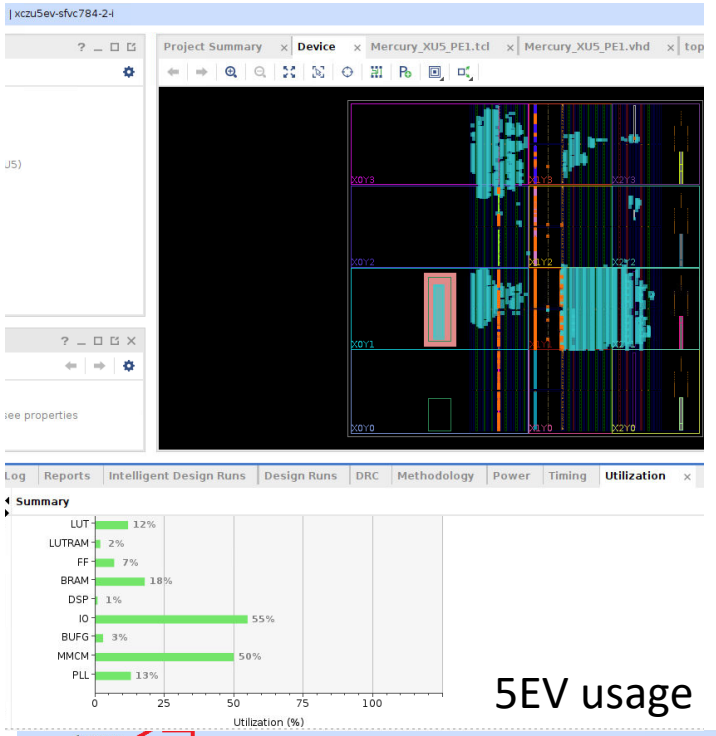


- What does it mean?
- Evidence that the hardware link is working
  - EtherCAT packets in Wireshark must be coming from XMC4300
  - XMC4300 LED status indicates EtherCAT block is being accessed
  - PHY LED status indicates 100Base-FX link is being maintained
- Suggest a possible code problem with the XMC4300
  - Debugging with vendor JTAG pod shows EtherCAT initialization routines being run, just like development board reference
  - EtherCAT packets seem to stop getting transmitted at some point after bus identification
  - Need to understand deep details of EtherCAT protocol next
  - Support tickets filed with Beckhoff and Infineon

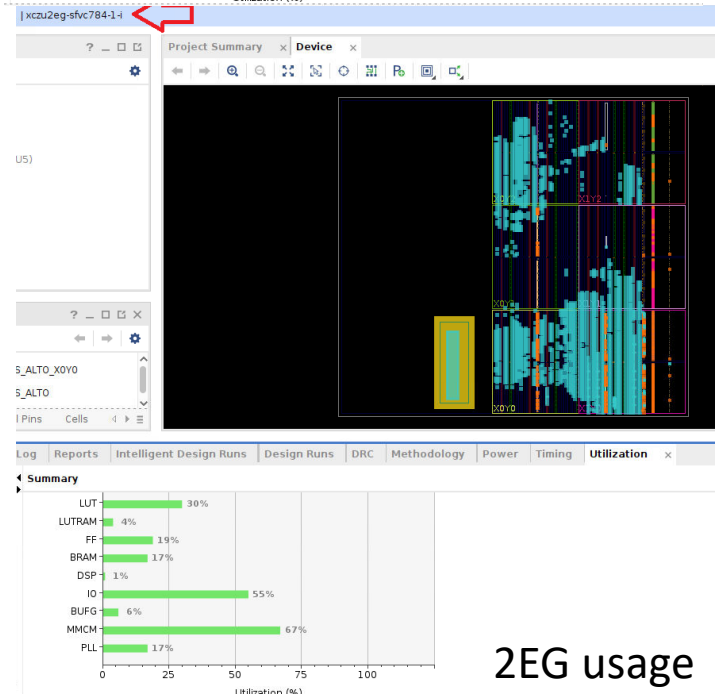
FPGA choice, components

- FPGA history
  - Originally suggested to use same FPGA as WIB
  - Agreed on using commercial mezzanine:
    - Prototype part: Enclustra ME-XU5-5EV-2I-D12E
    - Proposed production part: ME-XU5-2EG-1I-D11E*
    - Same Xilinx Zynq UltraScale+ FPGA family as WIB
    - Simple to design with, upgradeable during detector life

- Long lead time components:
  - LTM8064 DC-DC converters for WIBs, LTC2945 power monitors
  - Basically all other IC, and some large capacitors and inductors



5EV usage



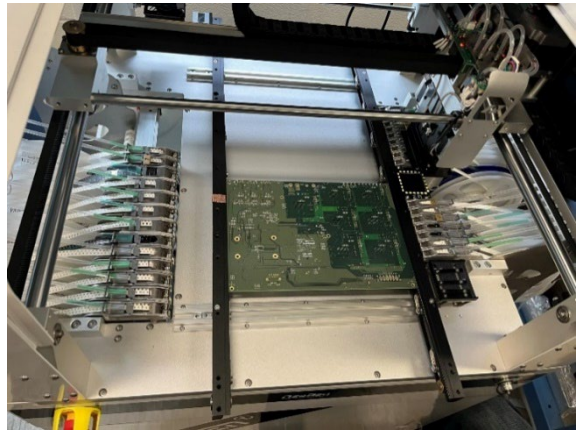
2EG usage

**Might require slight schematic change on final PCB*

Summary

Full project status

- PTCv4 arrived at Penn early March 2023, first board assembled in-house on pick-and-place machine.
  - Design is complete
  - Board is ~80-90% tested
- Old powering and timing schemes still work
- New power monitors over I2C to FPGA have been demonstrated to work
  - Thus, we know that the power monitors and timing components (clock fanout, MUX, priority encoder, level translator) will work
- New GbE link to SC has been demonstrated to exchange data
- New EtherCAT link shows signs of life and preliminary identification of PTC on EtherCAT bus
  - But more work is needed to understand why full data exchange does not take place
- New PTC<->WIB I2C bus has been electrically tested
  - More FW work on WIB to be done
  - Potential issues with I2C bus hold on non-powered WIBs are already known and mitigations have been discussed with Jack Fried
- A second PTC has been brought up and was provided to BNL for a noise test
- We have a plan to produce 8 more PTCs this year at Penn
  - All electronic components have been procured (except for LTC2945, which could be replaced with LTC2945-1)
  - Prototype front panels have been manufactured, but have a small mechanical error which can be easily corrected



Pick-and-place setup

Full project status

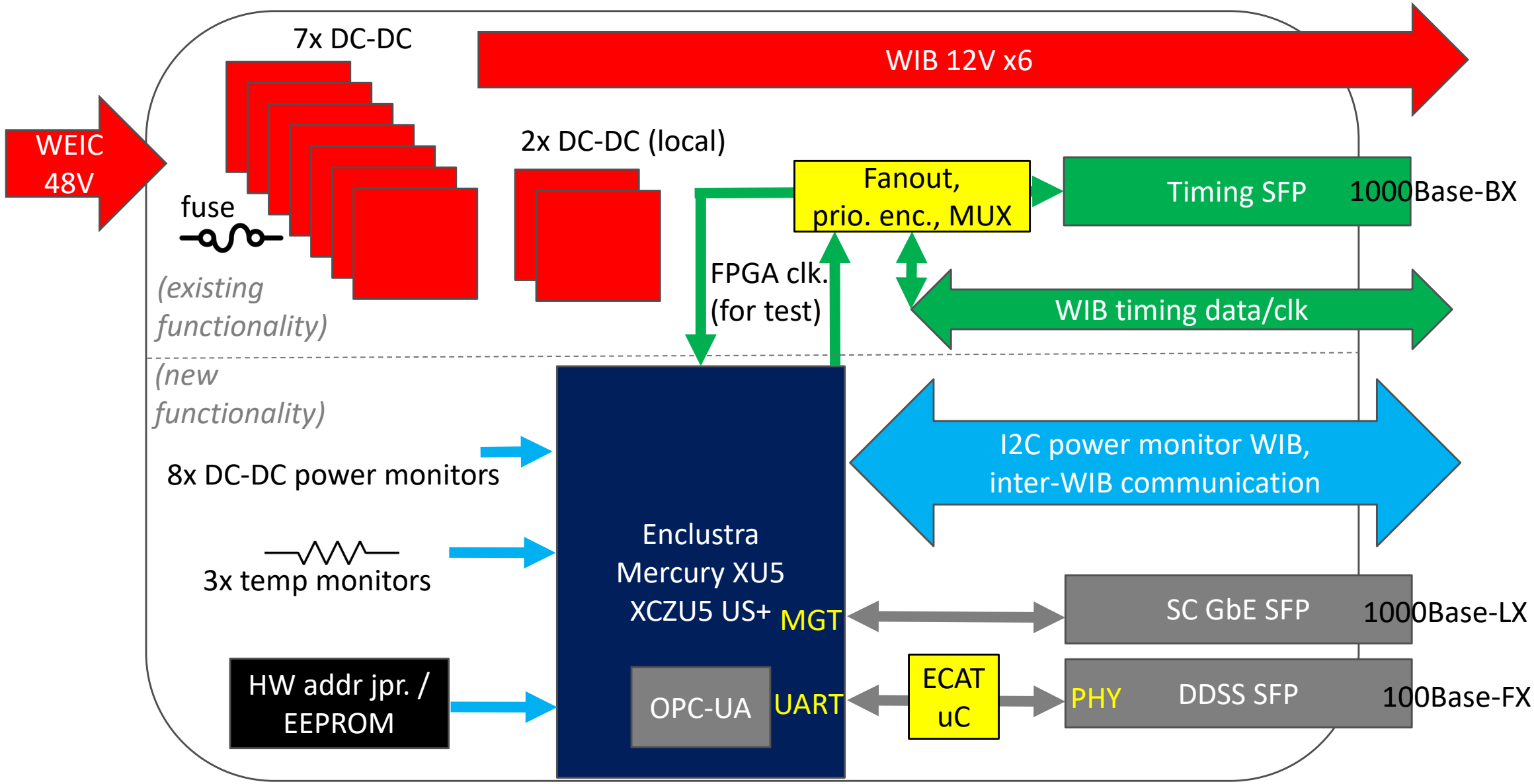
- We need the results of full WEIC tests to qualify some features / components
- We would also like to test a less expensive FPGA mezzanine board (we have these in-house) to take advantage of a potential cost savings opportunity.
  - This also allows us to finalize procurement of long lead time components
- We will need a minor board re-spin (and minor BOM changes):
  - Mostly for some signal polarity reversals and a few minor connections
  - Production layout may have a minor change to accommodate alternate power monitor part variant
- SW and some FW work still to do:
  - Firmware and SoC software (i.e. PetaLinux) estimate ~75% done
  - Software (i.e. EtherCAT uC) estimate ~50% done
- Needs for 2023:
  - 2+1 prototypes for VD Module 0
  - 1 for ICEBERG
  - 1 for BNL
  - Will need 4+1 boards for ProtoDUNE-II-HD or NP04 (schedule unclear)
  - Full detector will have: 150+10 PTCs for HD, and 80+10 PTCs for the VD
- At the moment, the biggest risk is the EtherCAT functionality
  - Which we would like to completely demonstrate before signing off on component purchases

PTC contributions

- Josh Klein: PI at Penn
- Adrian Nikolica: lead engineer, component selection and procurement, FPGA selection, firmware, microcontroller software, low-level Zynq PS software, board debug and bringup
- Godwin Mayers: PCB schematic entry and layout, assembly, rework, board debug and bringup
- Mike Reilly: purchasing support, mechanical design (e.g. front panels)
- Mitch Newcomer, Rick Van Berg, Nandor Dressnandt: internal review support
- Jack Fried (BNL): verification of PTC<->WIB interface, PCB review
- Trevor Nichols (FNAL): help with EtherCAT and Beckhoff integration
- Jason Farrell (BNL): help with mechanical checks and drawings
- Hans Berns (UC Davis): help with providing design files and information from PTCv3B

Backup

Top level PTC v4 block diagram

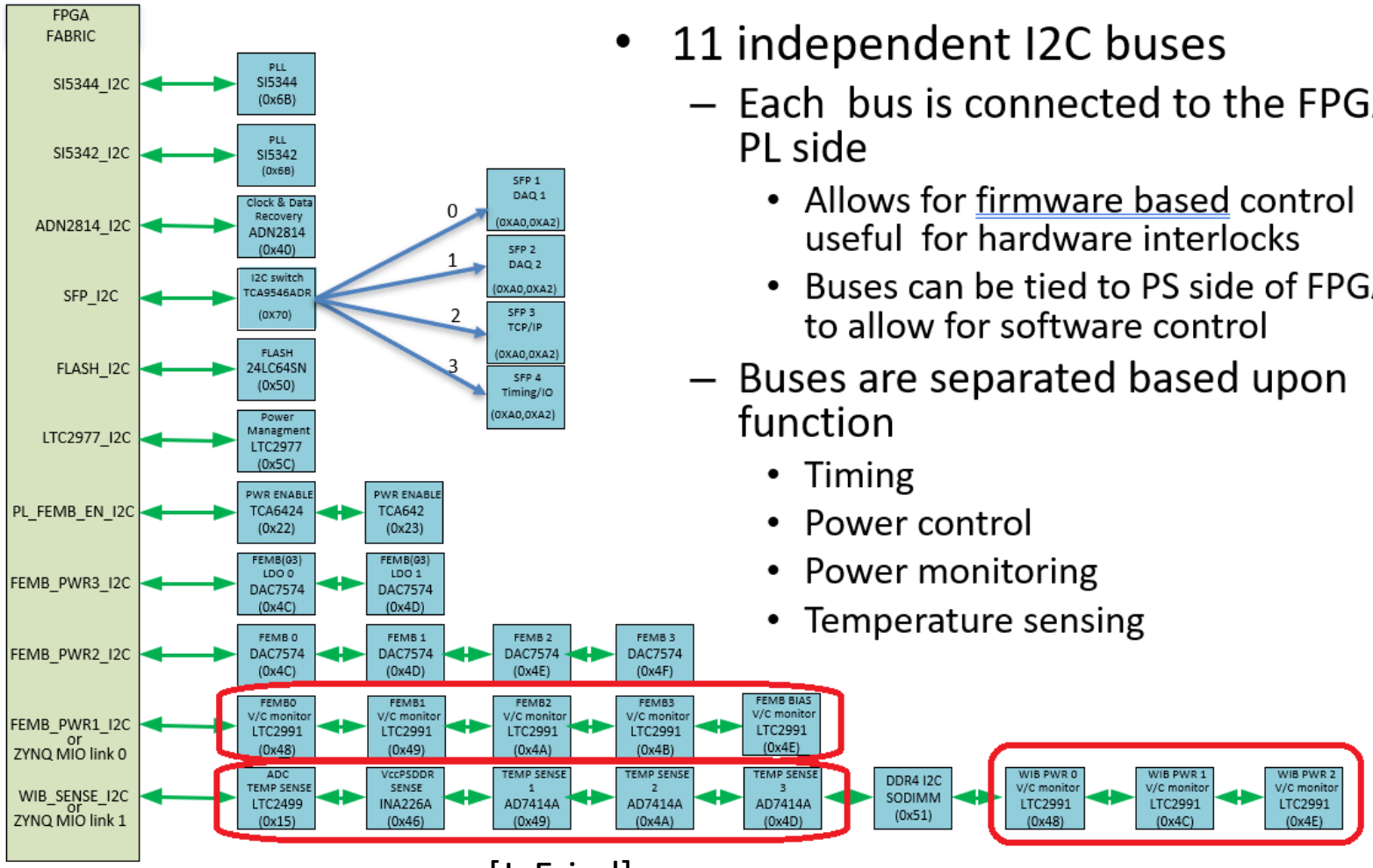


WIB monitored quantities

BROOKHAVEN NATIONAL LABORATORY

DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT

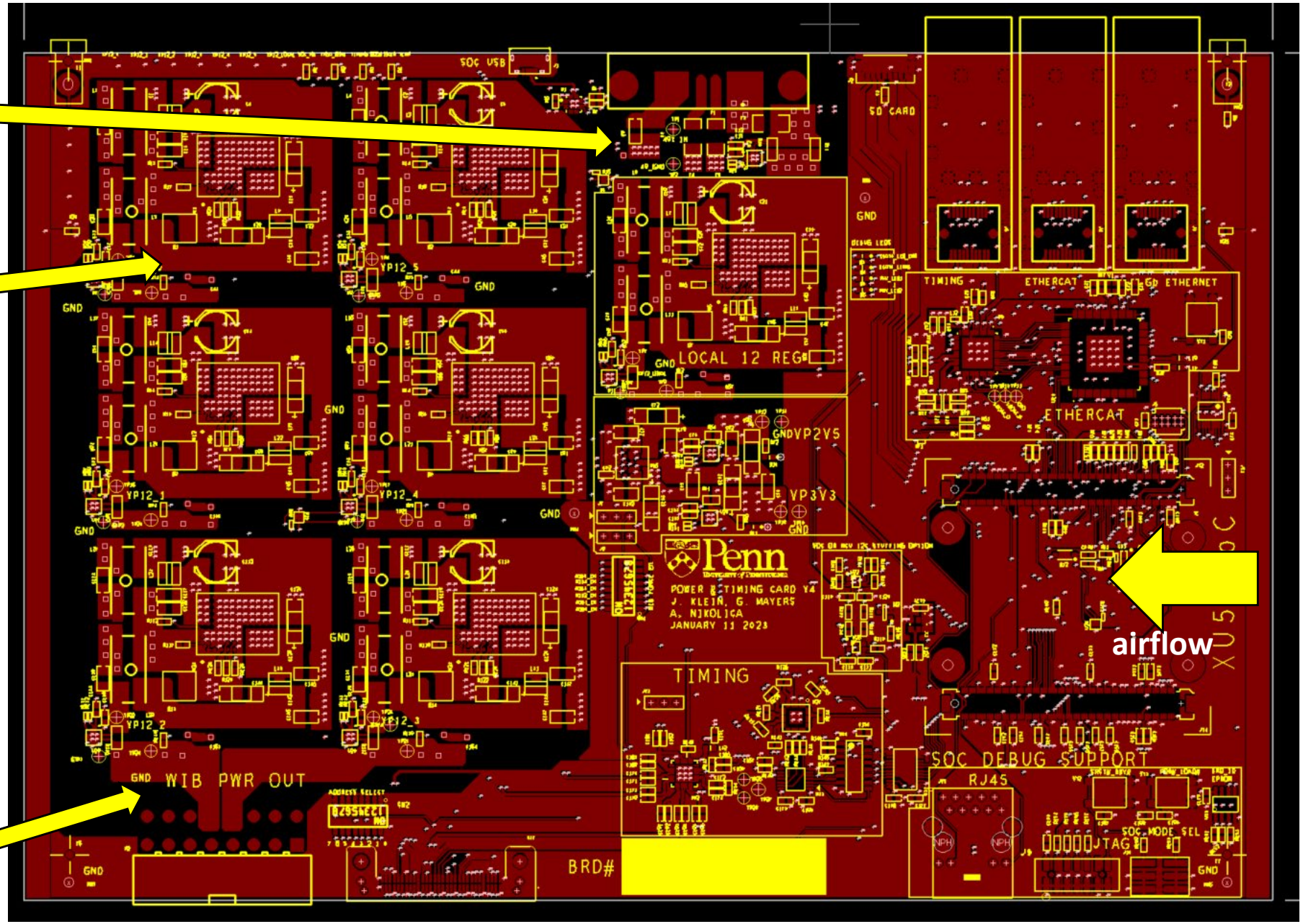
WIB I2C MAP



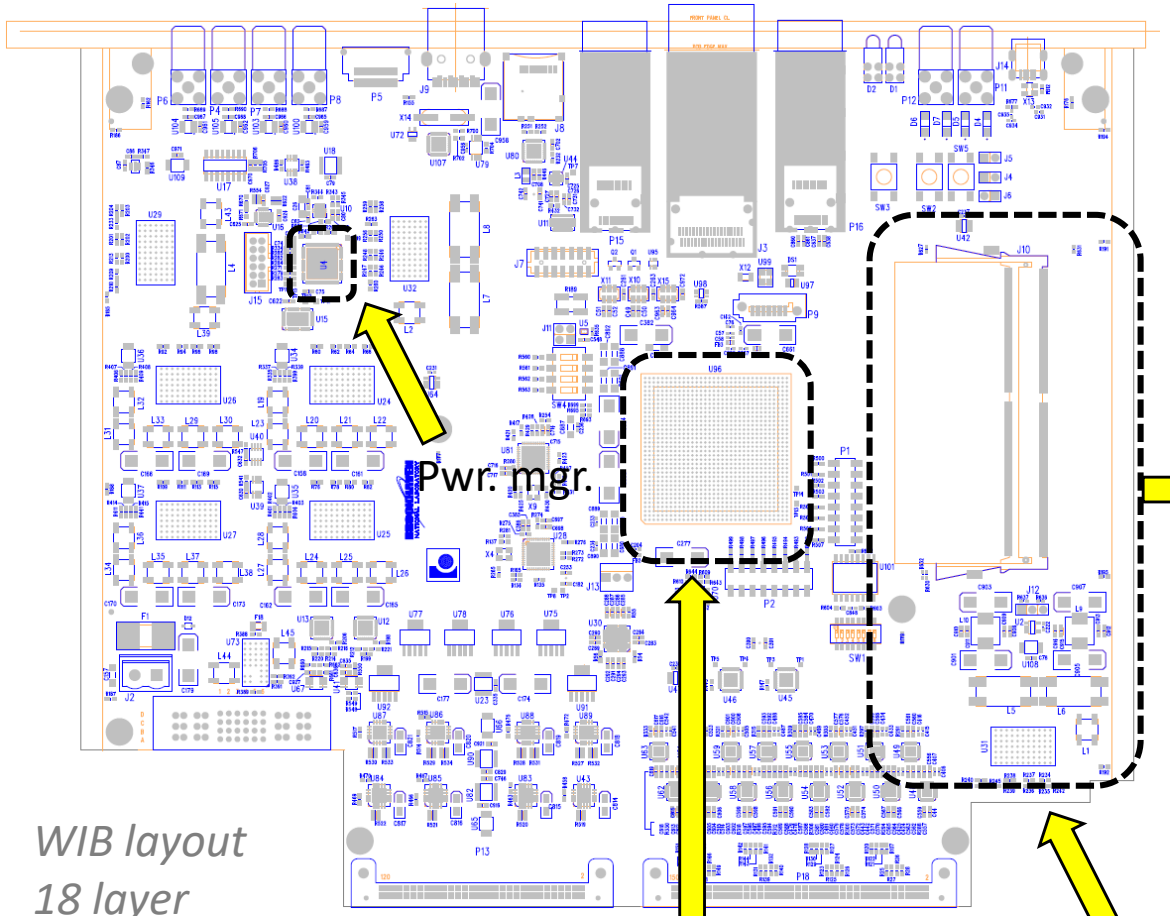
- 11 independent I2C buses
  - Each bus is connected to the FPGA PL side
    - Allows for firmware based control useful for hardware interlocks
    - Buses can be tied to PS side of FPGA to allow for software control
  - Buses are separated based upon function
    - Timing
    - Power control
    - Power monitoring
    - Temperature sensing

Layout

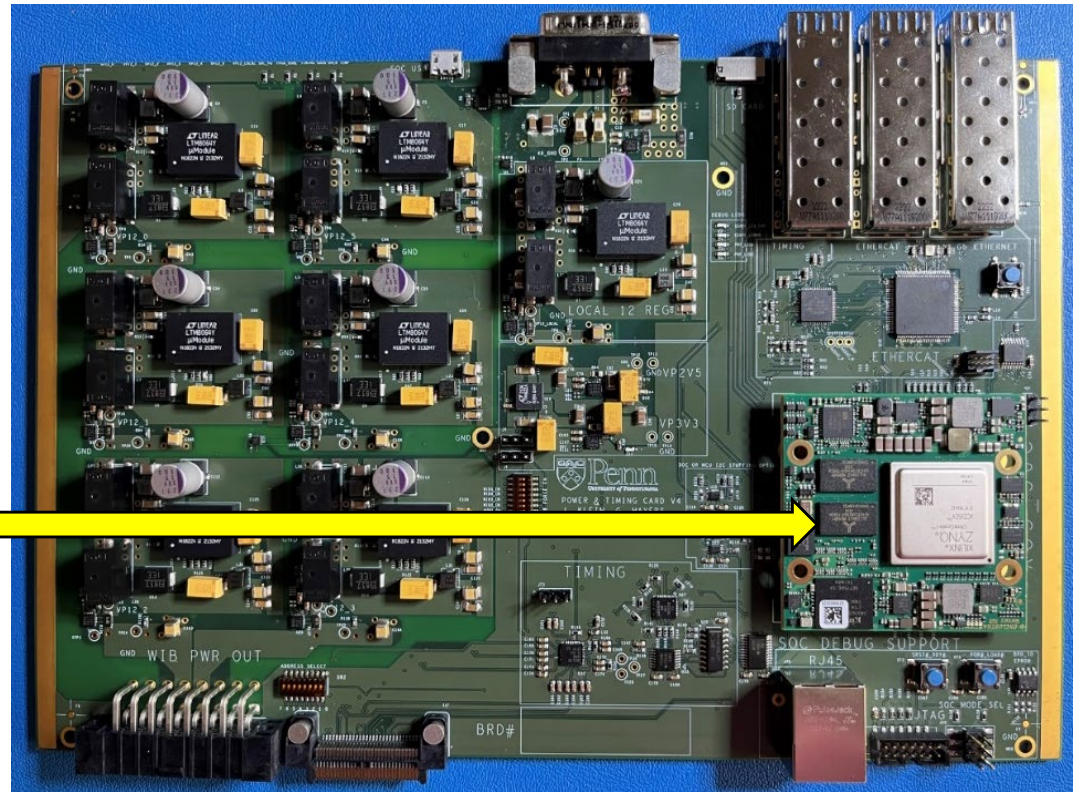
- Main fusing added
- Regulators layed out as modules.
- Moved to other side so SoC does not intrude on power plane
- All trace widths checked for max power capability
- Isolated return paths



Design choices: FPGA



WIB layout
18 layer



PTC v34
10 layer

Roughly to same scale

Zynq
XCZU6CG-1FFVB1156E
~$400 ea.

33mm x 35mm

DIMM memory for Zynq
and power regulator

Zynq needs several voltages (0.85, 0.9, 1.2, 1.8, 2.5V)

Pro / con

- WIB Zynq
  - Availability? Maybe same as Enclustra.
  - Same as WIB, simplifies PetaLinux builds? Not really.
  - Bulk discount? Price on same order as mezzanine.
  - Support? How is this tied to particular part?
  - Most complex routing
  - Most hardware design time
  - Don’t really need biggest part

- Enclustra mezzanine
  - Modular - can re-use if PTC needs re-spin
  - Replaceable during detector life
  - Delivery and price same as WIB Zynq?
  - We have experience with this module at Penn (and have a few spare for ptototyping)
  - Dependent on one vendor. But dependent on Xilinx anyway.
  - Reliability?

Favored option at the moment for prototypes

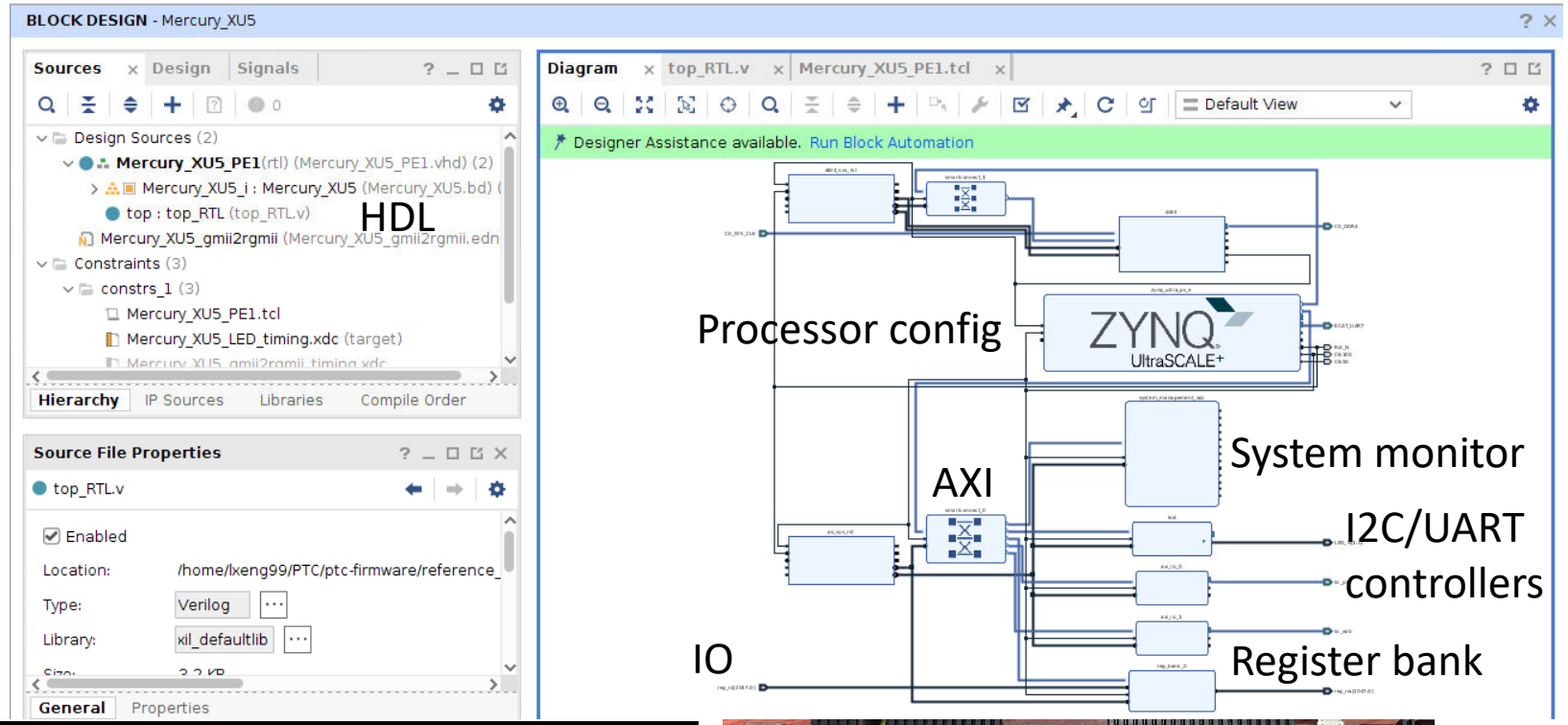
- Microcontroller
  - Easiest and cheapest
  - Probably cannot read in timing info – but we don’t need this.
  - Need EtherCAT support
  - More software effort
    - OPC-UA?

Backplane addressing and IO buffering

- On PTC, we retain the same DIP switch and pullup method of setting the 8-bit address (this is in the requirements)
  - We could aslo drive the backplane address onto the PTB (instead of passive pullups) with the FPGA, with a very small layout change in the production boards. Idea is that PTC stores the address in an EEPROM, instead of using a DIP switch.
  - Should we do this? It's probably easiest to just make this small change.
- Current WIB FW does not have the 4 new backplane addresses wired [7:4] – this is a small firmware change on WIB
- WIBv4 will need buffers (discussion with Jack Fried July 2022):
  - Clock inputs to WIB go to buffers that should tolerate being powered off
  - Clock outputs from WIB should tolerate back-voltage from PTC while WIB is off
  - The 8 IO lines that go directly to WIB 2.5V banks have been shown to source a few tens to hundreds of microAmps of current, which pulls down the voltage levels for address pullups and I2C bus. These are the ones that need to be buffered.
    - In principle, the same question exists for these lines as above: with a small layout change, we could make then bidirectional the repurpose them for driving signals.
- This problem was not forseen on PTCv3B, since all WIBs were always powered up.

Firmware status

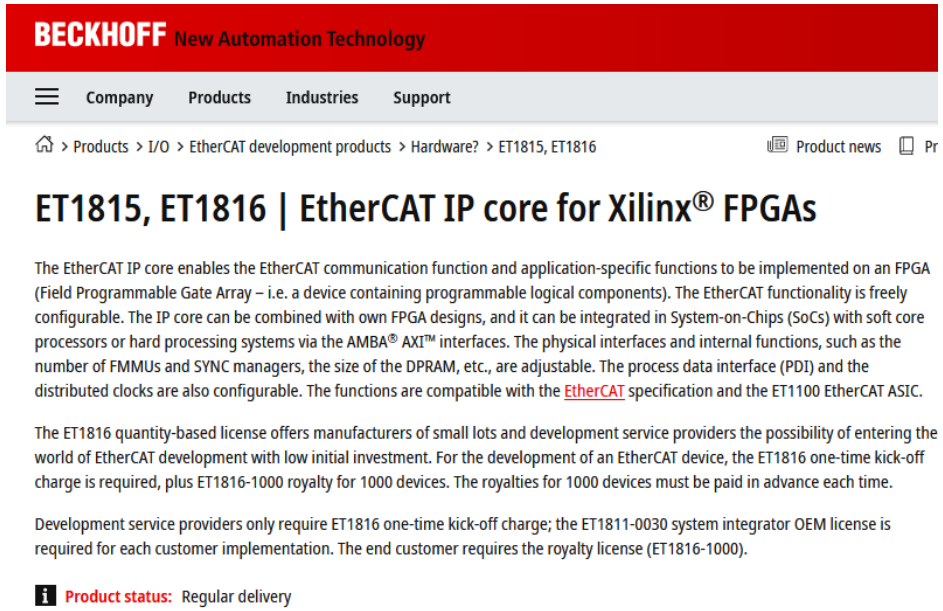
- Snapshot of Vivado project
  - Much work done in software
  - Additional custom firmware can be added in HDL files
- Firmware started on vendor development board
  - Already migrated to PTC and testing succesfully




```
INFO: bitbake petalinux-image-minimal
Parsing recipes: 100% |##################################################################| Time: 0:03:49
Parsing of 2995 .bb files complete (0 cached, 2995 parsed). 4265 targets, 173 skipped, 0 masked, 0 errors
.
NOTE: Resolving any missing task queue dependencies
NOTE: Fetching uninative binary shim from file:///home/lxeng99/PTC/ptc-firmware/reference_design/tempy/ME
-XU5-5EV-2I-D12E_PE1_SD/components/yocto/downloads/uninative/9498d8bba047499999a7310ac2576d07964611849653
51a56f6d32c888a1f216/x86_64-nativesdk-libc.tar.xz;sha256sum=9498d8bba047499999a7310ac2576d079646118496535
1a56f6d32c888a1f216
Initialising tasks: 100% |################################################################| Time: 0:00:04
Checking sstate mirror object availability: 100% |#########################################| Time: 0:00:17
Sstate summary: Wanted 1076 Found 851 Missed 225 Current 0 (79% match, 0% complete)
NOTE: Executing Tasks
NOTE: Setscene tasks completed
NOTE: Tasks Summary: Attempted 3774 tasks of which 2722 didn't need to be rerun and all succeeded.
INFO: copy to TFTP-boot directory is not enabled !!
[INFO] Successfully built project
```

PetaLinux build environment

EtherCAT options



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Company Products Industries Support

> Products > I/O > EtherCAT development products > Hardware? > ET1815, ET1816 Product news Pr

ET1815, ET1816 | EtherCAT IP core for Xilinx® FPGAs

The EtherCAT IP core enables the EtherCAT communication function and application-specific functions to be implemented on an FPGA (Field Programmable Gate Array – i.e. a device containing programmable logical components). The EtherCAT functionality is freely configurable. The IP core can be combined with own FPGA designs, and it can be integrated in System-on-Chips (SoCs) with soft core processors or hard processing systems via the AMBA® AXI™ interfaces. The physical interfaces and internal functions, such as the number of FMMUs and SYNC managers, the size of the DPRAM, etc., are adjustable. The process data interface (PDI) and the distributed clocks are also configurable. The functions are compatible with the EtherCAT specification and the ET1100 EtherCAT ASIC.

The ET1816 quantity-based license offers manufacturers of small lots and development service providers the possibility of entering the world of EtherCAT development with low initial investment. For the development of an EtherCAT device, the ET1816 one-time kick-off charge is required, plus ET1816-1000 royalty for 1000 devices. The royalties for 1000 devices must be paid in advance each time.

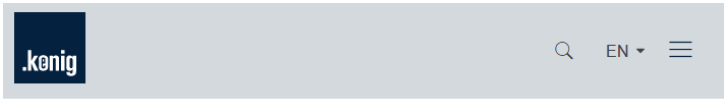
Development service providers only require ET1816 one-time kick-off charge; the ET1811-0030 system integrator OEM license is required for each customer implementation. The end customer requires the royalty license (ET1816-1000).

Product status: Regular delivery

Beckhoff firmware core
License based:
$9,678 initial for 1,000 Xilinx devices
$3,229 per year maintenance

No license within DDSS group

FPGA resource consumption:
~44k LUT (9% of ZU6CG, or 17% ZU5EV)



.konig EN

Home > Products > EtherCAT® Products Overview > KPA EtherCAT Slave Stack

KPA EtherCAT Slave Stack

KPA EtherCAT Slave Stack is a software stack designed to run on microcontrollers, CPUs or DSPs with or without any operating system. It is provided as a source code or compiled library.

General

- Code written in "C"
- Small footprint for 8 and 16 Bit microcontrollers:
  - SAB 80x16x (Infineon)
  - XMC4800 (Infineon)
  - MicroBlaze (Xilinx)
  - Sitara AM335x with integrated ESC in PRUs (Texas Instruments)
  - C2000 (Texas Instruments)
  - STM32 (ST)
  - NIOS II (Intel FPGA/Altera)
  - ARM 3 – 9, ATmega128 (Atmel)
  - PPC 52xx, MPC8536 (Freescale)
- Supported operating systems:
  - Linux (with/without RT-Preemption patch)

Software core

RFQ sent, didn't get a response after several iterations

EtherCAT options, cont.

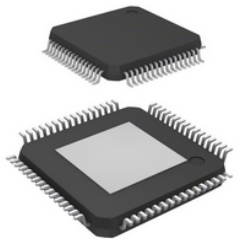


Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

LAN9252I/PT

Digi-Key Part Number	LAN9252I/PT-ND
Manufacturer	Microchip Technology
Manufacturer Product Number	LAN9252I/PT
Description	IC ETHERCAT CTLR 10/100 64TQFP
Manufacturer Standard Lead Time	50 Weeks
Detailed Description	Ethernet Controller 10/100 Base-FX/T/TX PHY SPI Interface 64-TQFP-EP (10x10)
Customer Reference	Customer Reference
Datasheet	Datasheet

ICs:
-Previously mentioned Infineon uC
Low stock

-MicroChip LAN9252
-Beckhoff ET1100
Difficult to find any in stock

-TI Sitaria family uC: low stock

Also option to implement point-to-point connection to another DSS object ?

EtherCAT options, cont.

- Penn joined EtherCAT consortium to get access to some code and documentation
  - We now have Vendor ID **0x00000E19** to be used for PTCs
- There are HW requirements on PHYs (Ethernet transceiver ICs)
  - Of the list of ~40, only a handful were available with reasonable lead times
  - And only 2 that supported Base-FX (fiber, instead of copper)

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2.3.3 Example Ethernet PHYs

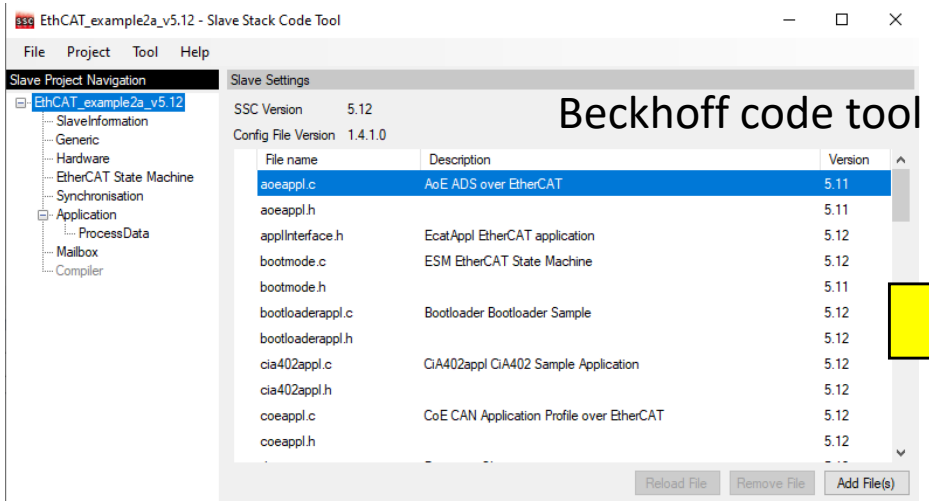
Table 4: Example Ethernet PHYs assumed to fulfill EtherCAT req

Vendor / Device	ET1200 suitable	ET1100 suitable	IP Core suitable	# Ports	Basic HW test[8]	TX_CLK fixed phase[7]	PHY addr.[8]	PHY addr. offset[9]	Link loss reaction time	Enhanced Link Detection	Auto-TX- (IP Core
Analog Devices											
ADIN1200	-	X	X	1	yes	yes (Data sheet)	0-15	0	0.6 µs	recommended[11]	
Broadcom											
BCM5221	X	X	X	1		yes (Data sheet[10])	0-31	0	1.3 µs	recommended[11]	
BCM5222	X[12]	X	X	2		yes (Data sheet)	0-31	0	1.3 µs	recommended[11]	
BCM5241	X	X	X	1	yes	yes (Data sheet)	0-7, 8, 16, 24	0	45 µs	required	
Cortina Systems											
LXT973	(X[13,12])	(X[13])	X	2	yes	Measurement[13]	0-31	0	1.9 ms	required	provisiona
Davicom Semiconductor											
DM9161B			X	1			0-31	0		provisionally	provisiona
DM9162	-	-	X	1		no	0-31	0	1.79ms	required	required
DM9163	-	-	X	1		no	0-31	0	1.79ms	required	required
IC Plus Corp.											
IP101ALF			X	1			0-31	0		provisionally	provisiona
IP101G			X	1			0, 1, x	0		provisionally	provisiona
Marvell											
88E3015/ 88E3018	-	-	X	1		no	0-31	0		provisionally	required
Maxim											
78Q2123 78Q2133			X	1			0/1	0		provisionally	provisiona

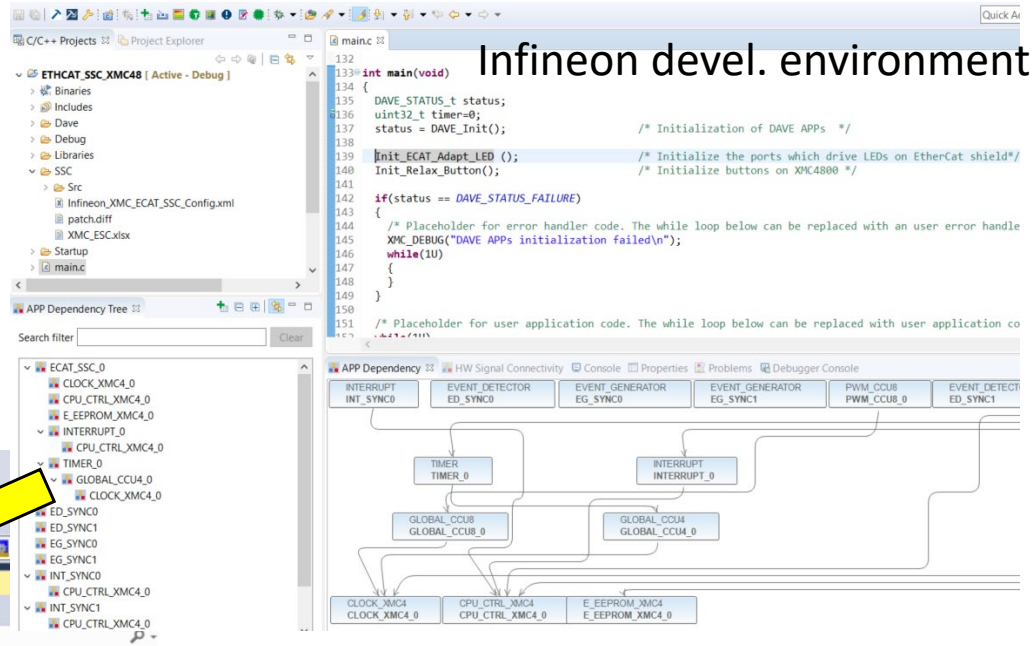
(Link in backup slides)

EtherCAT software

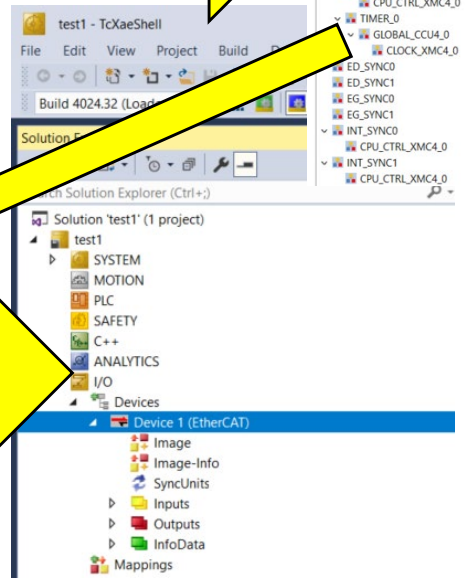
- Proprietary Beckhoff toolchain generates .c files for EtherCAT from Excel/.xml config files
- We got an example working on the development board
  - Still in process of migrating to PTC



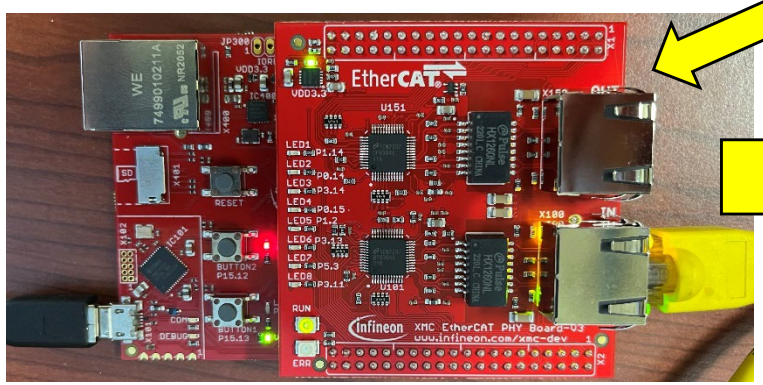
Beckhoff code tool



Infineon devel. environment

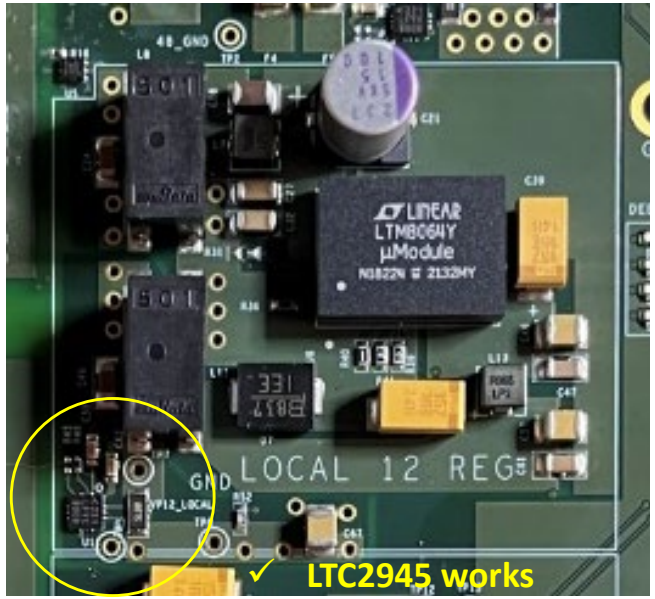


Beckhoff TwinCAT EtherCAT software master

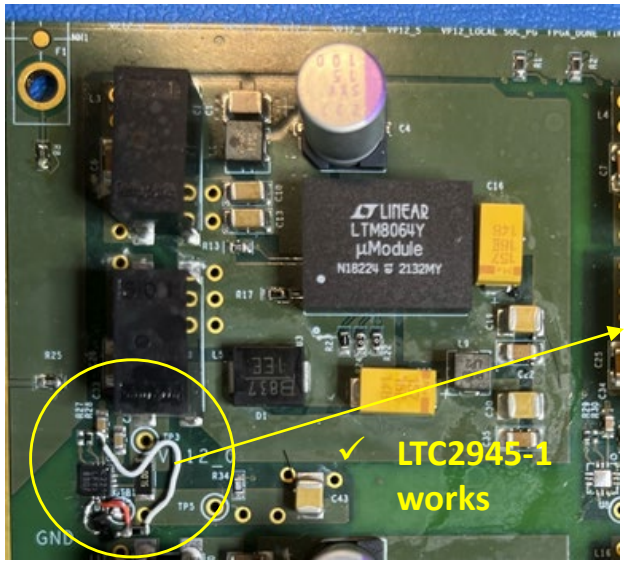


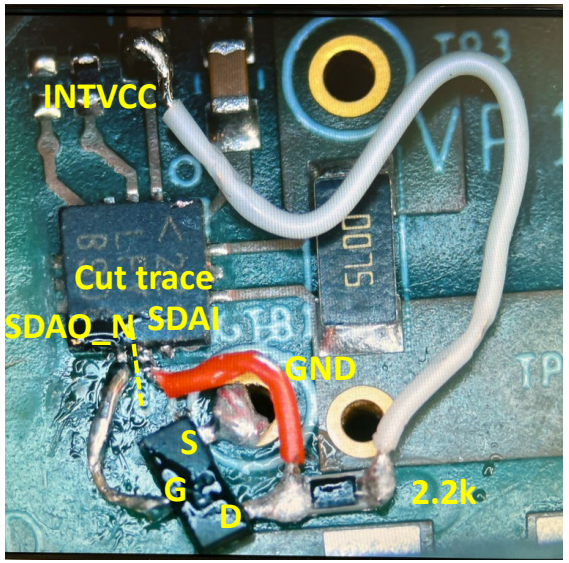
Infineon devel. board

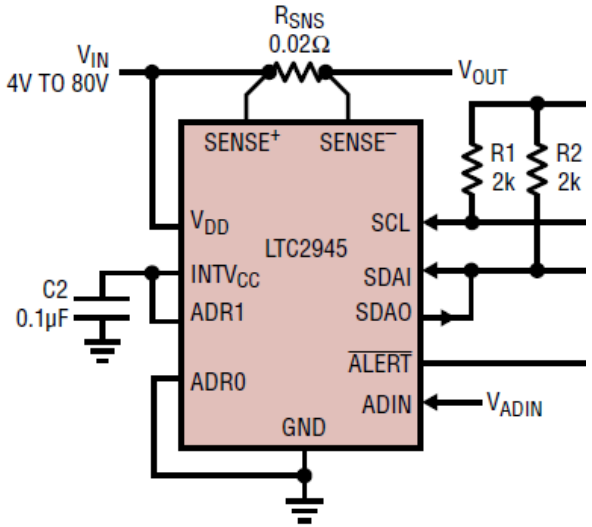
I2C: ability to use LTC2945 or LTC2945-1



OR

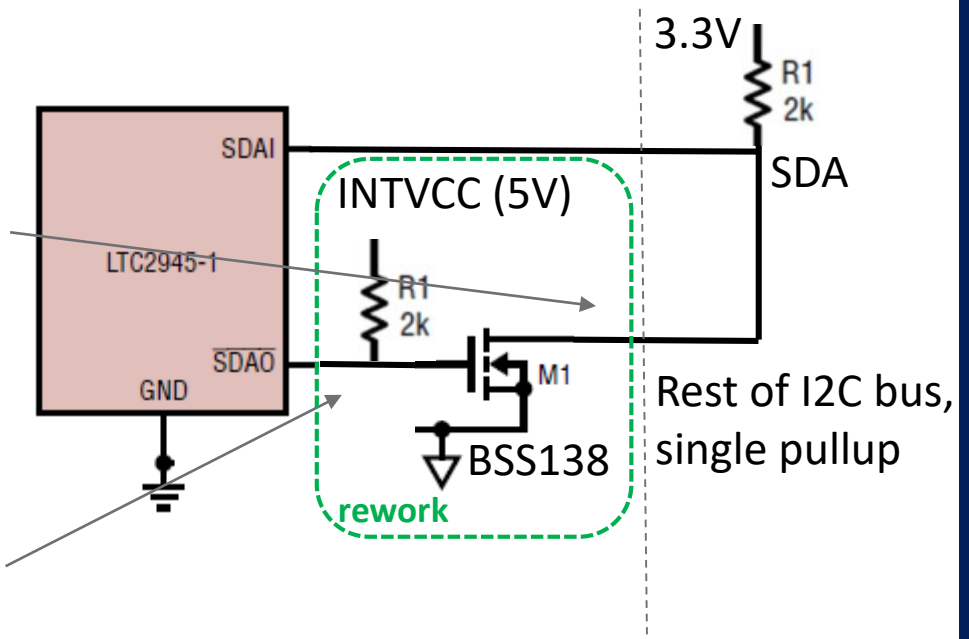






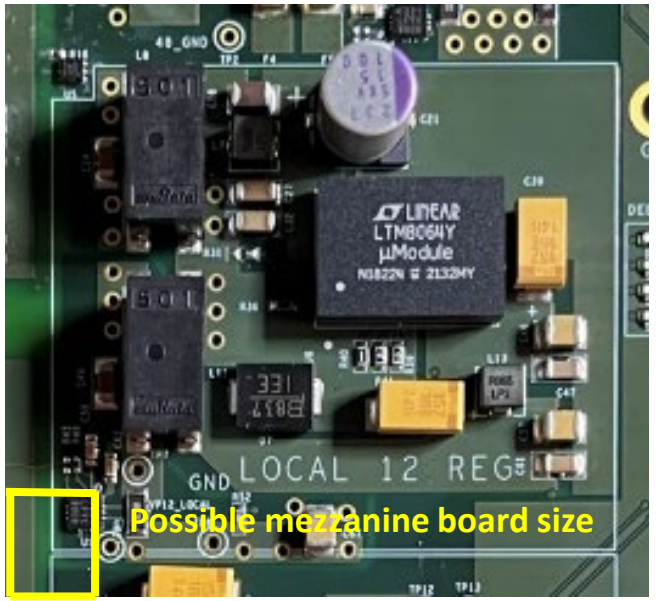
Normally open drain, pulled high by bus controller

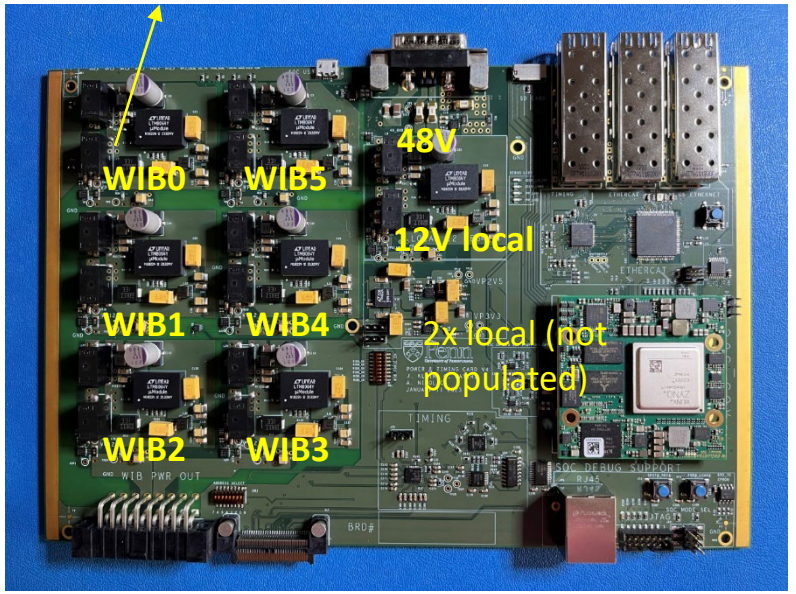
Normally pulled low by IC



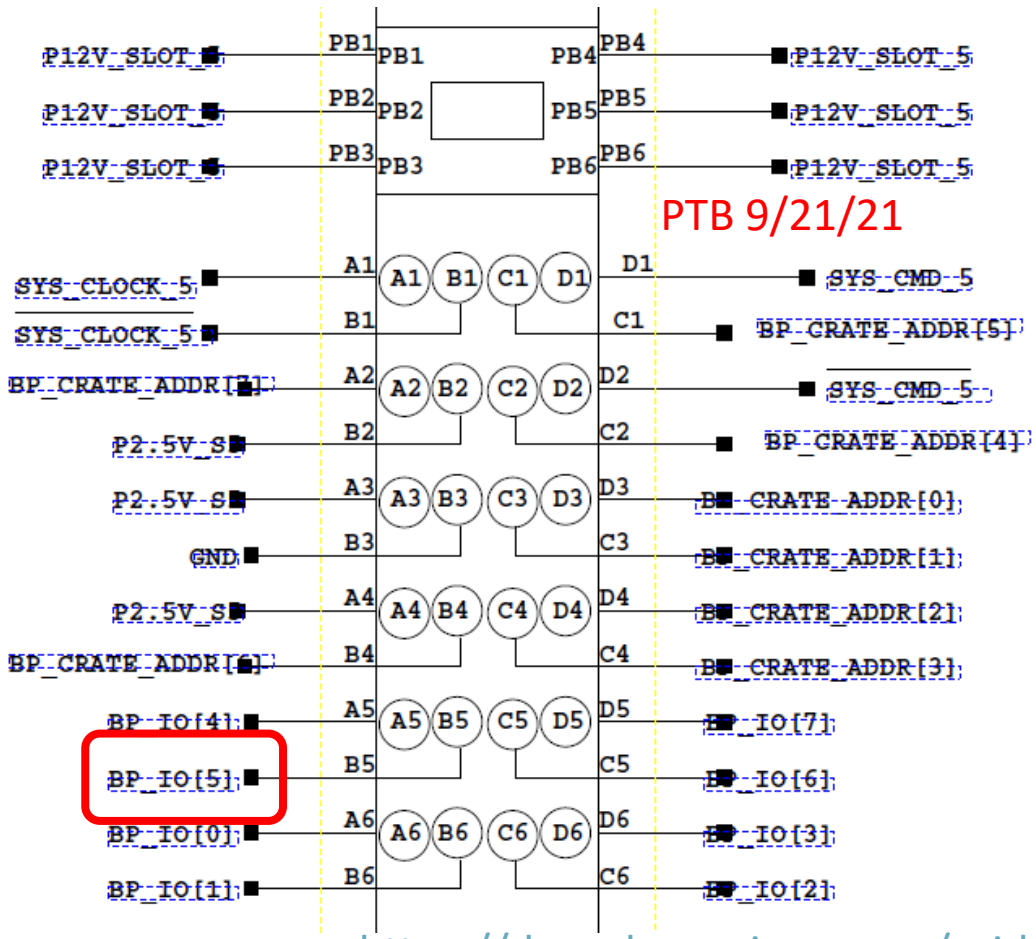
I2C plan

- We have the following very limited stock of LTC2945 (not “-1”) that we could use:
  - From a previous project, and samples from Cheng-Ju and Dave
  - Enough to populate the 48V and 12V local monitors on all 10 PTCs this year
- Send BNL board without other 6 WIB monitors
  - Probably not needed for “noise” test – can just read existing monitors
- For 3rd and 4th PTCs (for FNAL and CERN)
  - Fabricate an adapter board
  - Or rework
  - Can populate remaining 6 * 10 WIB monitors with LTC2945-1
- For the 5th through 10th PTCs (all for CERN NP02 / NP04)
  - Continue to use the adapter board
  - Or re-spin PTC to add I2C fix, and any other fixes we need

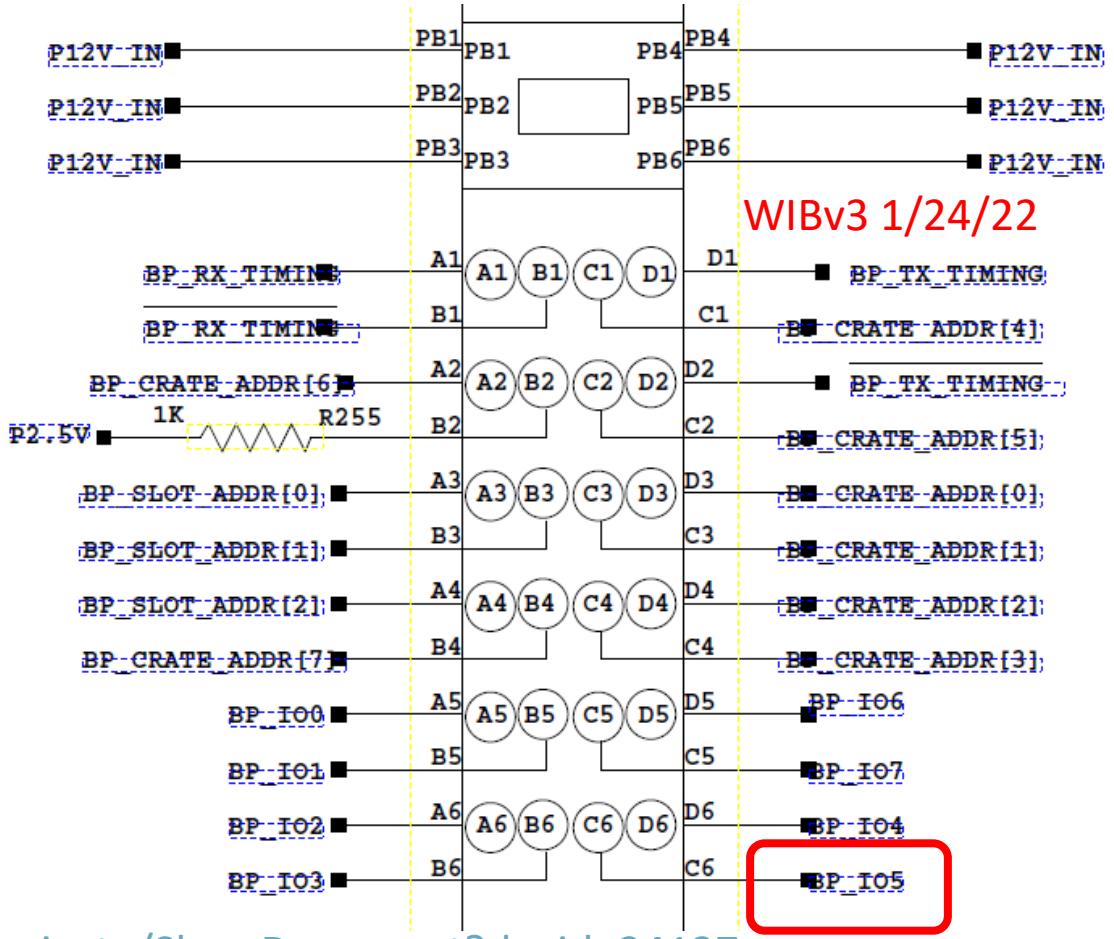




Timing priority encode WIB->PTB



PTB 9/21/21

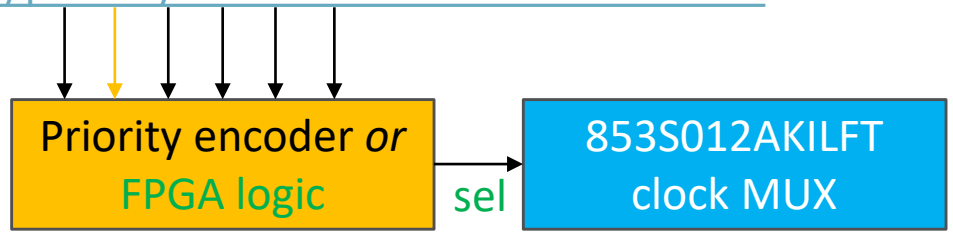


WIBv3 1/24/22

https://docs.dunescience.org/cgi-bin/private/ShowDocument?docid=24127

PTCv4 has followed latest PTB mappings

Taken into account in WIB FW



Timing priority encode WIB->PTB

- There are three possible combinations of hardware:

4.9.1 Control registers (read/write) are listed in Table 6:

Address, hex	Bits in register	Parameter name	Description
A00C0000	15:0	ts_addr	Timing point address
A00C0000	17:16		2'b00 -> "new" PTB with PTCv4 (default) 2'b01 -> "new" PTB with PTCv3B 2'b10 -> "old" PTB with PTCv3B 2'b11 -> not a legal value
A00C0000	28	ts_srst	Timing point reset

- Change WIB lines mappings in FW, with register bit to select option 1) 2) 3), above
  - WIB firmware addition already tested and deployed

- In production, there will only be one valid mapping

WRT old PTC3B -- scrambled			P1
Old net, PTCv3B	Net, new PTB	WIBv3 net	pin #
	GND		60
CLOCK1_N	SYS_CLOCK_1_N		58
CLOCK1_P	SYS_CLOCK_1_P		56
	GND		54
FBEN5	BP_IO[2]	BP_IO[5]	52
FBEN4	BP_IO[3]	BP_IO[4]	50
	GND		48
FBEN3	BP_IO[0]	BP_IO[2]	46
FBEN2	BP_IO[1]	BP_IO[3]	44
	GND		42
FBEN1	BP_IO[4]	BP_IO[0]	40
FBEN0	BP_IO[5]	BP_IO[1]	38
GND	BP_CRATE_ADDR[7]		36
SPARE1	BP_IO[6]	BP_IO[7]	34
SPARE0	BP_IO[7]	BP_IO[6]	32
GND	BP_CRATE_ADDR[6]		30

	WRT new PTCv4 -- scrambled in a different way		
Old net, PTCv3B	Net, new PTB	WIBv3 net	pin #
	GND		60
CLOCK1_N	SYS_CLOCK_1_N		58
CLOCK1_P	SYS_CLOCK_1_P		56
	GND		54
FBEN5	BP_IO[2]	BP_IO[5]	52
FBEN4	BP_IO[3]	BP_IO[4]	50
	GND		48
FBEN3	BP_IO[0]	BP_IO[2]	46
FBEN2	BP_IO[1]	BP_IO[3]	44
	GND		42
FBEN1	BP_IO[4]	BP_IO[0]	40
FBEN0	BP_IO[5]	BP_IO[1]	38
GND	BP_CRATE_ADDR[7]		36
SPARE1	BP_IO[6]	BP_IO[7]	34
SPARE0	BP_IO[7]	BP_IO[6]	32
GND	BP_CRATE_ADDR[6]		30

Mechanics

- Prototype front panels ordered from ProtoCase
- We also have ELMA extruded blanks
- Jason Farrell agreed to update production mechanical drawing

PTCv3B

PTCv4