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U.S. DEPARTMENT OF ENERGY

DUNE FD2-VD BDE FDR QA/QC, ESD, HWDB

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BDE QA/QC, ESD, HWDB documentation

Charge question #10. Has the QC plan document been produced, including a comprehensive ASIC and board ESD handling procedure?

- BDE QA plan: https://edms.cern.ch/document/2606690 (TDR, see section 1.3)
- BDE QC plan: https://edms.cern.ch/document/2815079
  - FEMB QA/QC presentation at ASICs PRR https://indico.fnal.gov/event/59429/contributions/265862/attachments/166717/222170/DUNE%20FEMB%20QAQC_v2.pdf

- BDE ESD protection and control: https://edms.cern.ch/document/2782612
  - ASIC ESD presentation at ASICs PRR: https://indico.fnal.gov/event/59429/contributions/265867/attachments/166715/222169/DUNE%20ASIC%20Test-Stand.pdf

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BDE QC plan

Charge question #10. Has the QC plan document been produced, including a comprehensive ASIC and board ESD handling procedure?

https://edms.cern.ch/document/2815079

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BDE QC plan – key components

- Off-the-shelf items: quality certificates, reputable vendors, reception inspection.
- Custom built products: reputable certified vendors. Fabrication and validation of pre-production quantity of final design products.
- Train and qualify the QC testing personnel.
- Design and produce tools and equipment for QC testing (e.g. RTS, mobile Test Setups, ASICs test board, etc.).
- Develop the QC testing software.
- Develop and document the QC testing procedures and acceptance criteria.
- Develop the assembling, handling, installation, shipping, transportation, etc. procedures (inc. ESD control and prevention).
- QC test and characterize both individual components (as needed), subassemblies, system tests.
- Analyze the information collected during the QC processes.
- Record the test results to DUNE HardWare DataBase (HWDB) and archive the raw data from QC tests for future reference. Part serialization.
- Review the results of QC process at regular intervals and develop corrective actions.
- Feed back the QC testing information to manufacturers to implement corrective actions and achieve the required quality level of deliverables.
- Coordinate the work between different QC testing sites; assure that the QC procedures are applied uniformly across the various sites involved in detector construction, installation, integration.
- Organize QC meetings to share experience between different testing sites, discuss problems, develop corrective action, etc.
- Report to the DUNE management on the results and progress of QC testing.
- Review and, if necessary, update the QC testing procedures.
- Continuous engineering support during production and QC testing.

DUNE TPC electronics PID

	A	B	C	D	E	F	G	H
1	IMPORTANT : It is strongly advised not to use commas or any quotation marks to avoid parsing errors							
2	THE USE OF EMPTY (BLUE) ROWS IS ENTIRELY AT YOUR DISCRETION							
3	**Color**		**Ready for implementation in the parts identifier DB**					
4			**Still under discussion - not to be implemented in the parts identifier DB**					
5			**Already implemented in the parts identifier DB - still in use**					
6			**Already implemented in the parts identifier DB - obsolete, do not use**					
7	**Project**	**System Name**	**System ID**	**Subsystem Name**	**Subsystem ID**	**Item Type Name**	**Item Type ID**	**Notes**
8								
9	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC	001	P5 version preprodution 1	0001	Front end amplifier ASIC P5 version (chips from first pre-produ
10	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC	001	P5B version preproduction 1	0002	Front end amplifier ASIC P5B version (chips from first pre-prod
11	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC	001	to be decided	0003	Front end amplifier ASIC (chips from second pre-production)
12	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC	001	to be decided	0004	because expected serial range may exceed FFFF,
13	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC	001	to be decided	0005	because expected serial range may exceed FFFF
14								
15	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	ColdADC	002	P2 version preproduction	0001	Cold digitizer ASIC (chips from pre-production run)
16	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	ColdADC	002	P2 version batch 1	0002	the production sequence
17	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	ColdADC	002	P2 version batch 2	0003	the production sequence
18	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	ColdADC	002	P2 version batch 3	0004	the production sequence
19								
20	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	COLDATA	003	E4 version preproduction	0001	Cold data serializer ASIC (chips from pre-production run)
21	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	COLDATA	003	E4 version batch 1	0002	depending on the production sequence
22	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	COLDATA	003	E4 version batch 2	0003	depending on the production sequence
23	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	COLDATA	003	E4 version batch 3	0004	depending on the production sequence
24								
25	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC wafers	005	LArASIC P5+P5B version	0001	First preproduction of LArASIC wafers with both P5 and P5B ver
26	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC wafers	005	LArASIC to be decided	0002	Second preproduction of LArASIC wafers with only the xxx versi
27	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	LArASIC wafers	005	LArASIC to be decided	0003	Production LArASIC wafers
28								
29	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	DUNE_COLD wafers	006	ColdADC_P2+COLDATA_E4	0001	Preproduction wafers with ColdADC_P2 and COLDATA_E4 chip
30	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	DUNE_COLD wafers	006	ColdADC_P2+COLDATA_E4	0002	Production wafers with ColdADC_P2 and COLDATA_E4 chips
31								
32	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FPGAs	008	WIB FPGA	0001	First version of FPGA for the WIBs
33	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FPGAs	008	PTC FPGA	0011	First version of FPGA for the PTCs (not implemented yet becaus
34	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FPGAs	008	Test board FPGA	0021	First version of FPGA for the test boards
35								
36	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FEMB	011	FEMB prototype FD1 FEMB v1	0001	First monolithic prototype FEMB with LArASIC P5 ColdADC P2 a
37	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FEMB	011	FEMB prototype FD1 FEMB v2	0002	Second monolithic prototype FEMB with LArASIC P5 ColdADC P
38	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FEMB	011	SAMTEC FEMB FD1	0011	ProtoDUNE-II FEMB with LArASIC P5 ColdADC P2 and COLDATA
39	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FEMB	011	MiniSAS FEMB FD2	0021	ProtoDUNE-II FEMB with LArASIC P5 ColdADC P2 and COLDATA
40								
41	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FEMB components	012	Printed circuit board FD1 FEMB v1	0001	PCB for first monolithic prototype FEMB with LArASIC P5 ColdA
42	D	FD1-HD TPC Electronics and FD2-VD Bottom Drift Electr	081	FEMB components	012	Printed circuit board FD1 FEMB v2	0002	PCB for second monolithic prototype FEMB with LArASIC P5 Co

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DUNE PID: https://edms.cern.ch/ui/file/2505353/5/PartsIdentifier_v6_docx_cpdf.pdf

ESD control and prevention plan

Key elements:

1. **Design in protection** – designing to be as robust as reasonable from the effects of ESD.
2. **Define the level of control** needed for DUNE TPC electronics.
3. **Setup electrostatic protected areas** (EPAs) in which we will be handling ESD susceptible (ESDS) items.
4. **Automate** the QC testing process (Robotic Test Station) to minimize human intervention.
5. **Dissipate and neutralize** electric charge by grounding and the use of conductive and dissipative static control materials (wrist bands, antistatic mats).
6. **Reduce Electrostatic charge generation** by reducing and eliminating static generating processes.
7. **Protect products** from ESD with proper grounding or shunting and the use of static control packaging and material handling products.
8. **Define procedures** (QC testing, handling, transportation, installation).
9. **Train personnel**.

https://edms.cern.ch/document/2782612

Electrostatic Discharge control for TPC electronics — PURPOSE AND

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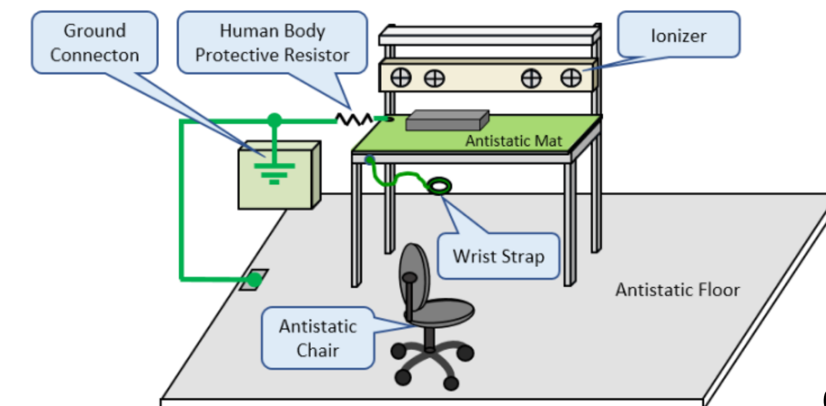

ESD protection for ASICs / CE boards

Indico:59429

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Summary

- BDE consortium has a comprehensive QC plan in place in order to produce quality CE parts that meet the requirements of the DUNE experiment.
  - QC testing at MSU, LBNL, UC-Irvine, Fermilab, U. Cincinnati, Iowa State U., U. Florida, U. Pennsylvania, BNL, CRP production sites, SURF.
  - Work in progress on developing a software interface/procedures/tools for uploading the QC test results to the centralized DUNE Hardware Database (HWDB).

- BDE consortium has a plan in place for continuous ESD control and prevention – ASICs -> FEMBs -> CE boxes -> Shipping -> Installation -> APA/CRP handling (as a single document now – in response to previous review recommendation).