DEEP UNDERGROUND NEUTRINO EXPERIMENT

Penn
University of Pennsylvania

PTCv4 Design Status

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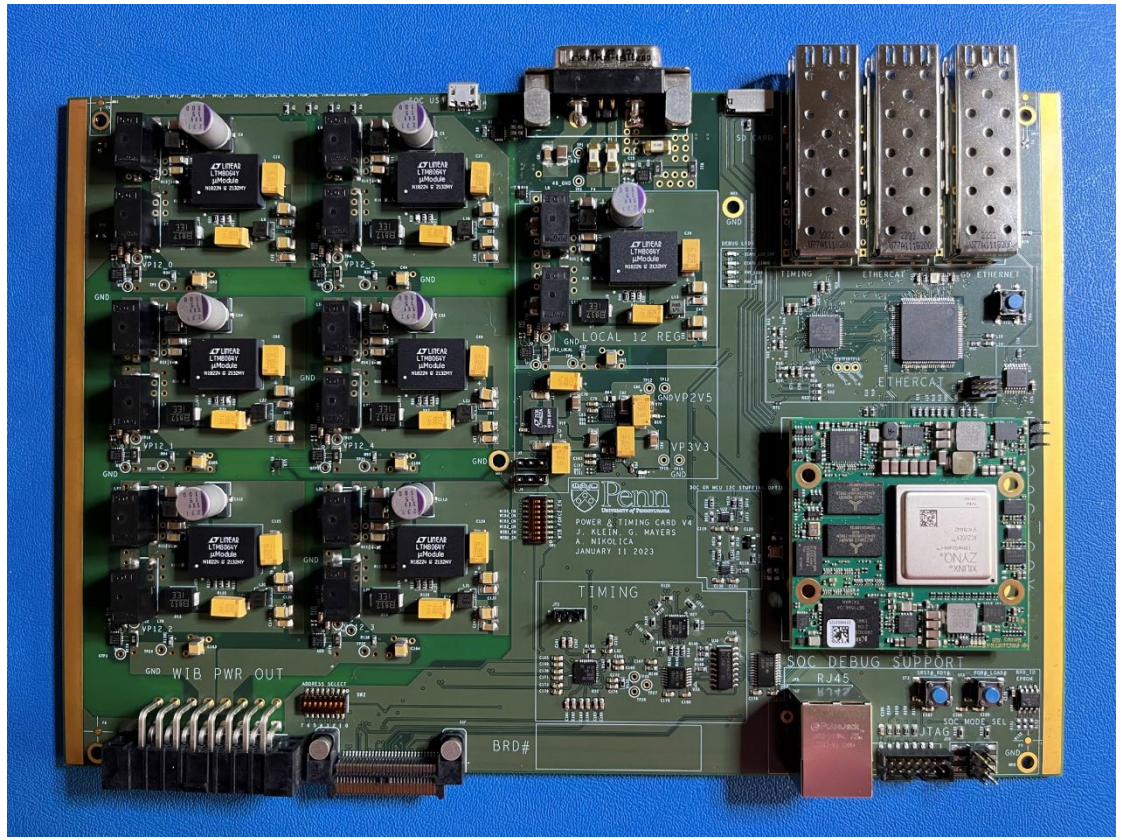
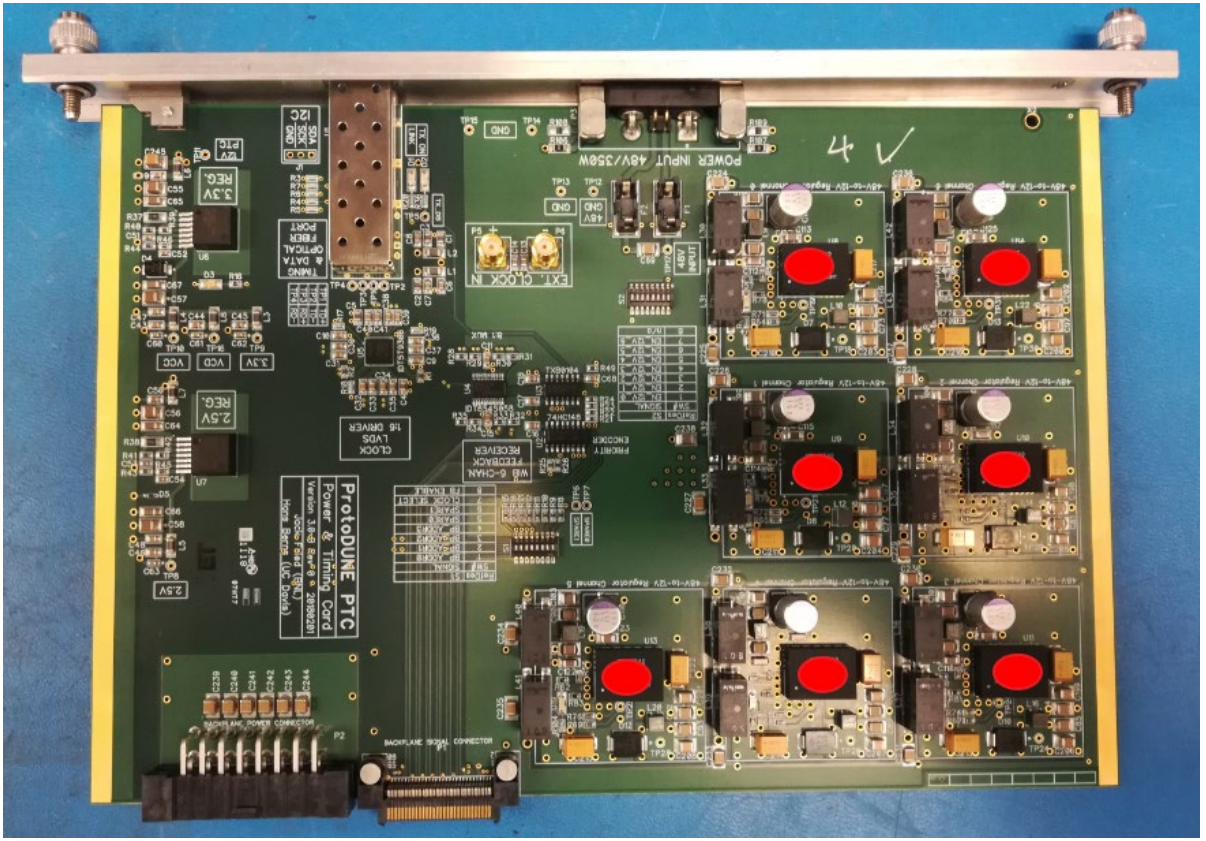
Introduction

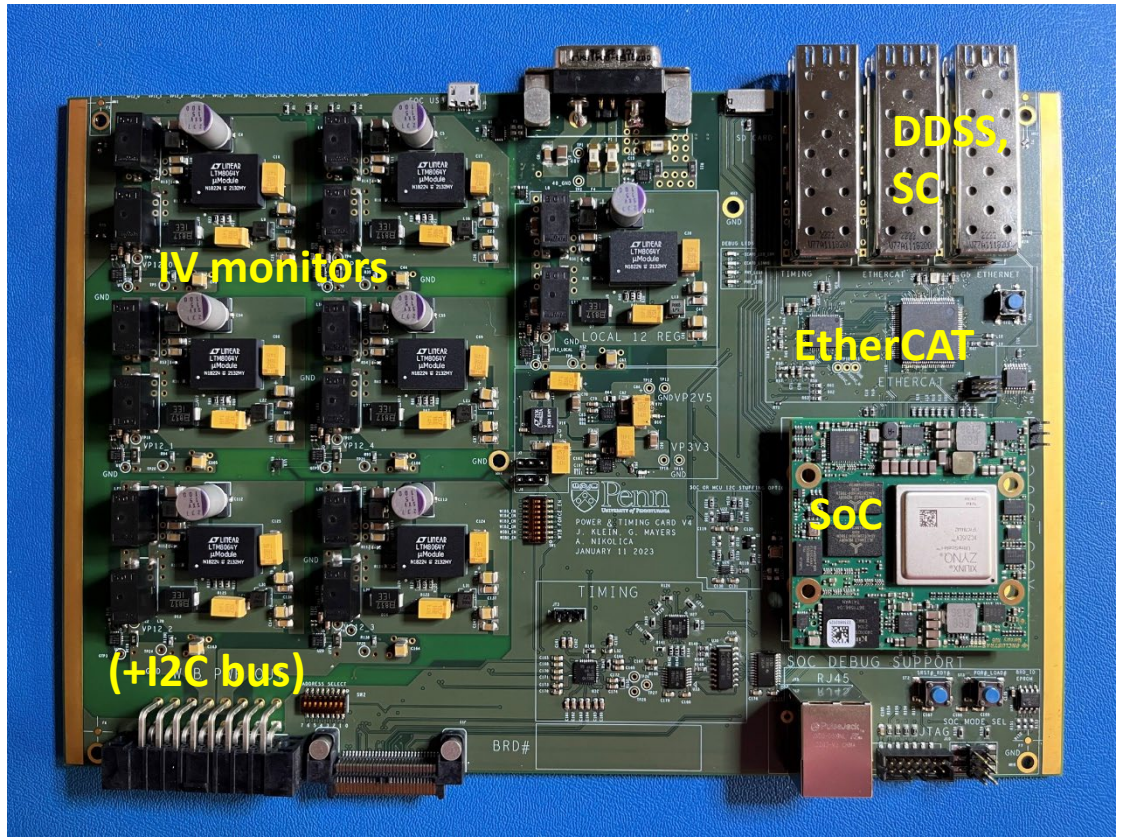
- The current Power and Timing Card (v3B) provides power to 5-6 WIBs in a crate, and distributes timing information
- Reasons for re-designing the PTC:
  - Monitoring of local voltages and temperatures
  - Slow Control (SC) interface
  - DUNE Detector Safety System (DDSS) interface
  - Individual WIB control* and/or communications
- This presentation will focus on:
  - Assembly and bringup
  - List of tested features so far
  - Test stand
  - TODO list
  - Final FPGA choice
  - Parts procurement and assembly



Existing WIBv3 may not be able to be powered down in a crate with PTCv4 – details in backup slides

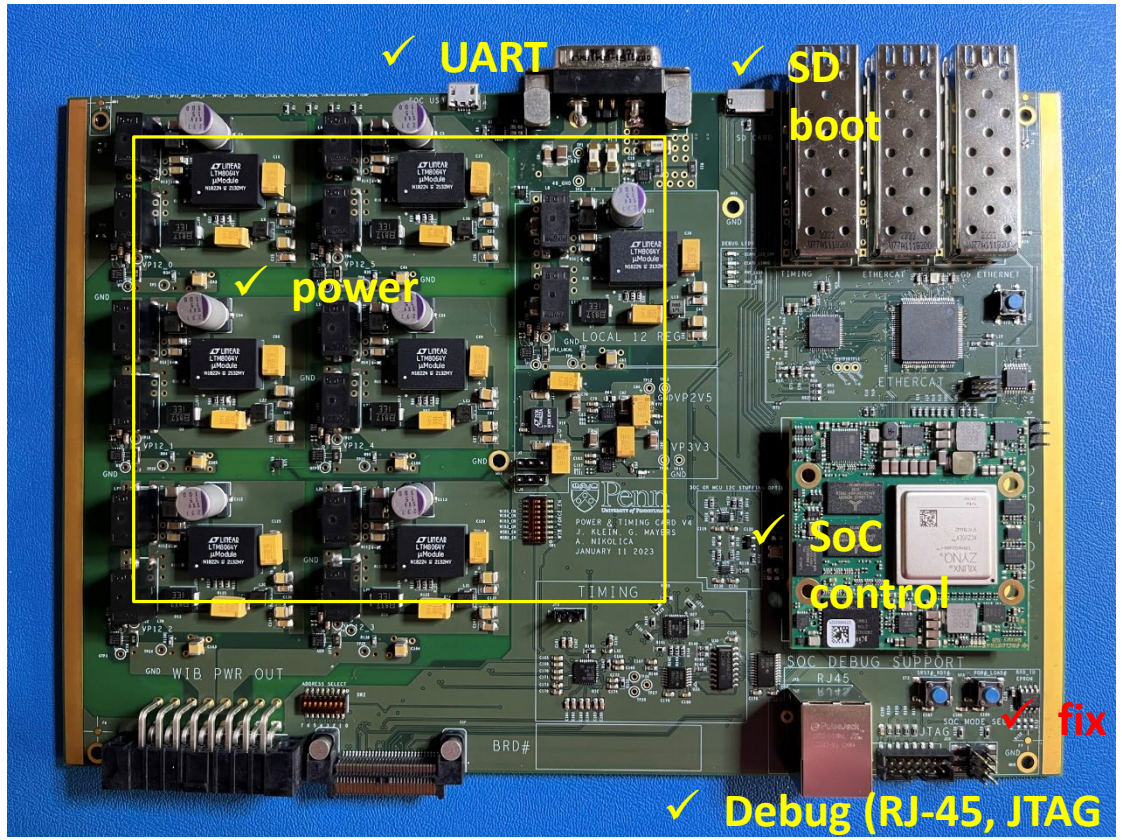
PTCv3B and PTCv4 side-by-side





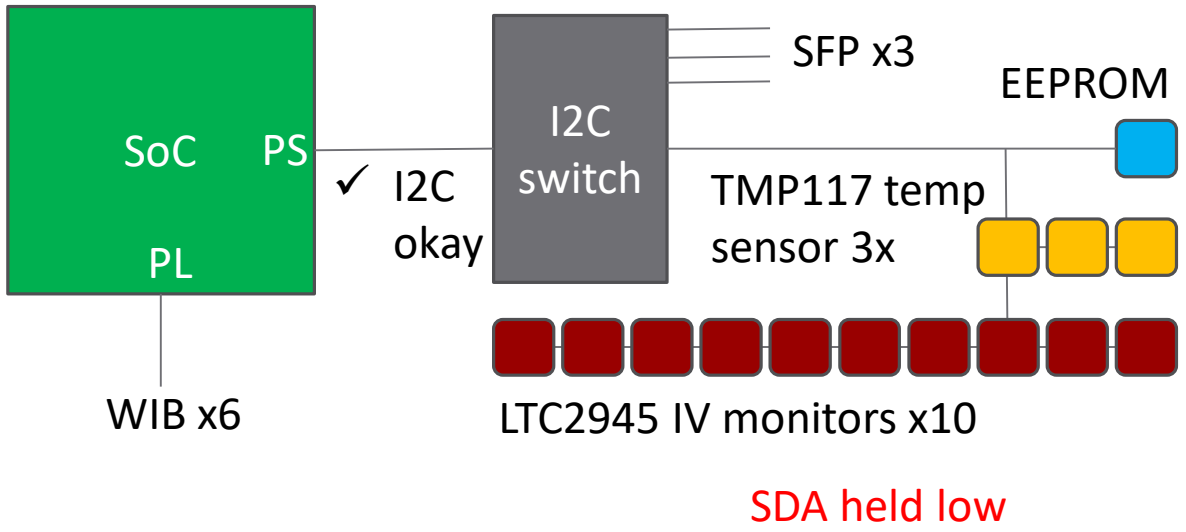
List of tests to date

- All six 12V regulators power up, can be enabled via FPGA register bit
- Local 12V, 3.3V, 2.5V power all ICs with no excessive current
- Enclustra Mercury XU5 mezznanine (Zynq 5EV Ultrascale+):
  - Boots via SD card
  - Front panel UART, debug RJ-45, and JTAG work
  - SFP status signals can be read in via FPGA register bits
- Errata:
  - One minor footprint error on pushbutton reset switches; mitigation in place for prototypes
- Working on I2C and GbE bringup



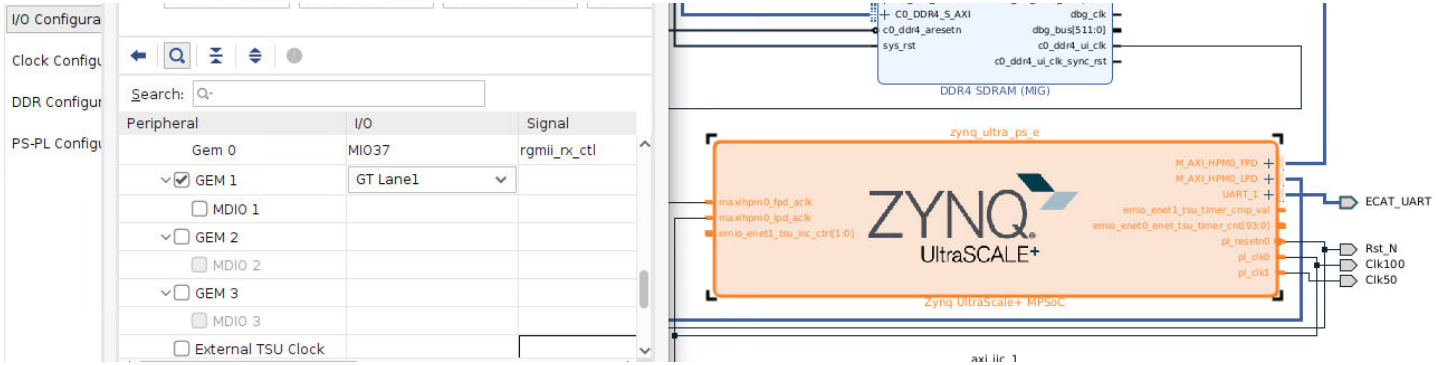
Currently working on: I2C reads

- There are a few I2C busses
  - Zynq PS I2C works to I2C switch
- SDA held low on bus with PTC temp and IV measurements
  - Double checked schematics, layout, bare board connectivity
  - Confirmed not a direct short
  - Have isolated EEPROM and temp sensors
  - Confirmed IV monitors are powered
- In process of debugging which of the 10 sensors is holding line low
  - Could also assemble second board and try



Currently working on: GbE to SC

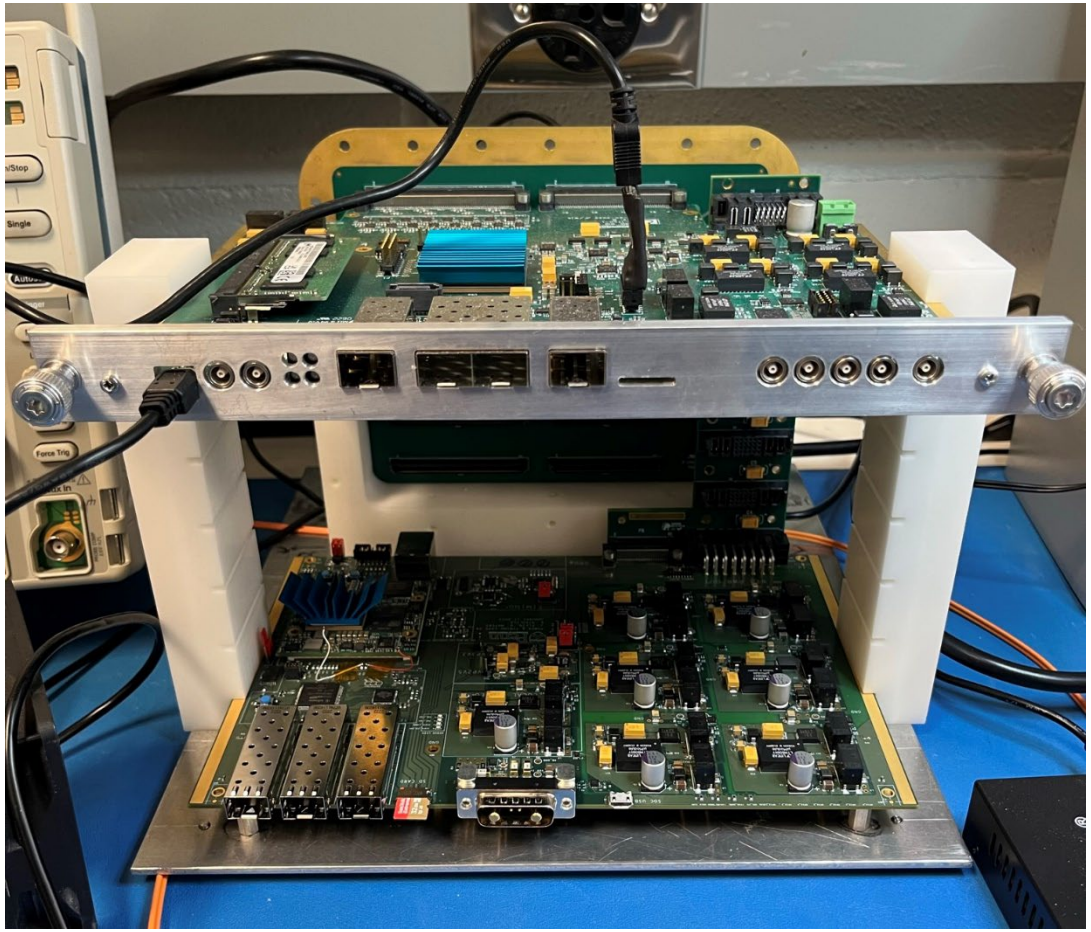
- SC GbE is on front panel SFP
- Configured in Zynq settings
  - PS transcievers
  - Same HW/config as WIB
- Using 10GTek A7S2-33-1GX1GT-SFP/GT3 fiber-to-copper converter
  - Same exact HW as WIB test stand
- Can see device come up, but cannot ping
- Verified reference clock is okay
- Need to dig further with Wireshark
- Possible PetaLinux issue?



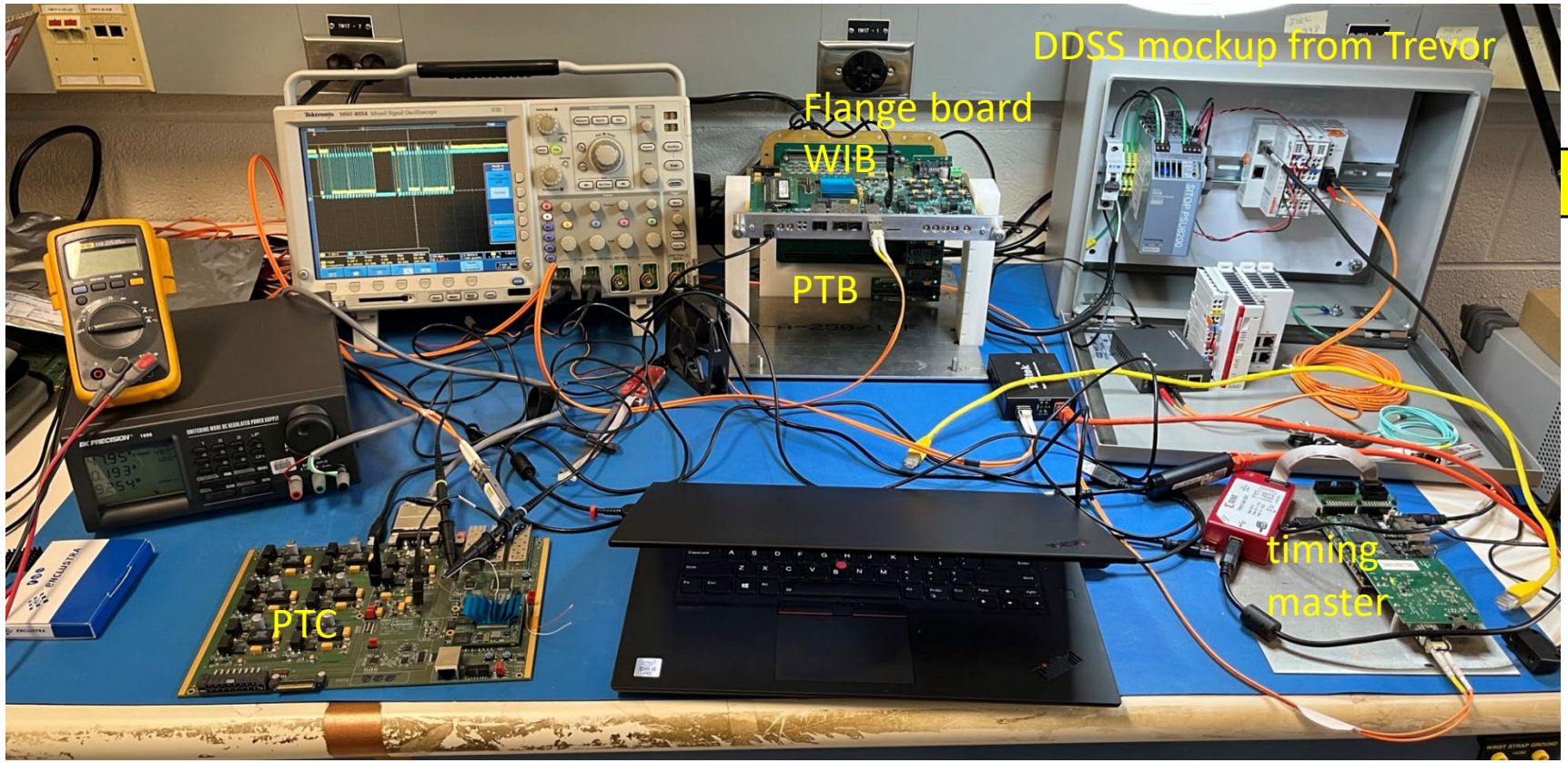

```
root@ptc:~# ifconfig
eth0      Link encap:Ethernet  HWaddr C6:10:4A:82:8C:13
          inet6 addr: fe80::c410:4aff:fe82:8c13/64 Scope:Link
          UP BROADCAST MULTICAST  MTU:1500  Metric:1
          RX packets:118 errors:0 dropped:0 overruns:0 frame:0
          TX packets:51 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:13135 (12.8 KiB)  TX bytes:8082 (7.8 KiB)
          Interrupt:38

eth1      Link encap:Ethernet  HWaddr 00:0A:35:00:22:01
          inet addr:192.168.200.12  Bcast:192.168.200.255  Mask:255.255.255.0
          inet6 addr: fe80::20a:35ff:fe00:2201/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:44 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:0 (0.0 B)  TX bytes:8609 (8.4 KiB)
          Interrupt:39

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:80 errors:0 dropped:0 overruns:0 frame:0
          TX packets:80 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:6080 (5.9 KiB)  TX bytes:6080 (5.9 KiB)
```

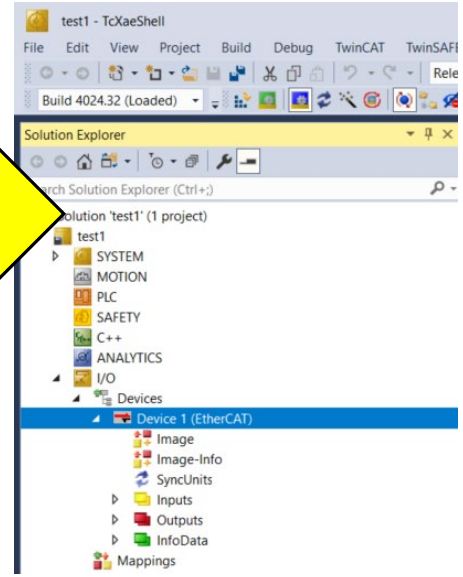
Currently working on: powering a WIB

- Carefully checking new interfaces
  - I2C
  - Level translation on backplane addressing and timing priority encode
  - Power sequencing
- PTC-only tests:
  - SC and DDSS connections
  - On-board I2C read of IV monitors
  - Initial temp. measurements under load
- “One-WIB” tests:
  - Mechanical check with PTB
  - Powerup check for one WIB
  - I2C communications with one WIB
- Other tests that require a real WEIC:
  - Front panel mechanical check
  - Power and temp. testing with 6 WIBs
  - “Noise” measurements



Penn test stand

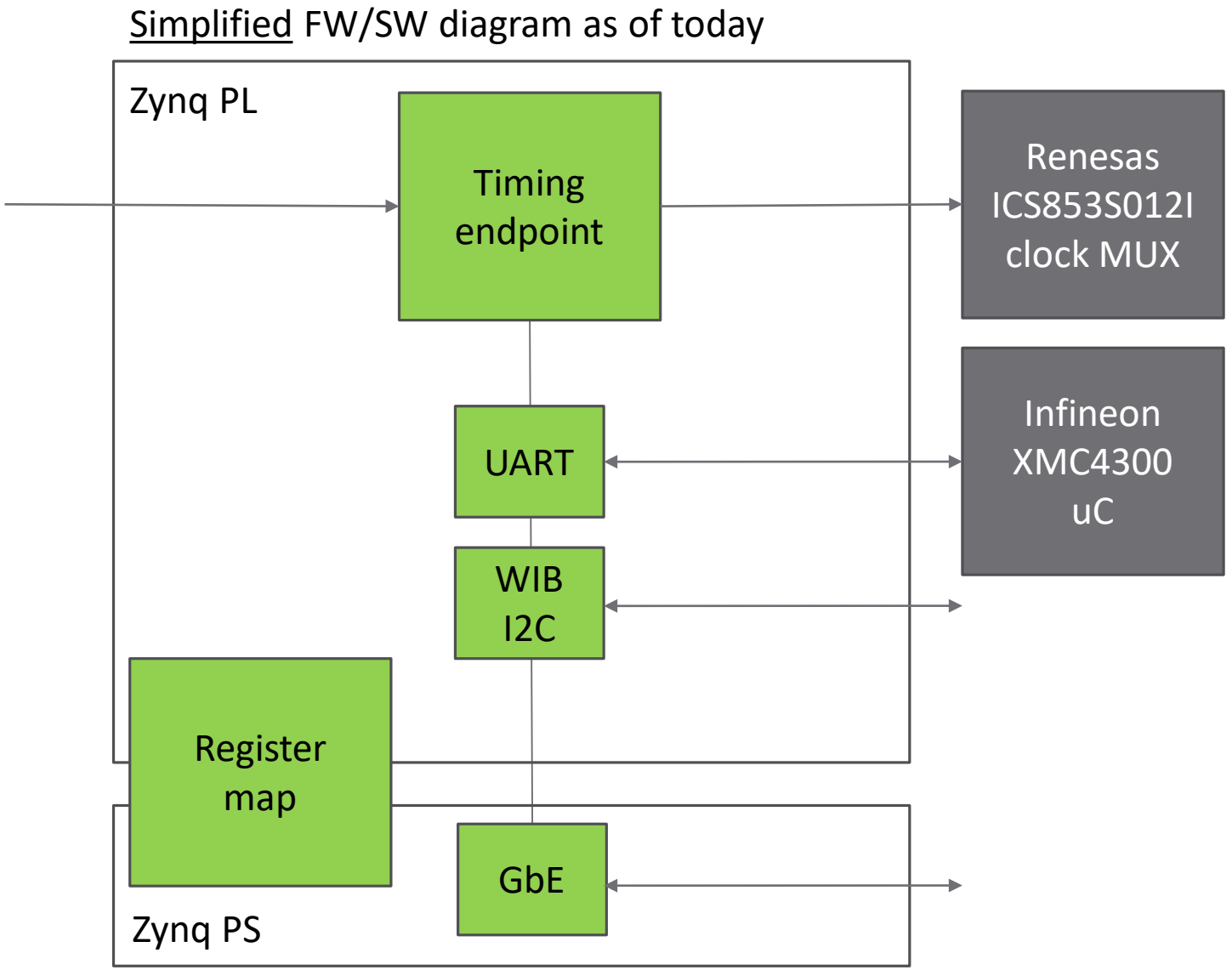




Beckhoff TwinCAT
EtherCAT software master

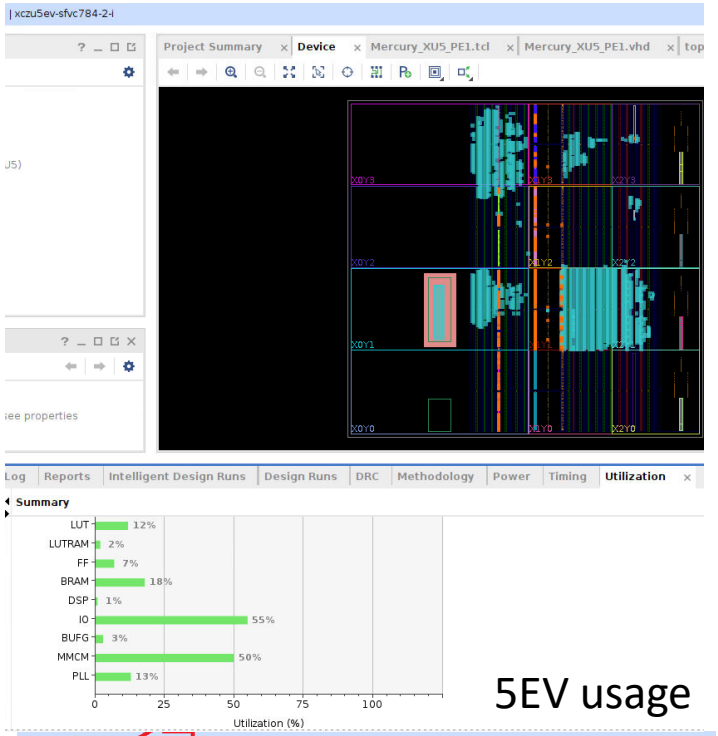
Firmware

- Firmware is work in progress
  - But looking fairly simple so far
- Lots of work probably done in SW

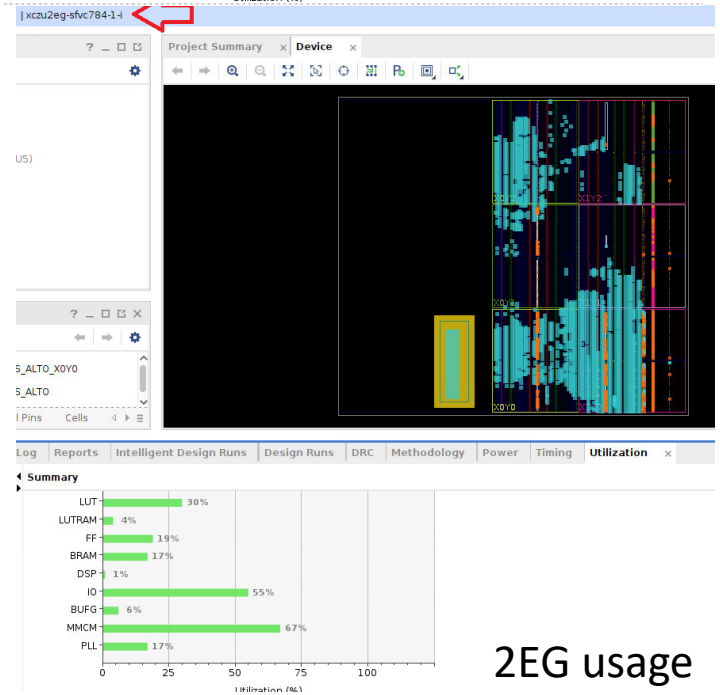


FPGA choice

- FPGA history
  - Originally suggested to use same FPGA as WIB
  - Agreed on using commercial mezzanine:
    - Enclustra ME-XU5-5EV-2I-D12E (prototypes)
    - Alternate: ME-XU5-2EG-1I-D11E*
    - Same Xilinx Zynq UltraScale+ FPGA family as WIB
    - Simple to design with, upgradeable during detector life
  - Option to use a custom mezzanine or on-board FPGA will be evaluated?
    - Mitigate concerns about reliability and switching noise
- Final FPGA choice
  - Depends on resource usage
  - May be able to go with alternate choice at lower cost
  - Will evaluate as testing proceeds



5EV usage



2EG usage

**Might require hardware additions / modifications*

Mechanics

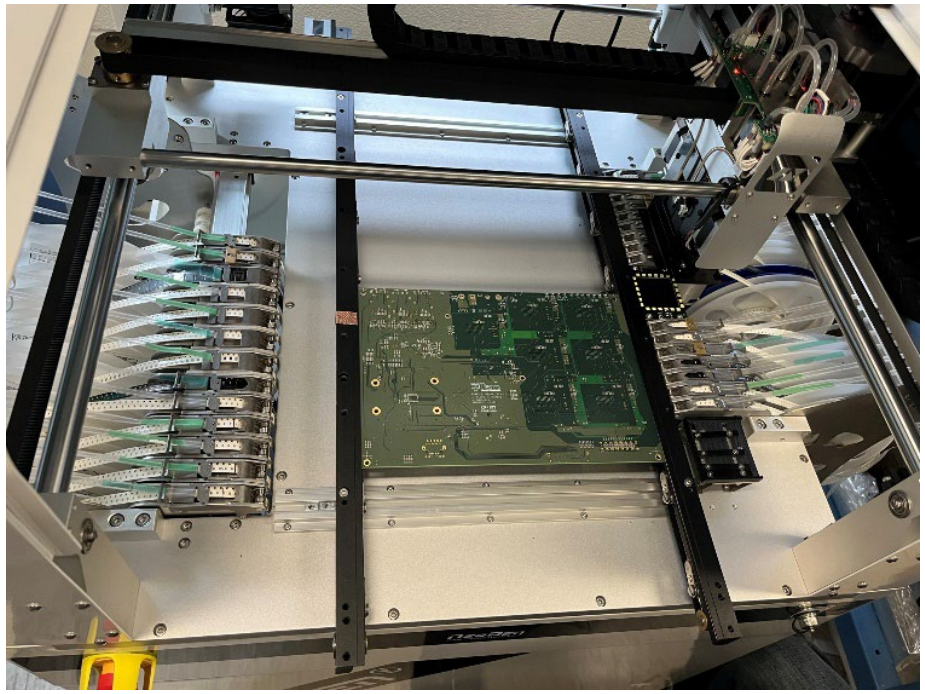
- Prototype front panels ordered from ProtoCase
- We also have ELMA extruded blanks
- Jason Farrell agreed to update production mechanical drawing

PTCv3B

PTCv4

Next steps

- Continue debugging I2C, GbE
- Power up WIB
- Timing tests
- Assemble second PTC for BNL tests
- EtherCAT
- We have 2 assembly quotes for the production order
  - Zentech (have used before)
  - Advanced Assembly
- Component lead times are long
  - ICs continually go in and out of stock – will test functionality of critical ICs
  - Enclustra FPGA availability is getting better
- Needs for 2023:
  - 4+1 prototypes for VD Module 0, ICEBERG, BNL
  - Will need 4+1 boards for ProtoDUNE-II-HD or NP04 (schedule unclear)
- Full detector will have:
  - 150+10 PTCs for HD, and 80+10 PTCs for the VD



Pick-and-place setup

Summary

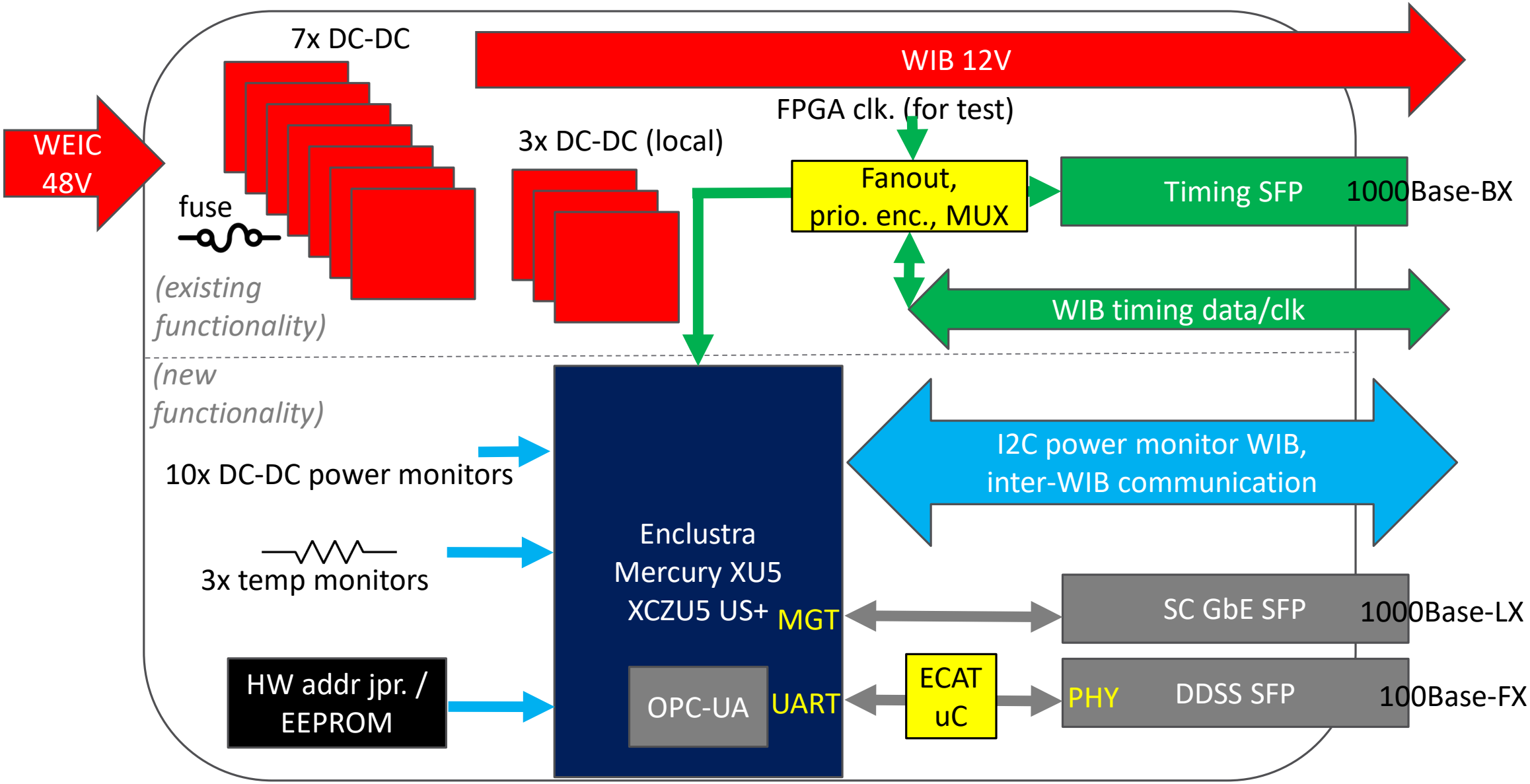
- ✓ PTC has been re-designed to provide:
  - ✓ Monitoring of local voltages and temperatures
  - ✓ Slow Control (SC) interface
  - ✓ DUNE Detector Safety System (DDSS) interface
  - ✓ Individual WIB control and/or communications
- ✓ Project status:
  - ✓ PCBs back and assembled
  - ✓ All components in-house
  - ✓ Bringup and firmware testing underway
  - Simple EtherCAT demo software exists using Infineon development board
- Work to do in the next month
  - Power and timing tests
  - Assembly second PTC
- Future work
  - Lots of software work (SC, DDSS – biggest unknown)

Backup

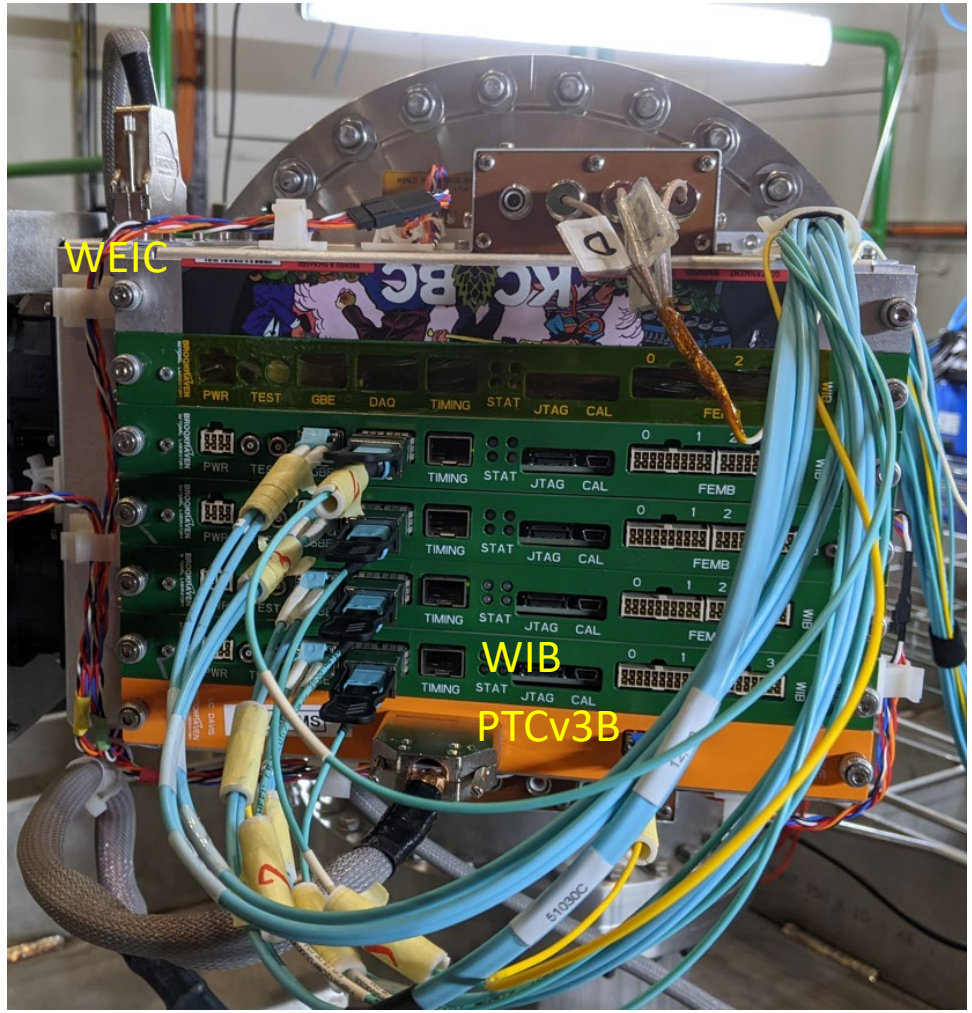
Additional documentation

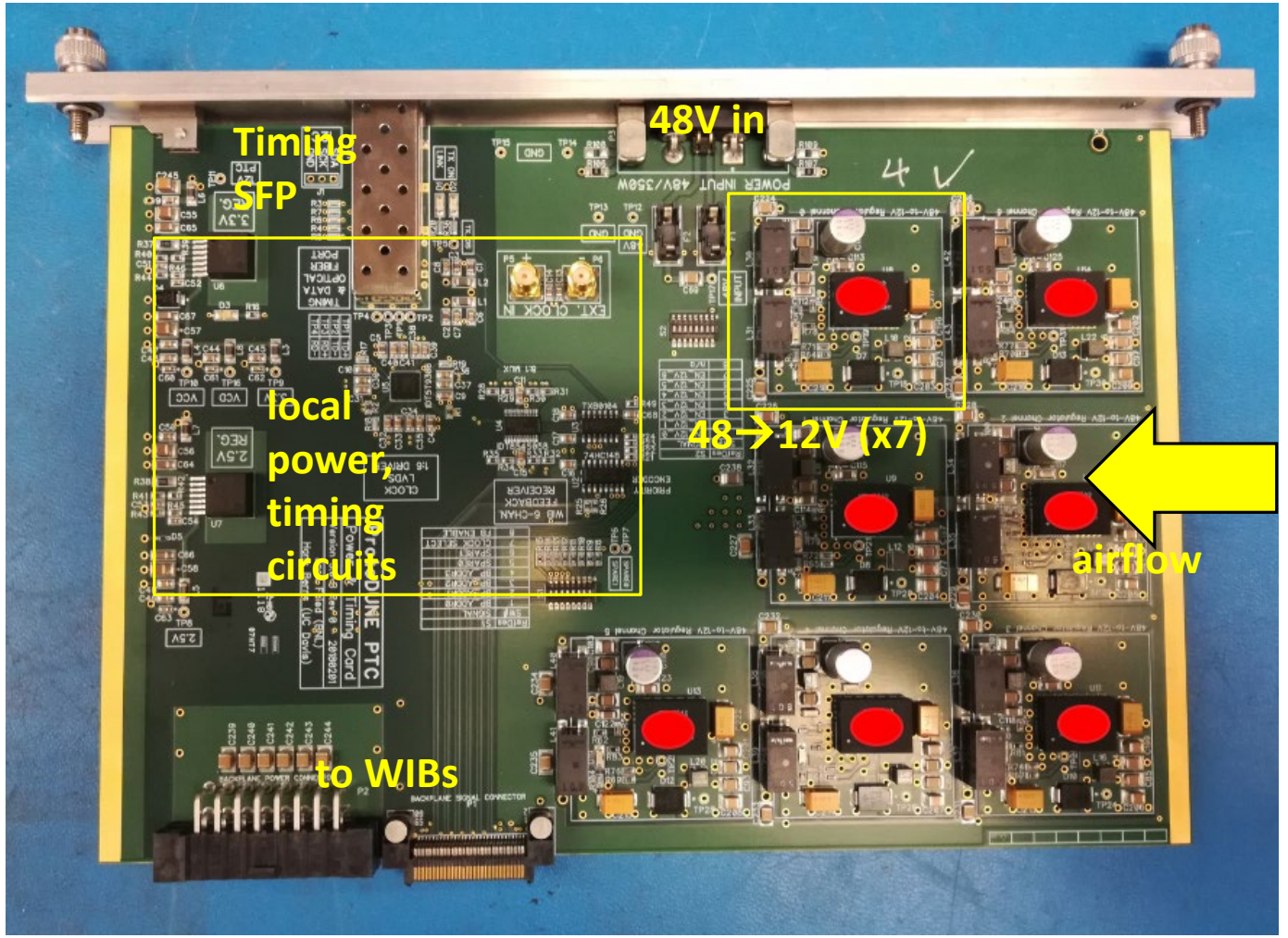
- Draft Requirements and Specifications here: https://edms.cern.ch/document/2731292/3
- DDSS specifications: https://edms.cern.ch/document/2401090/2
- Beckhoff PHY selection guide: https://download.beckhoff.com/download/document/io/ethercat-development-products/an_phy_selection_guidev2.7.pdf
- Previous DUNE Collaboration Meeting presentation:
  - (26 January 2023) https://indico.fnal.gov/event/53965/contributions/258363/attachments/163356/216220/PTC_status_20230126_v1e.pdf
- Previous Cold Electronics presentations:
  - (18 July 2022) https://indico.fnal.gov/event/55442/contributions/246656/attachments/157237/205657/PTC_v4_Design.pdf
  - (25 Oct 2022) https://indico.fnal.gov/event/56748/contributions/252918/attachments/160836/212036/PTC_status_20221025.pdf

Top level PTC v4 block diagram



Reminder: PCTv3B (current version)





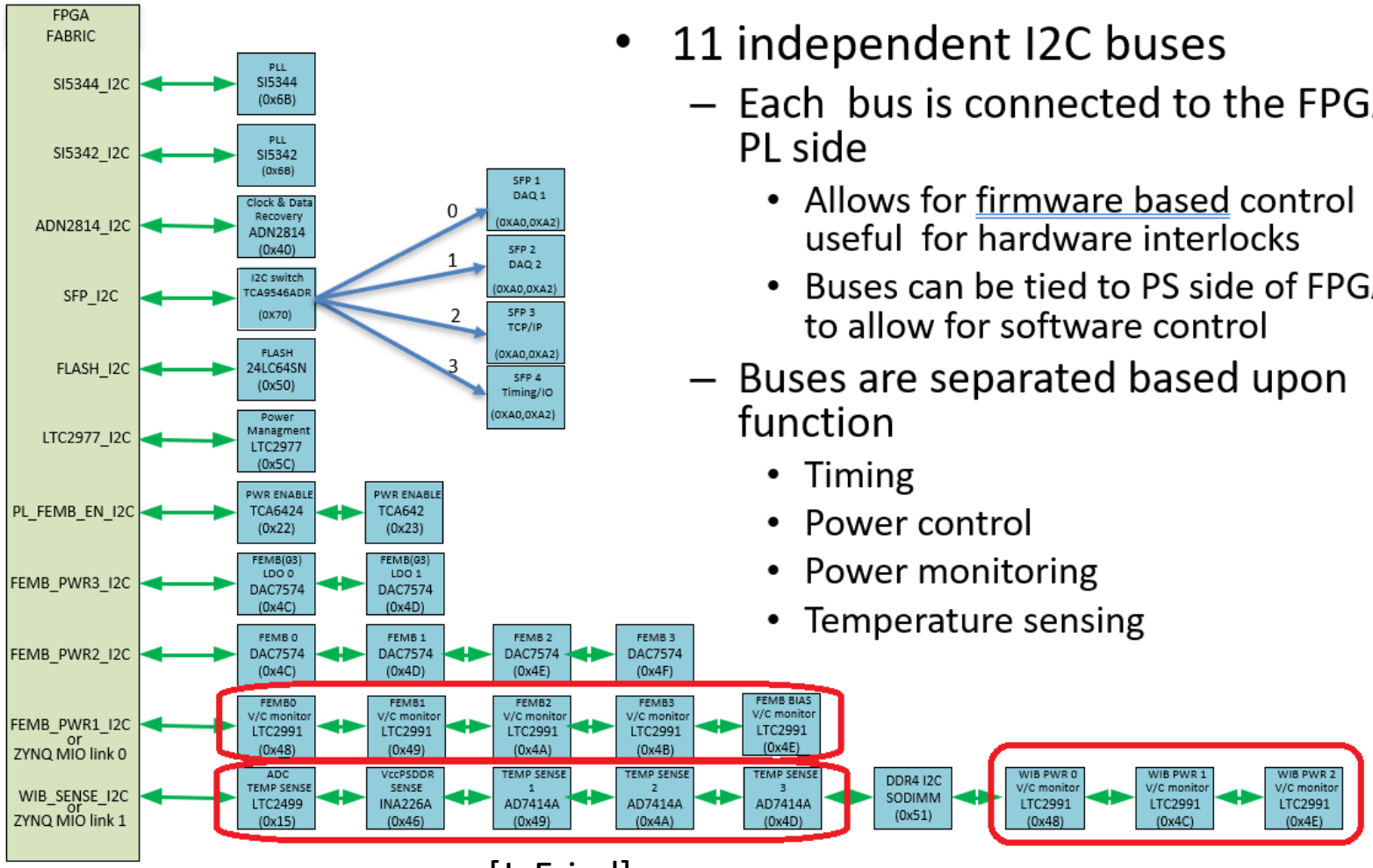
[J. Fried]

WIB monitored quantities

BROOKHAVEN NATIONAL LABORATORY

DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT

WIB I2C MAP



- 11 independent I2C buses
  - Each bus is connected to the FPGA PL side
    - Allows for firmware based control useful for hardware interlocks
    - Buses can be tied to PS side of FPGA to allow for software control
  - Buses are separated based upon function
    - Timing
    - Power control
    - Power monitoring
    - Temperature sensing

Architectural questions

- Powered-off WIBs
  - It was confirmed in conversation with Jack Fried at BNL that there is no way to permanently power off a WIB in a crate with PTCv4 without affecting functionality of all other WIBs in the crate
  - This is because WIBs have no IO buffering for the following signals: timing TX enables, crate addresses, spare IOs
  - This means a powered off WIB's FPGA can pull down a line
  - **There are two solutions, for prototypes ONLY:**
    - **Do not power off WIB for the first prototypes; only power cycle if needed, or remove from crate**
    - **Re-spin the PTB (power and timing backplane) to include buffers powered by local WIB and PTC 2.5V**
  - For the long term, the WIB will be re-spun with additional buffers added
- IO bandwidth
  - I2C will limit local BW
  - ~90 quantities that can be monitored, so maybe ~100sps rate for I2C bus @ 400kHz
  - EtherCAT 100Mbps is also a hard limit total BW
  - Really only need 1-2Hz for a lot of these power and temp measurements – much more reasonable
- Is PTC an independent OPC/UA endpoint, or the OPC/UA endpoint for all WIBs in a crate, or not an OPC/UA endpoint at all?
  - PTC can do any / all options
  - But final decision drives final hardware design (i.e. less powerful SoC needed if not an OPC/UA endpoint)