Overview

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FD1 TPC Electronics (Cold ASICS+FPGA) PRR

8-9 May 2023

Thank you for taking time to serve on the ASIC+FPGA PRR Committee

Your assessments and recommendations are important to us

The goal of this Review:

1. Obtain approval from the Committee to proceed with the fabrication of ColdADC/COLDATA ASICs for FD1

2. Affirmation for the procurement of Xilinx FPGAs for the Warm Interface Board (WIB) for FD1

   (Note: given long lead time of 64 weeks quoted from the vendor, DUNE management granted approval to submit the FPGA PO with a written justification document, see Hucheng's talk)

Presentations for this Review

https://indico.fnal.gov/event/59429/timetable/

Talks are selected to address charge questions. Additional backup materials in the list of documents provide

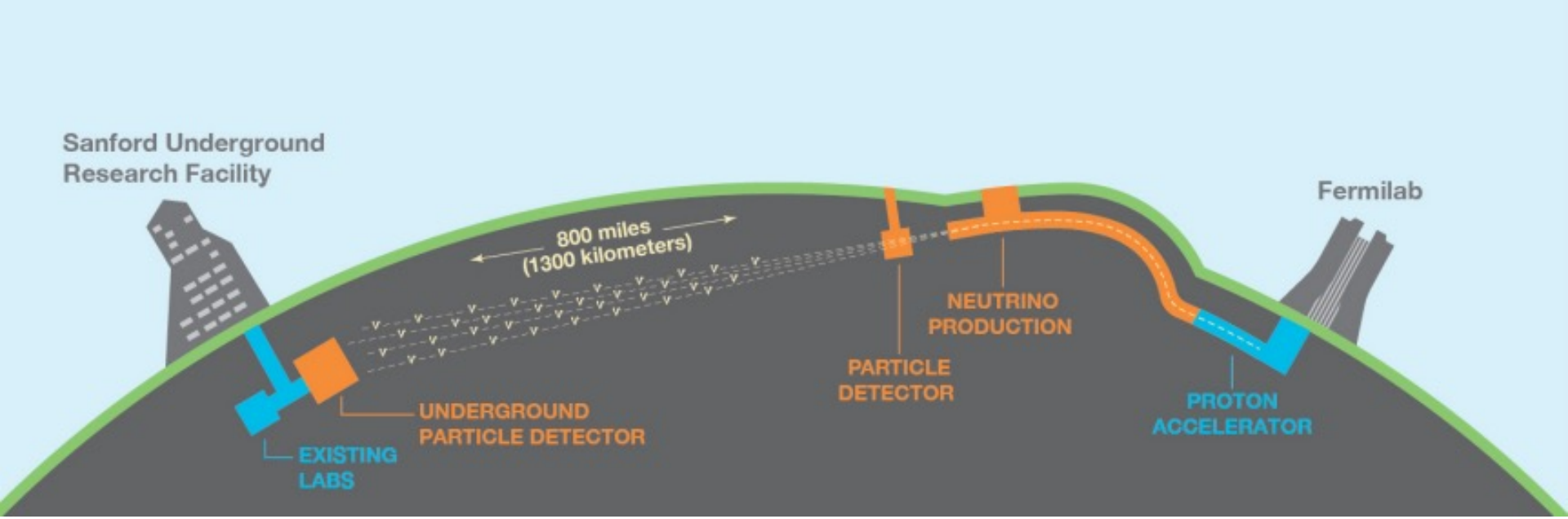
1. Overview [charge # 1, 5, 6]
2. ColdADC and COLDATA [charge questions # 2, 5]
3. ASIC lifetime studies [charge question # 4]
4. Frontend Motherboard Testing [charge question # 3]
5. Warm Interface Board and FPGA [charge question # 10]
6. CERN Cold Box and ProtoDUNE-II [charge question # 3]
7. ASIC QC Teststand [charge question # 7, 8]
8. Production Plan (cost and schedule) [charge question # 9]

Documentation for this Review

Link to the documentation guide spreadsheet is provided on the Review homepage: https://indico.fnal.gov/event/59429/

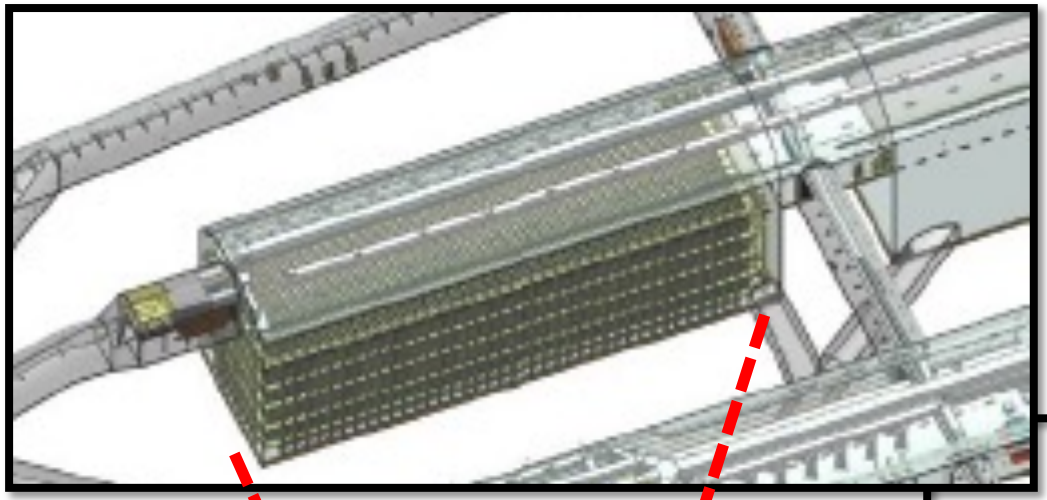
Category	Document	EDMS	File Name	Description	Charge Questions
Design Documents	FD1 TDR Chapter	2606684	DUNE-FD-TDR-vol-IV-SP-for-arxiv.pdf-vol-IV-SP-for-arxiv.pdf	DUNE Technical Design Report, Volume 4: DUNE FD SP Technology (copy or arXiv:2002:03010, also published in JINST 15 (2020) 08, T08010	
		2606690	TPC electronics Chapter from DUNE-SP Tecnical Design (includes post TDR updates)	Chapter 4: TPC Electronics only (updated on September 2022)	2, 3, 5, 7
	ASIC Documentation	2314429	COLDADC_P2_Datasheet_docx_cpdf.pdf	Datasheet for version P2 (production) version of ColdADC	
		2314430	COLDATA_P3_Datasheet_docx_cpdf.pdf	Datasheet for version P4 (production) version of COLDATA	
		2588343	IMEC reticle	IMEC reticle for the engineering and proposed production run. Reticle contains both ColdADC and COLDATA	
	Warm Interface Board Documentation	2712914	WIB schematics, board layout, and BOM	WIB Design files including BOM	
		2341138	WIB_firmware_docx_cpdf.pdf	WIB firmware document	
		2892599	WIBandPTC_Firmware_and_Software_development_docx_cpdf.pdf	WIB and PTC Firmware development plan	
		2892641	WIB-FPGA.CD-3A.pdf	WIB FPGA Resource Estimate.	
Requirements Documents	Summary of requirements on ASICs	2397298	ASIC_Requirements_v3_docx_cpdf.pdf	Summary list of the requirements affecting the DUNE ASICs	2
	Warm Interface Board Requirements	2341138	WIB_v3_requirements_v3_docx_cpdf.pdf	WIB reqirements document	2
	EB-Held Requirements	2346091	Far_Detector_EB_held_specifications_15June2021.xlsx	Complete list of all the top level specifications for the first DUNE far detector module (approved by the DUNE executive board)	2, 3, 5, 7
	TB-Held Requirements	2384645	Far_Detector-TB-held-specifications-12JUN2020-update28sep2020.xlsx	Complete list of all the specifications for the first DUNE far detector module that required for integration and installation purposes (require approval by the DUNE technical board)	2
	Consortium-held Requirements	2397298	Far_Detector_SP_consortium_specifications_08Sep2022.xlsx	Spreadsheet with all the requirements / specifications, including those determined by the individual consortia	2
Production and QC plans	Quality Control Plan	2815079	FD1_Time_Projection_Chamber_TPC-Electronics_and_FD2_Bottom_Drift_Electronics_BDE_Quality_Control_Plan-04May2023_docx_cpdf.pdf	Document describing the quality control plan for the entire cold electronics system. QC disscussion relevant to the ColdADC and COLDATA are in Section 4.1 of this document. For the WIB QC, the discussion is in Section 4.7.	5
	ESD Procedure	2782612	LBNF_DUNE_Prevention_and_Control_of_Electrostatic_Discharge_(ESD)_Ver_0.pdf	LBNF DUNE Prevention and Control of Electrostatic Discharge	7
		2782612	ESD_CE_docx_cpdf.pdf	ESD procedure specific for the TPC electronics. ASICs procedure is discussed in Section 5.	7
	Production Plan and Resources	2604783	2604783_ASIC_Production_QC_v4_docx_cpdf.pdf	Production plan covering LArASIC, ColdADC, and COLDATA	5, 9
		2781366	TPCelectronics_PBS.xlsx	Parts Breakdown Structure. ColdADC and COLDATA are in lines 11 to 14. For the WIB, the FPGAs are not tracked. The WIB is on line 125.	
		2821837	FD1-DUNE-Multi_Institutional_MOU-ANNEXES_01_25_2023_docx_cpdf.pdf	FD1 Institutional MOU. TPC Electronics MOU is in Annex 7.	5
Previous Reviews	Answers to the recommendations from past reviews	2604159	FD1_HD_TPC_Electronics_ASIC_FDR_Recommendation_tracking_May_5_2023.xlsx	Response to the recommendations from the ASICs FDR of July 2021. The recommendations are for all three ASICs and FEMBs. All recommendations have been closed except one. The one "for future" is pending the conclusiong of the COLDATA lifetime study expected to complete by summer of 2023.	1
		2889782	FD1_TPC_Electronics_FDR_Recommendation_tracking_May_5_2023.xlsx	Recommendations relevant to the ASICs and the WIB are completed	1
Review Presentations		DUNE-Indico-59429	Overview Presentation		1, 5, 6
			ColdADC and COLDATA		2, 5
			ASIC Lifetime Studies		4
			Frontend Motherboard Testing		3
			Warm Interface Board and FPGA		10
			CERN Cold box and ProtoDUNE-II		3
			ASIC QC Teststand		7, 8
			Production Plan (Cost and Schedule)		9

Deep Underground Neutrino Experiment (DUNE)



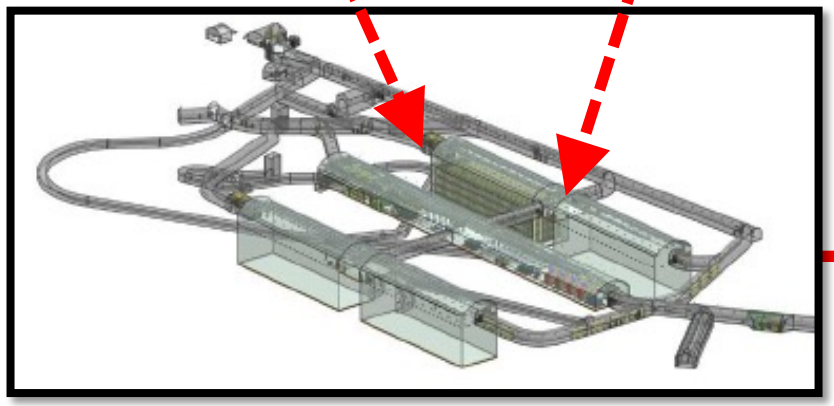
- Future flagship neutrino oscillation experiment
- Three major components: neutrino beamline, near detector, and liquid Argon far detector modules
- Broad physics program: BSM studies supernovae, solar neutrinos, three-flavor oscillation measurements
- >1300 people, > 200 institutions, 33 countries + CERN

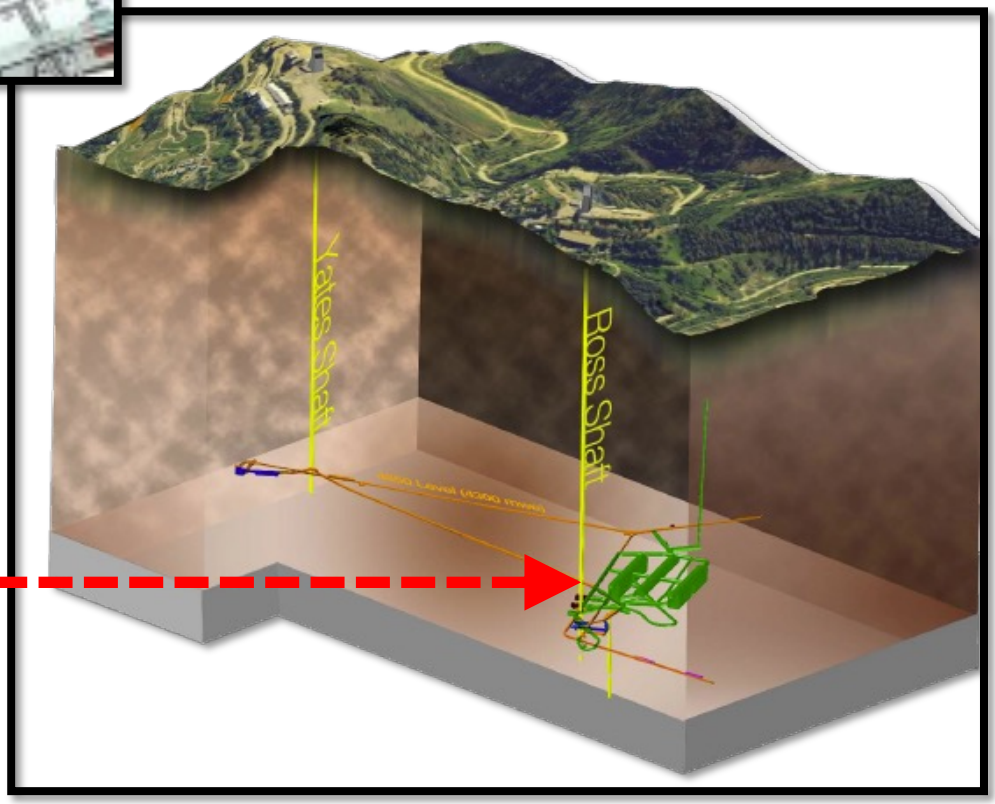
DUNE Far Detectors



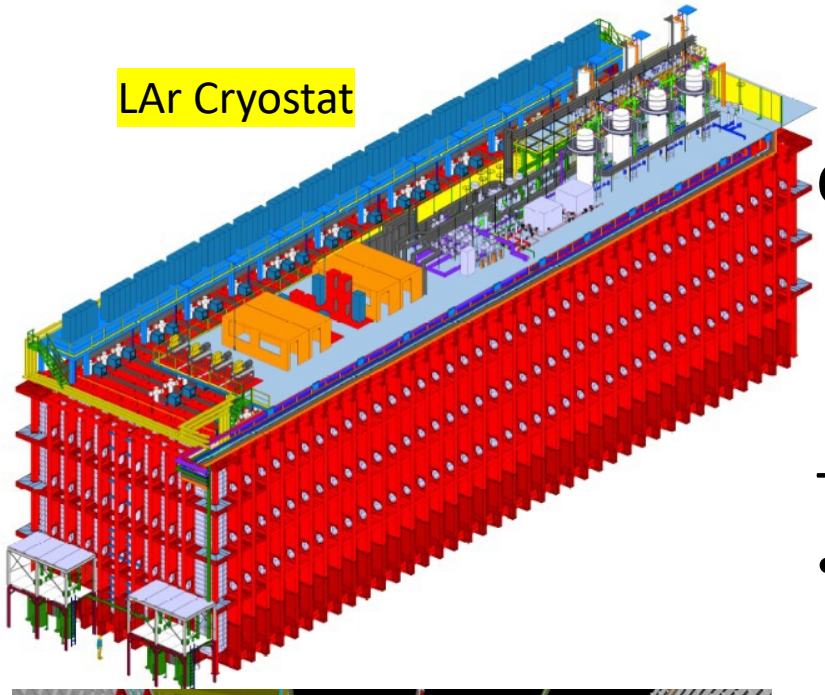
Four 10-kTon (fiducial) liquid argon detectors

~1500m underground



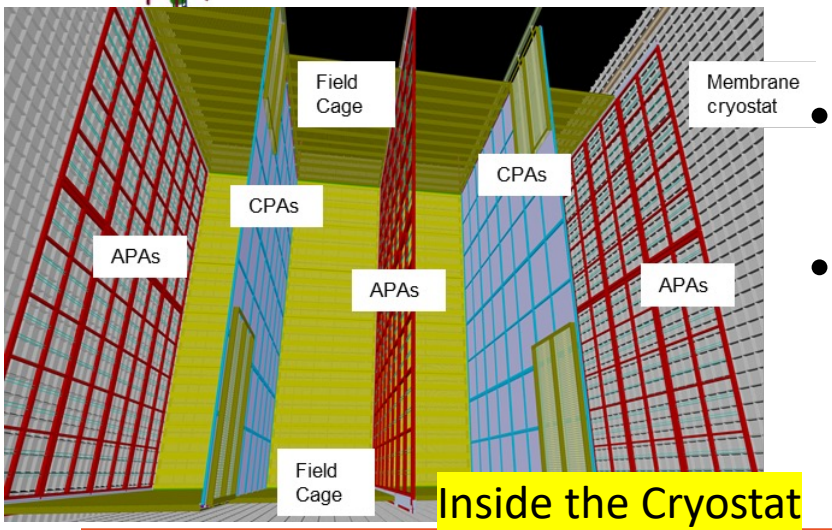


DUNE Far Detector #1



Cryostat dimensions:

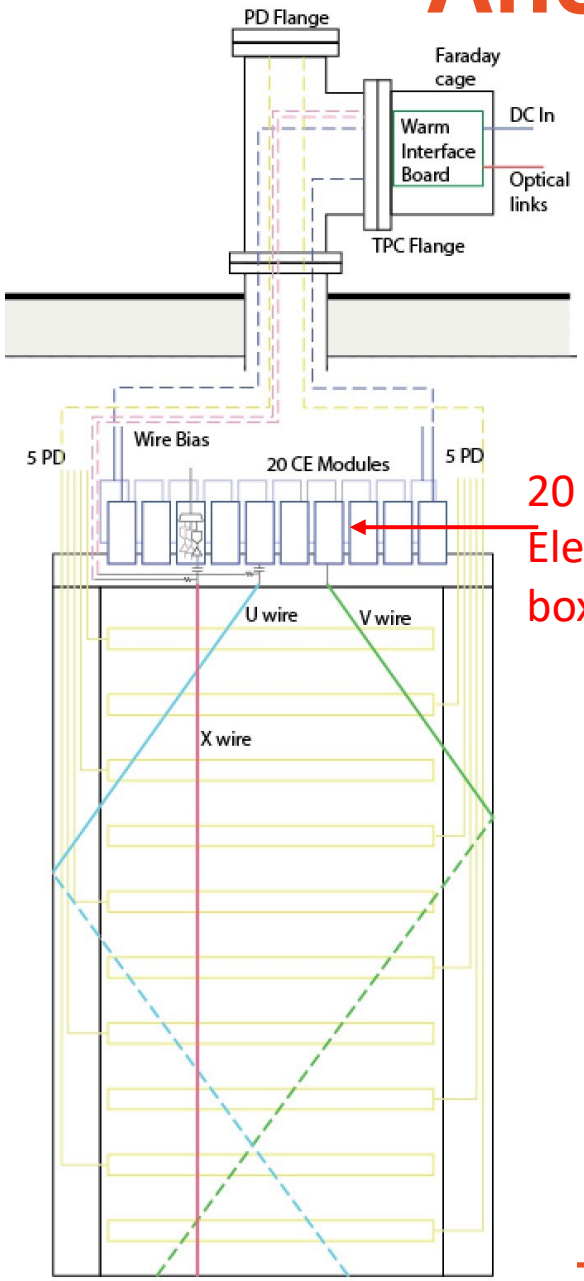
~65m (L) x 19m (W) x 18m (H)



Time Projection Chamber (TPC) Elements:

- Anode Plane Assembly (APA). Sense wires for detecting drift electrons in the TPC
- Cathode Plane Assembly (CPA) at -180kV. Electron drift field of 500V/cm
- Distance between CPA and APA plane = 3.6m (maximum electron drift distance)

Anode Plane Assembly (APA)

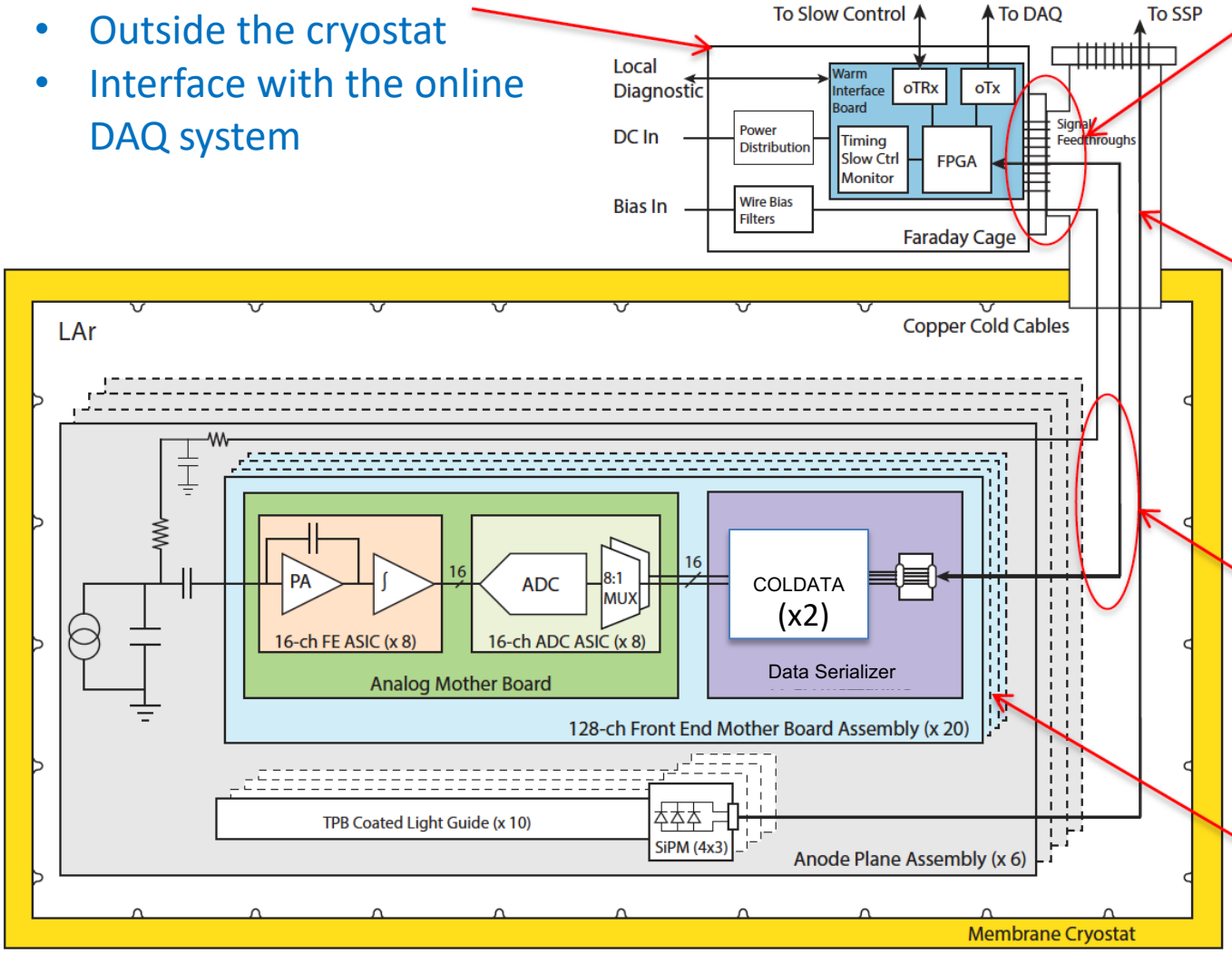


- Far detector #1 has 150 APAs
- Each APA has four wire planes:
  - 960 grid wires (un-instrumented)
  - 800 U (1st induction wires)
  - 800 V (2nd induction wires)
  - 960 X (collection wires)
- Readout electronics are integrated close to the sense wires on the APA and immersed in LAr to yield the best SNR → Cold Electronics
- 20 Cold Electronic (CE) Boxes are mounted on the top of each APA and connected to 2560 sense wires

TPC Readout Electronics

Warm interface electronics:

- Outside the cryostat
- Interface with the online DAQ system



CE Flange:

- On top of the cryostat
- Connect cold cables to the Warm Interface Electronics

Signal feedthrough:

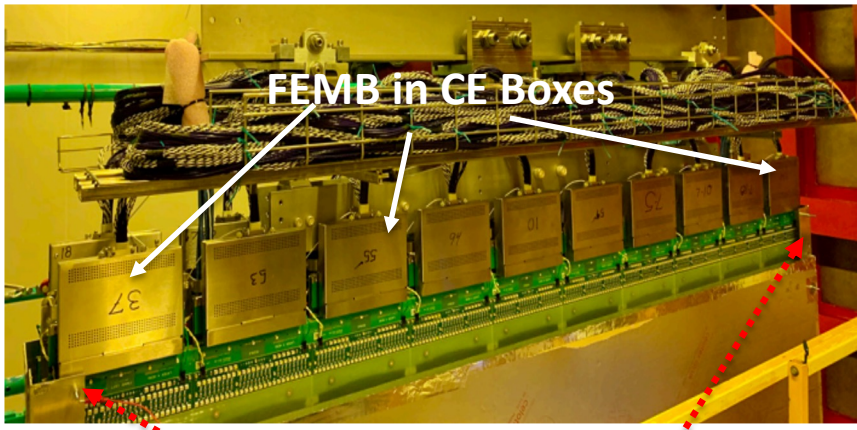
- 14” conflat
- Cable strain relief

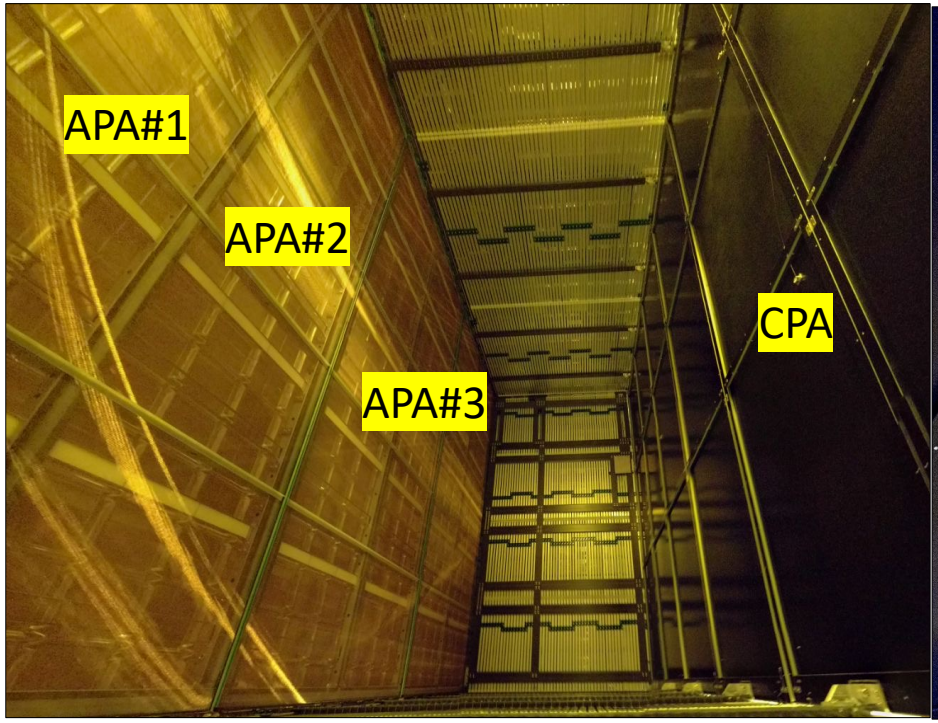
Cold cables: Low voltage and data cable to Frontend motherboard

Frontend Motherboard (FEMB): 128 channels of digitized wire readout enclosed in CE box

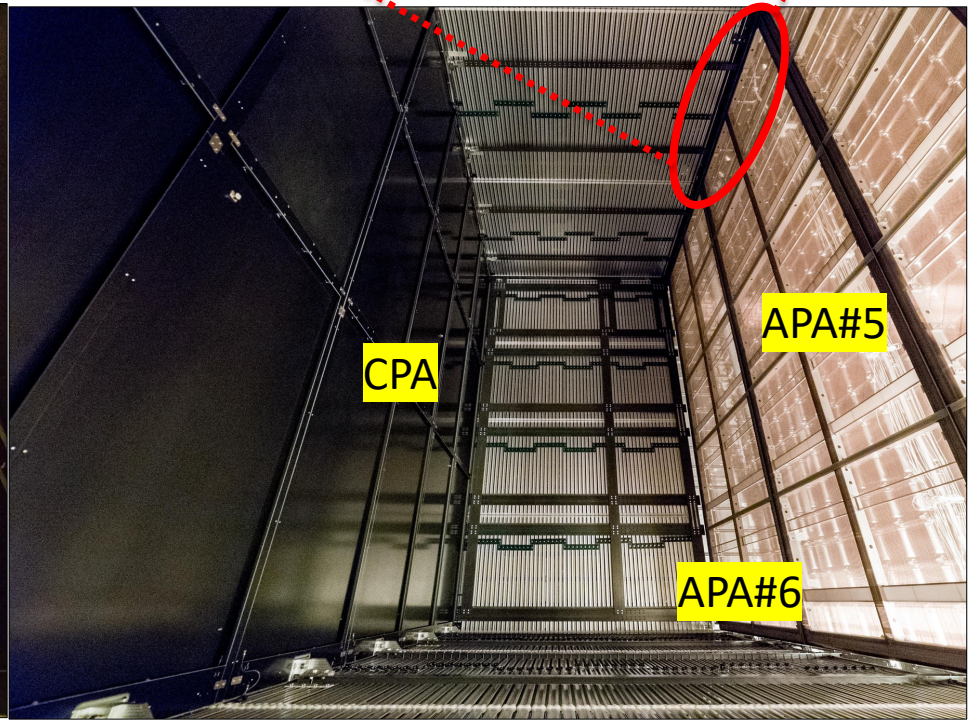
ProtoDUNE-1 operated in LAr for ~ 2 years (Sept 2018 to July 2020)

No degradation in CE performace





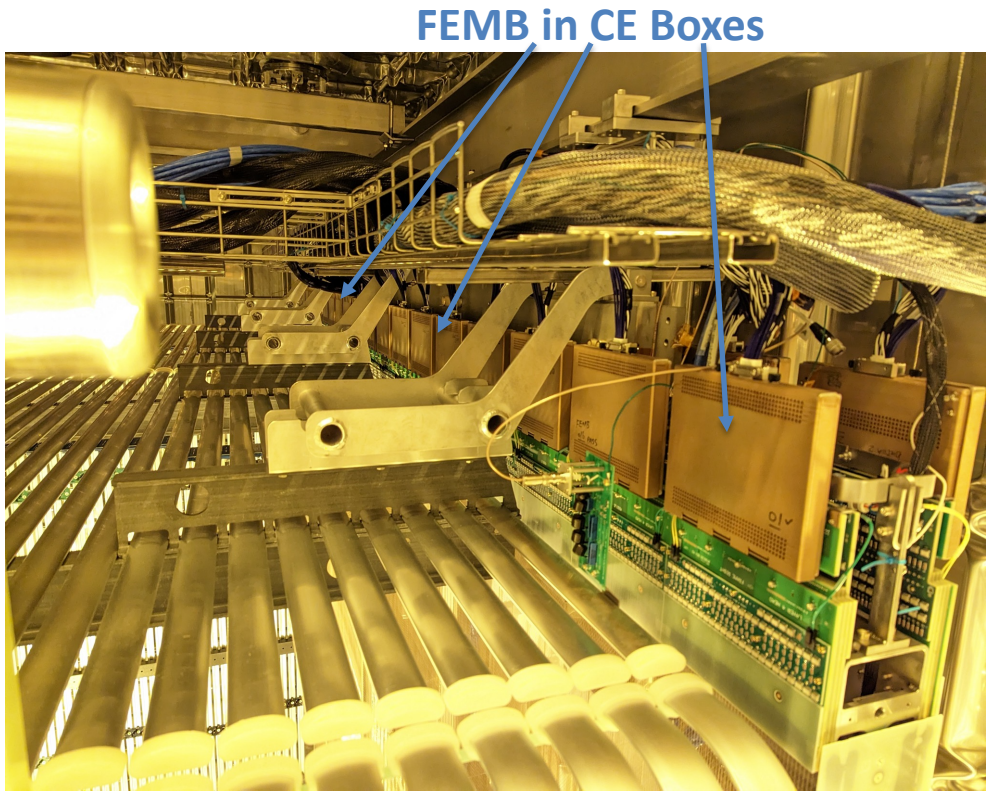
Beam-Right TPC Volume

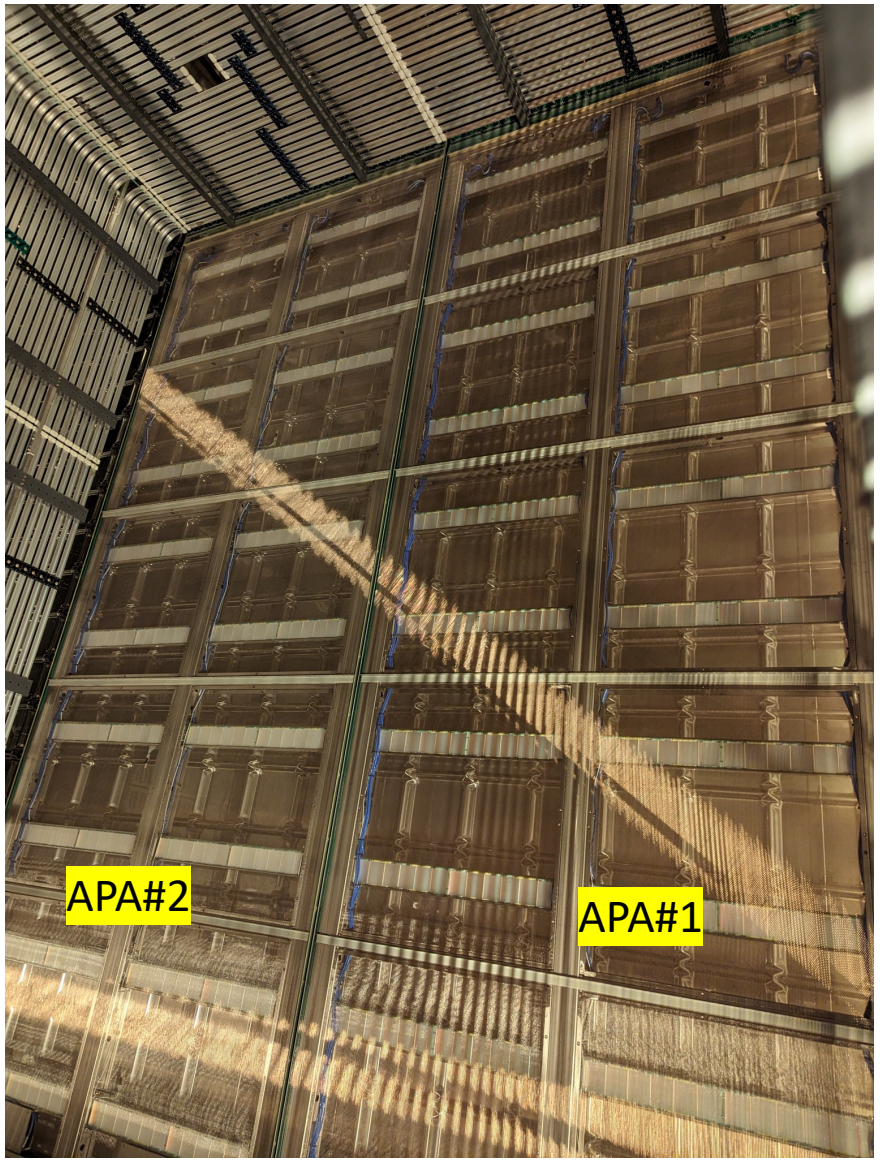


Beam-LEFT TPC Volume

ProtoDUNE-2 installation completed

80 FEMBs (final design) installed on four APAs





Past Review Recommendations

FD1 HD TPC Electronics ASIC FDR:

- Complete list of recommendations and status in EDMS#2604159
- All recommendations are closed except one
- We are leaving the lifetime study recommendation open ("for future") until the conclusion of the COLDATA lifetime this summer

FD1 HD TPC Electronics FDR:

- Complete list of recommendations and status in EDMS#2889782
- All recommendations relevant to the ASICs and FPGA are closed

Charge Questions #6

Has a decision about the need or not for testing all the ASICs at cold before assembly on the FEMBs been taken?

Our baseline plan is to LN2 test all ASICs before assembly on the FEMBs. ASICs from the engineering runs have good yield on the order of 98%. Without cold tests, about 35% of FEMBs will need to be re-worked

We need to test a sufficient number of ASICs from the production run to verify the yield to decide what fraction of the ASICs need to be cold tested

Performed a cost analysis assuming 99% yield on all three ASICs. Produce 20% more FEMBs to cover the problem FEMBs without the need to perform re-work → roughly break even in cost.
For yield < 99%, not cost effective

Thank You !