# ColdADC and COLDATA

David Christian

May 8, 2023

# Outline

- Choice of 65nm CMOS
- ColdADC
  - Requirements
  - Design
  - Performance
- COLDATA
  - Requirements
  - Design
  - Performance
- QC testing for ColdADC and COLDATA
- Preliminary yield measurements

# Choice of 65nm CMOS

- In 2014, the FNAL & SMU ASIC groups performed a study of TSMC 65nm & 130nm (standard oxide thickness) transistors to determine their suitability for cryogenic use.
- Results were published in IEEE Trans Nucl Sci Vol 62, No. 3 (June 2015):
  - Both technologies were less sensitive to the hot carrier effect than larger feature size CMOS technologies.
  - 65nm transistors were significantly less sensitive to the hot carrier effect than 130nm transistors were.
  - Minimum length 65nm transistors had a predicted lifetime of more than 20 years even if operated at 1.3V rather than the nominal 1.2V.
- As a result, 65nm CMOS was chosen for COLDATA and ColdADC.
  - Logix Consulting was paid to make cryogenic measurements of a variety of 65nm transistors and extract SPICE models.
  - To be extra safe, the decision was taken not to use minimum length transistors in the design.
  - A set of custom standard cells was developed (initially at Penn), characterized using the SPICE models, and used for digital design.

# ColdADC Requirements & Specifications

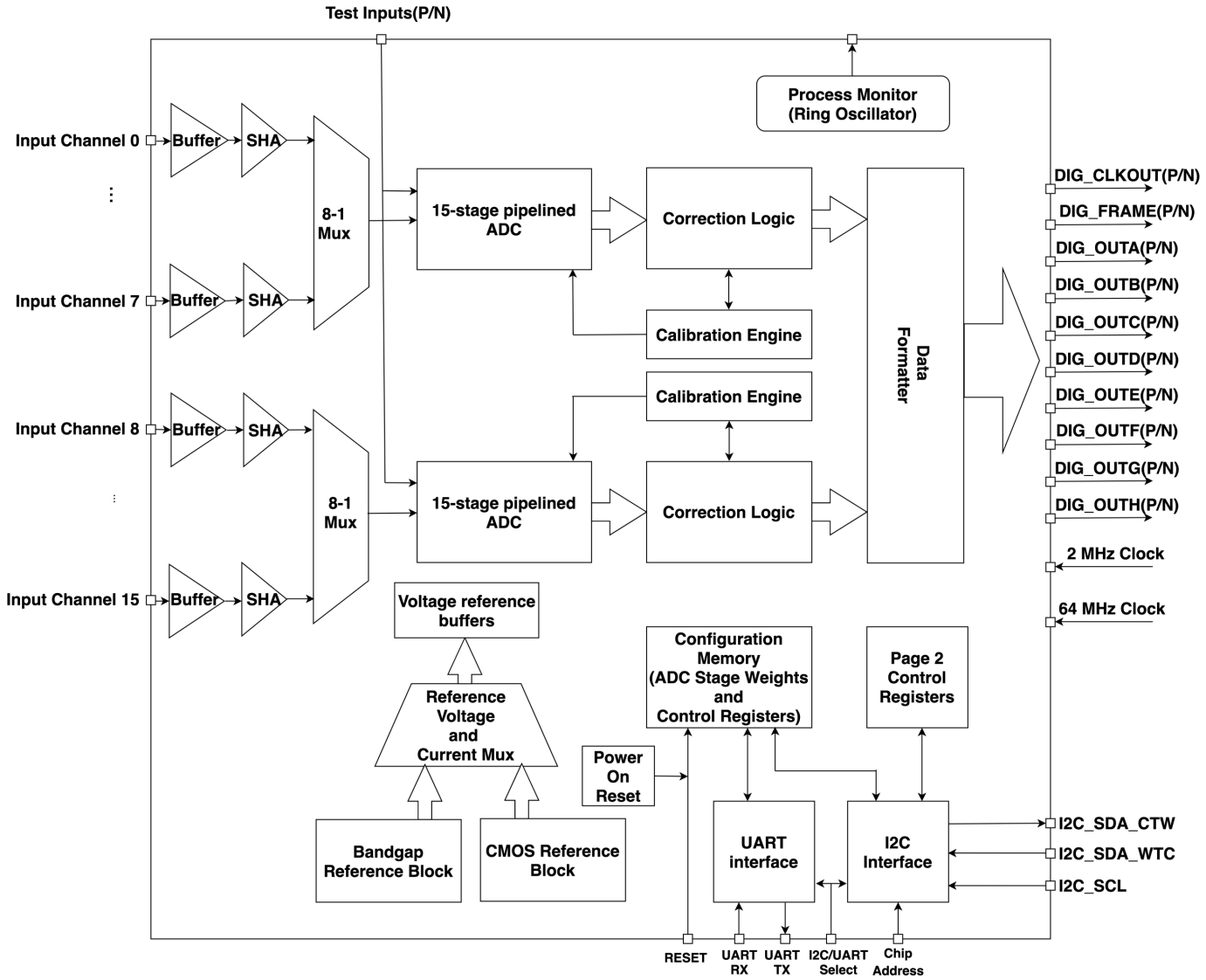
- Requirements:
- Sampling frequency ~2 MHz
- Number of ADC bits: ≥ 12
- Total power (of all ASICs): < 50 mW/channel
- Noise contribution ≪ 1000 e- (negligible compared to LArASIC)

- Specifications:
- Crosstalk: < 1%
- Differential Nonlinearity (DNL): Absolute value < 1
- Integral Nonlinearity (INL): < 1(12-bit ADC unit)
- Equivalent Number of Bits (ENOB) > 10.3
- Overflow protection: When input signal exceeds the upper or lower ADC range, the output should be fixed at the maximum or minimum value.

# ColdADC Design

- LBL, FNAL, BNL collaboration led by Carl Grace (LBL)
- Designed to digitize signals from 1 LArASIC:
  - 16 channels; linear output range of ~1.6V
- Analog blocks are implemented using thick oxide (2.5V) devices
- Digital logic is mostly implemented using thin oxide (1.2V) devices.
- Uses two 15-stage pipelined ADCs operating at ~16 MHz (1.5 bit/stage)
  - Digital calibration logic corrects for non-ideal stage gain and offsets
  - Calibration procedure is automatic (occurs on command)
  - Reference voltages and currents are produced on-chip

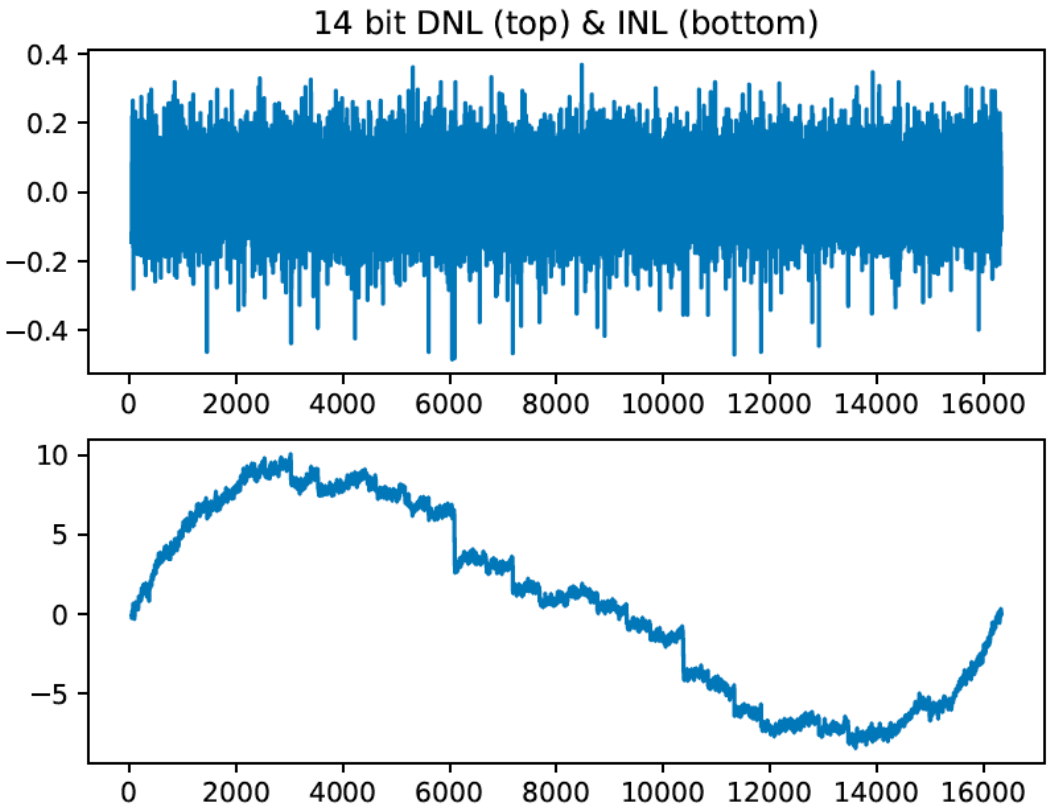
# ColdADC Block Diagram



# ColdADC Performance

- Power consumption is within budget (< 21 mW/channel)
- Noise is very low & uniform channel to channel & chip to chip:
  - Differential inputs: ~.75 (14-bit) ADC counts
  - Single ended inputs ~1.5 ADC counts
- Differential nonlinearity (DNL) is good
  - No missing 14-bit codes
- INL is larger than expected.

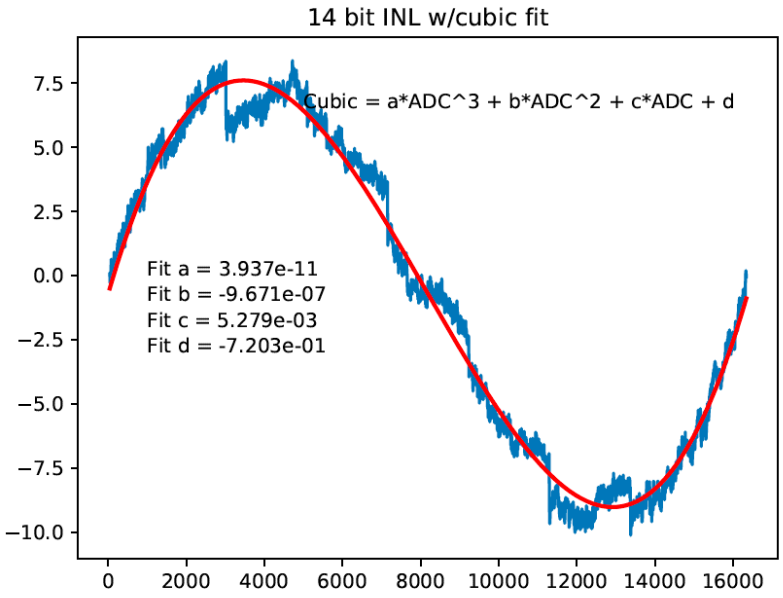
Typical DNL and INL (14-bit)



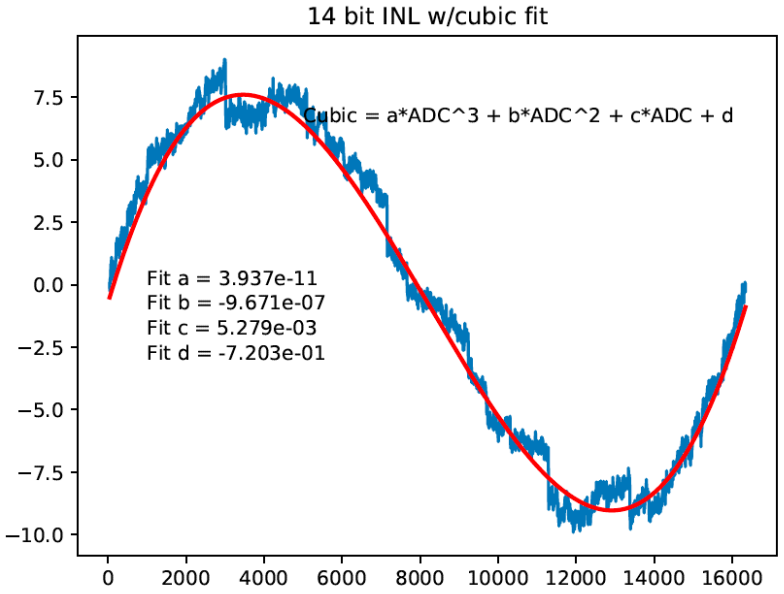
# ColdADC Integral Nonlinearity

- INL is larger than expected (especially for channels 0 and 8).
- INL (defined as the integral of DNL) is well fit by a polynomial of odd order and can be improved offline.
- Increasing bias currents in ADC stages does not reduce the nonlinearity--> not an MDAC settling problem
- Linearity can be dramatically improved by decreasing the ADC clock rate → not a capacitor nonlinearity problem
- Decreasing the settling time of the input buffer made no difference.
- We believe the nonlinearity is consistent with the presence of dielectric absorption in the capacitors.
  - Dielectric absorption is a phenomenon by which charged caps only partially discharge after being charged for a long time.
  - Caps used are MIM structures (because they are reasonably small and accurate)… but MIM caps implemented with high-k dielectric are known to suffer from dielectric absorption.
- We decided to live with the problem rather than redesign the chip using a different capacitor type (MOM).

# ColdADC INL is stable in time

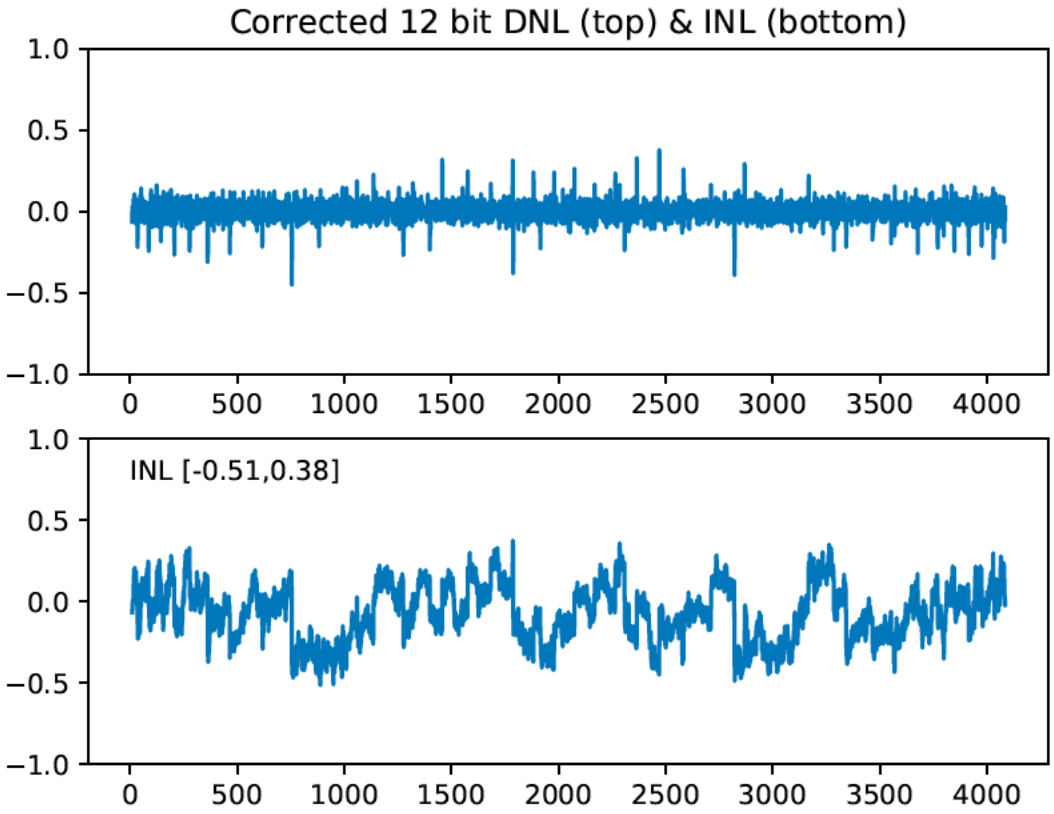



Fit to data taken on 10/27/20 together with a cubic fit to the data. Temp=77K



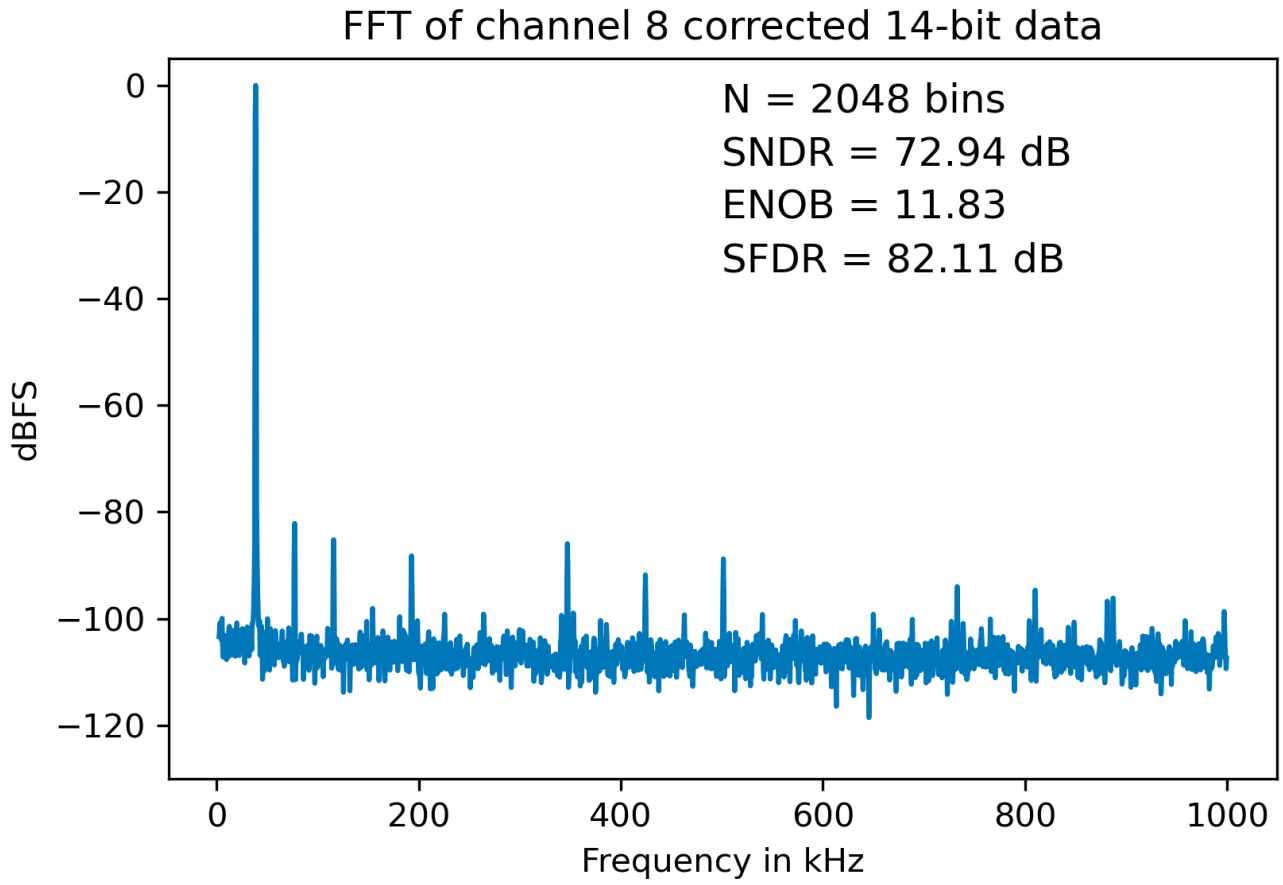

Data taken on 11/2/20 with the fit from the 10/27 data superimposed.

# INL is very good after offline correction



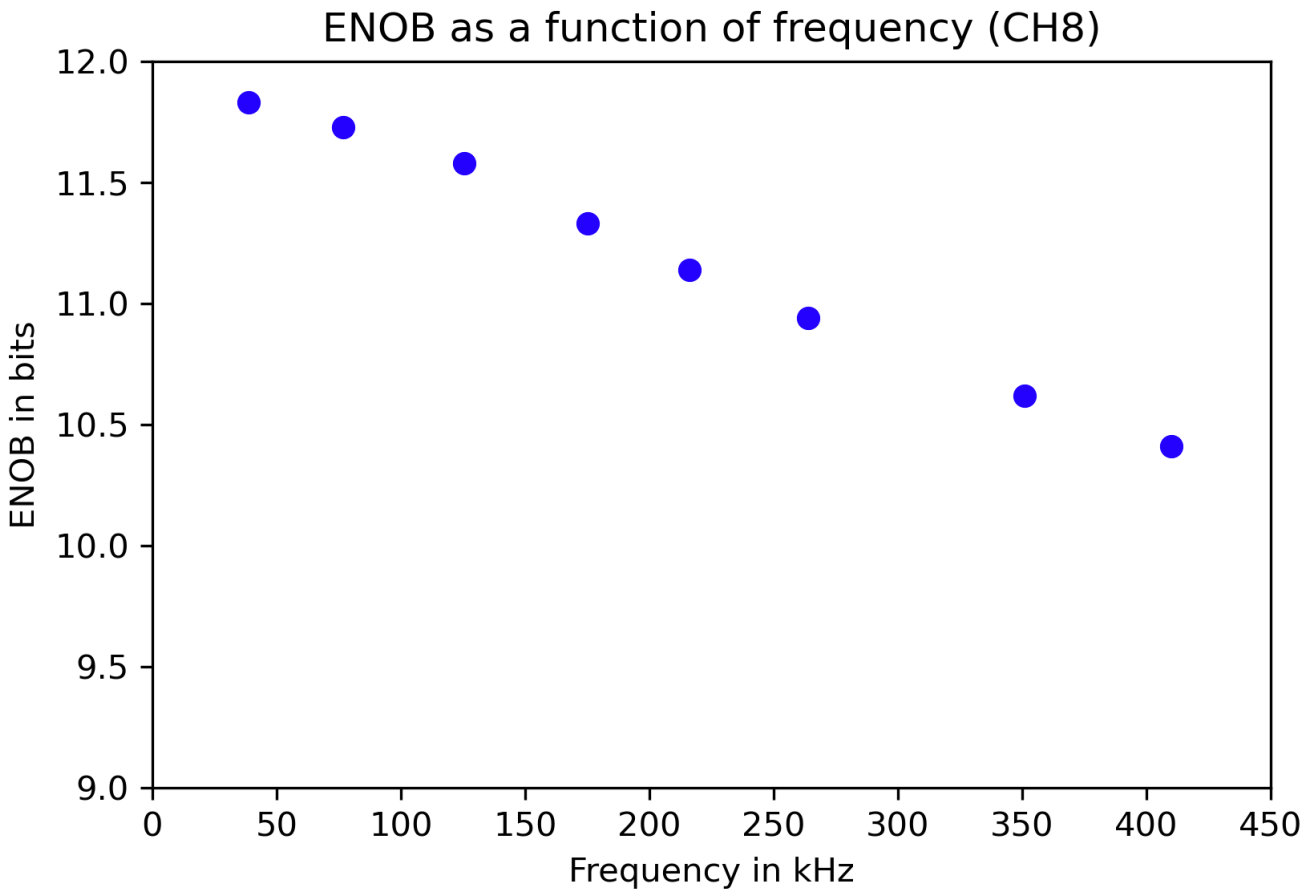

12-bit INL for data corrected using the cubic fit to the 14-bit data on the right hand side of the previous slide.

# Dynamic Linearity is also good after offline correction




Typical frequency spectrum of ADC output codes (with differential inputs at 77K) after offline polynomial correction. The input frequency was  38.6 kHz.

# ENOB as a function of frequency




LArASIC -3dB bandwidth is ~205 kHz with 1 us shaping time

# COLDATA Requirements & Specifications

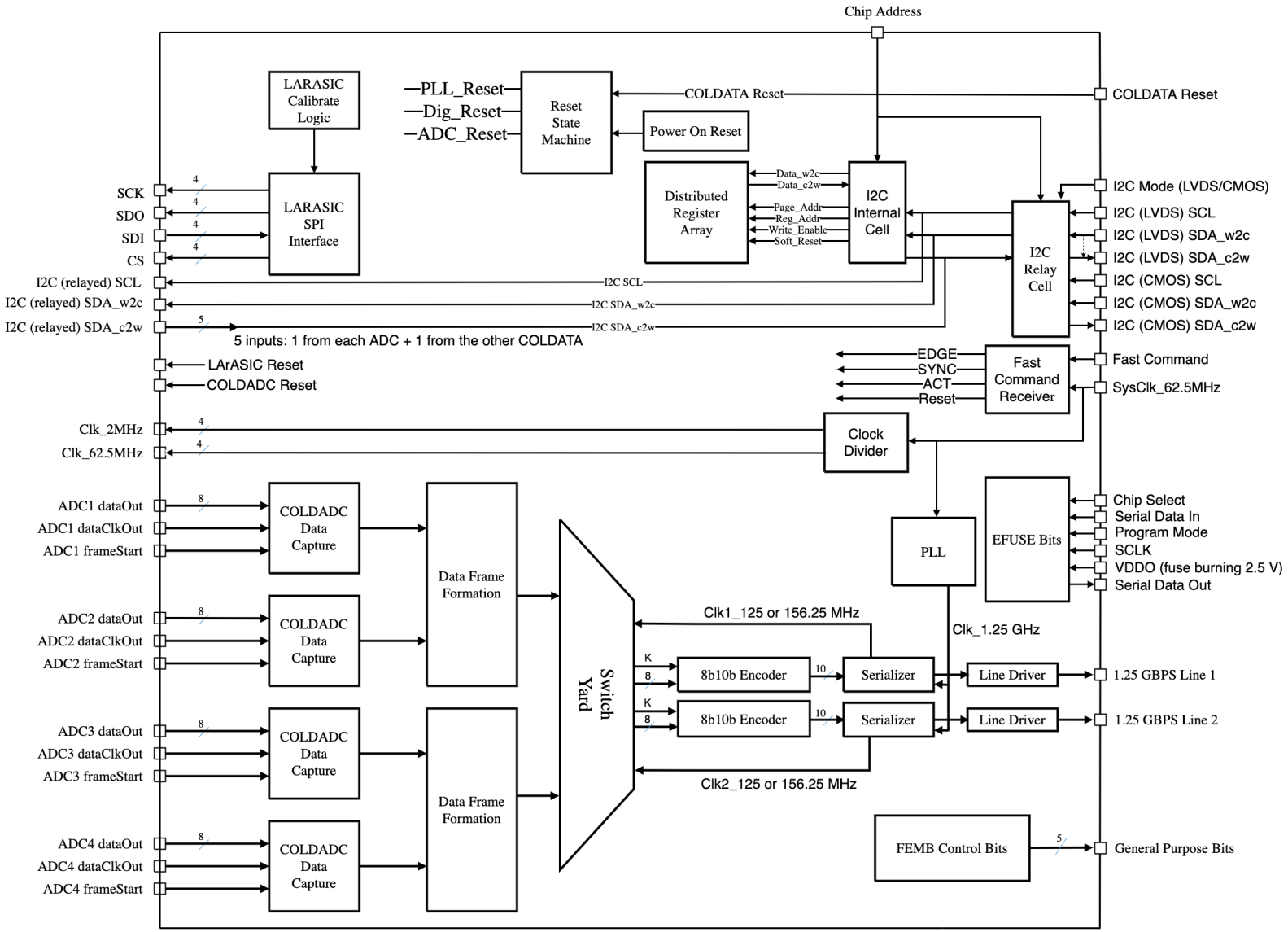
- Requirements:
- Total power (of all ASICs): < 50 mW/channel

- Specifications:
- Number of links between FEMB & WIB: 4 at 1.25 Gbps
- Clock jitter: < 180 ps [consistent with ADC ENOB of ~11 and signal bandwidth of 350 kHz]

# COLDATA Design

- FNAL, BNL, SMU collaboration led by Jim Hoff (FNAL)
- Only thin-oxide (1.2V) devices are used
- COLDATA controls 4 LArASICs and 4 ColdADCs
  - I2C-like control path for COLDATAs & ColdADCs
  - SPI control paths for LArASICs
- All clocks are derived from the 62.5 MHz system clock
- 1.25 Gbps hybrid-mode line driver (current-mode transmitter equalization and voltage-mode pre-emphasis) designed to drive long twinax cables (up to ~35m)

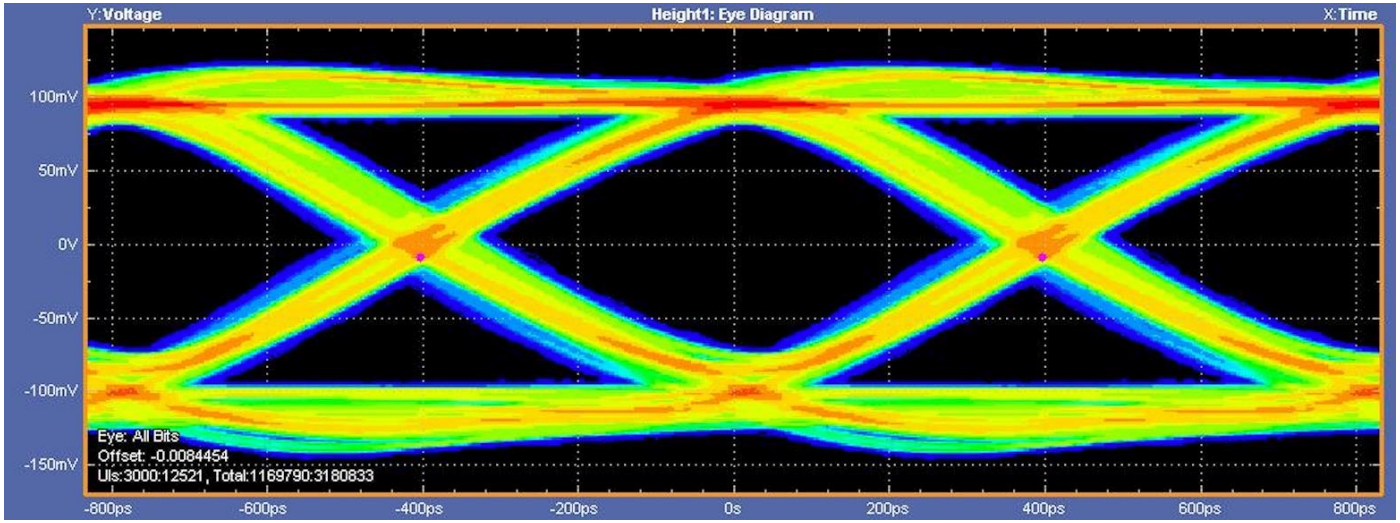
# COLDATA Block Diagram



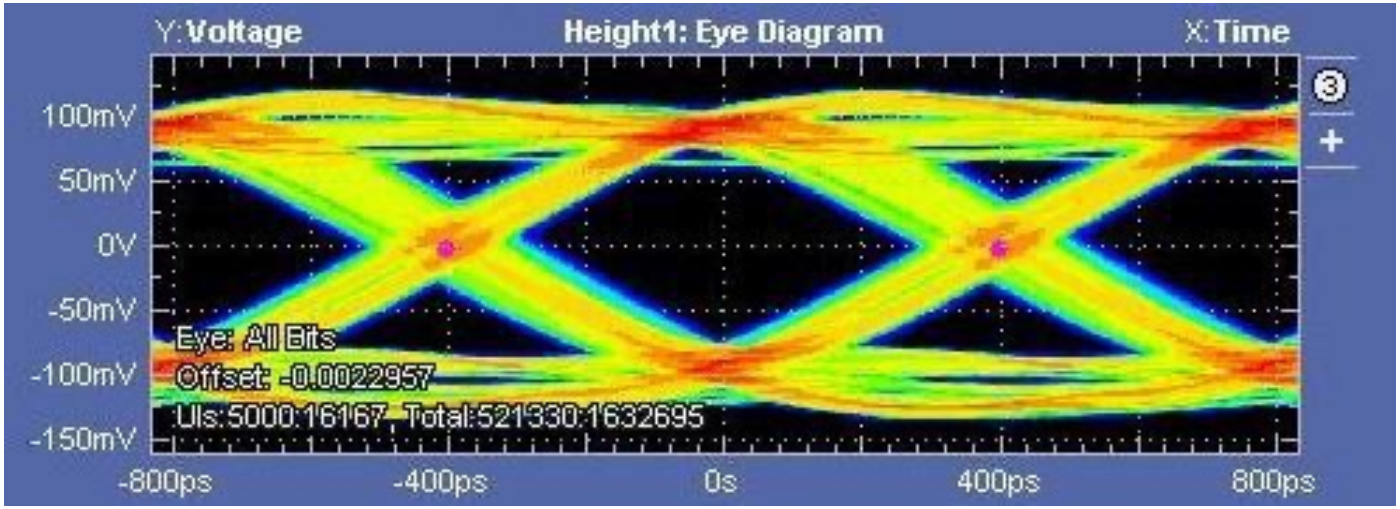
# COLDATA Performance

- All subcircuits operate as designed.
- Total power consumption ~170 mW (2.7 mW/channel)
- I2C Echo delay is ~4ns → cable delay can be accurately measured and compensated for (so all ADCs will sample simultaneously).
- PLL locking range is large and changes only slightly with change in temperature (RT – LN2).

# Line driver performance




~150 mV




~100 mV

PRBS7 eyes (RT): 25m Samtec twinax (top) & 35m (bottom)



Fermilab DUNE

# ColdADC QC

- Power cycle at least 5 times; measure currents
- Test I2C communication
  - Check power-on reset (verify default register values)
  - Write/read registers
- Measure reference voltages
- Perform auto calibration; check weights
- Measure open channel noise
- Measure DNL/INL (slow ramp or sine wave input)
- Check overflow protection
- Measure ENOB
- Repeat at LN2 temperature
- For a fraction of devices:
  - Measure ring oscillator frequency
  - Measure cross talk

# COLDATA QC (Not yet done; long lead time for sockets)

- Power cycle at least 5 times; measure currents
- Test I2C communication
  - Check power-on reset (verify default register values)
  - Write/read registers using both LVDS and CMOS paths
  - Verify I2C relay (read/write registers in ColdADCs)
  - Verify LArASIC SPI functionality
- Burn EFUSE bits (assign chip identifier)
- Measure PLL locking range
- Verify Fast Commands (check I2C echo, reset commands, & status regs)
- Verify output links using FRAME 14
- Check FEMB control bits
- Repeat at LN2 temperature

- For at least a fraction of devices:
  - Verify all output formats
  - Measure output link eye (for PRBS7) with long (warm) cable

# Yield

- Statistics from ColdADC QC done at 3 sites (LBL, UC Irvine, & LSU) indicate a yield of >98%
  - Most failures are obvious (power shorted to gnd, for example)
  - Some failures may have been due to test equipment problems.
  - Very few failures are observed at LN2 temperature for chips that operate properly at room temperature.
- COLDATA:
  - FEMB tests indicate COLDATA yield is also high (>97%)