ColdADC and ColdDATA Lifetime Studies

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DUNE PRR: FD1 TPC Electronics
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Content

To address Charge Questions # 4:
**Have life-time tests of all ASICs been done?**

- ColdADC lifetime study

- COLDATA lifetime study

- From FD2 BDE Preliminary Design Review: **A P5 LArASIC was stressed at 3.0V over 300 hours in liquid nitrogen, no significant change in current drawn is observed (BNL)**

Introduction to ColdADC

- ColdADC_P2 is a 16-channel, 12-bit, 2 MS/s digitizer

  - It's redesigned to correct several design errors, to improve performance and to add new features based on the first prototype of the ASIC (CodeADC_P1)

- It will be used inside the DUNE Far Detector, and intended for operation without replacement

  - Required to have low noise, good linearity and low crosstalk

 - Also required to have long-term reliability in cryogenic environments   ← Lifetime test

A bare die photograph
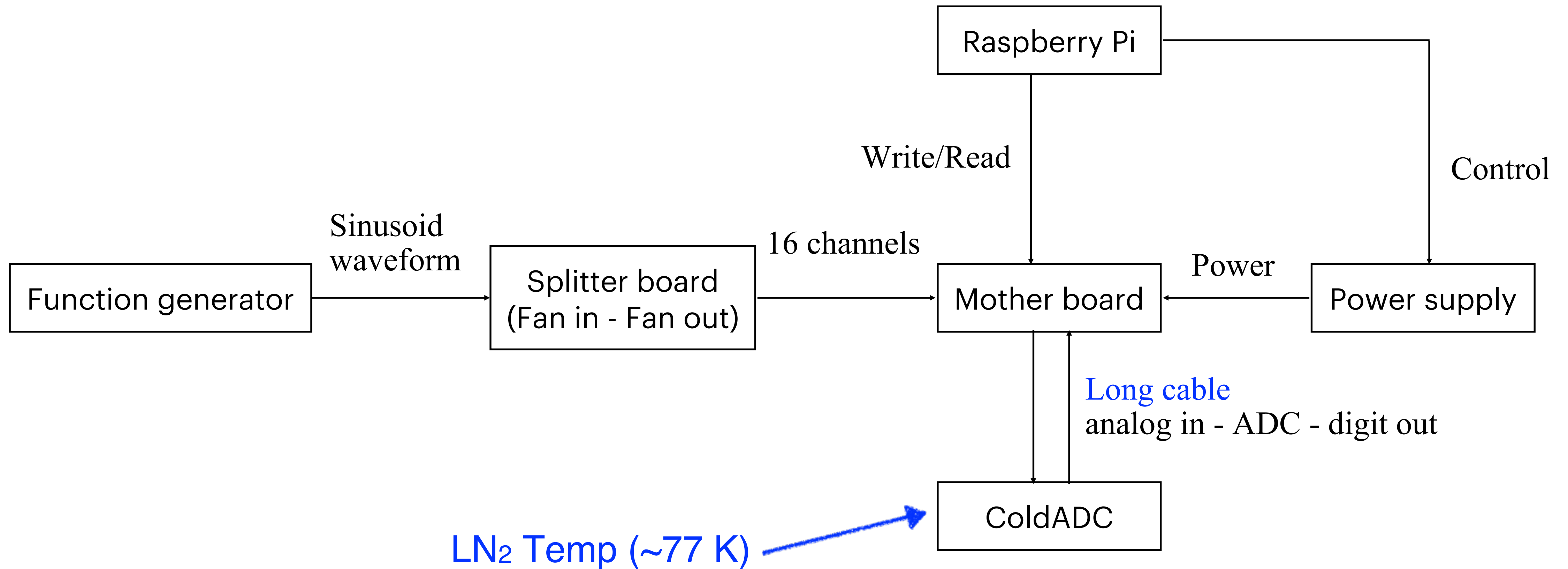

7.6 mm

6.9 mm

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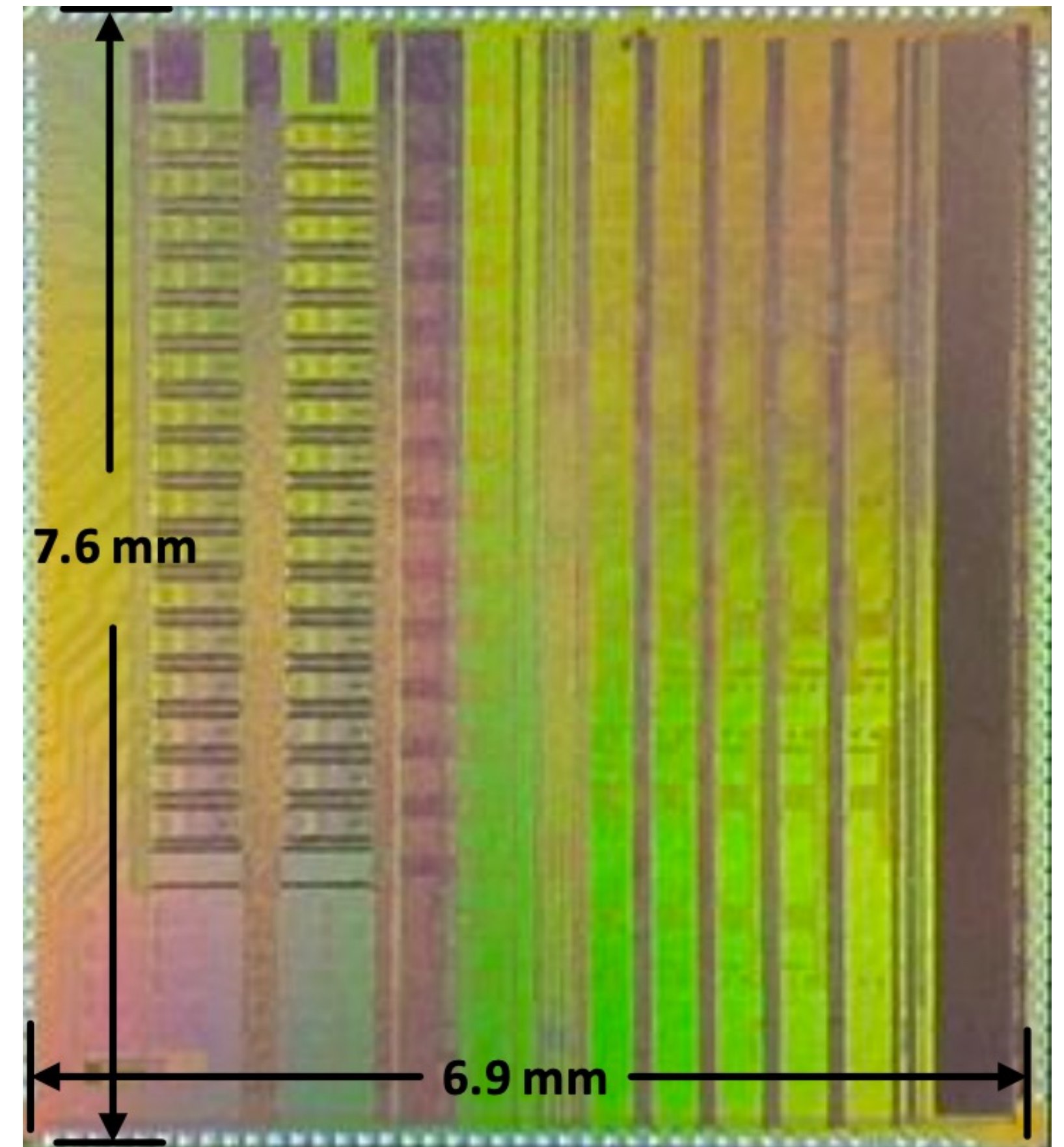
Preparation for the lifetime study

- Setup the ColdADC test stand

  - Power supply (Rohde&Schwarz NGE 100), SRS DS360 Ultra-Low Distortion Function Generator

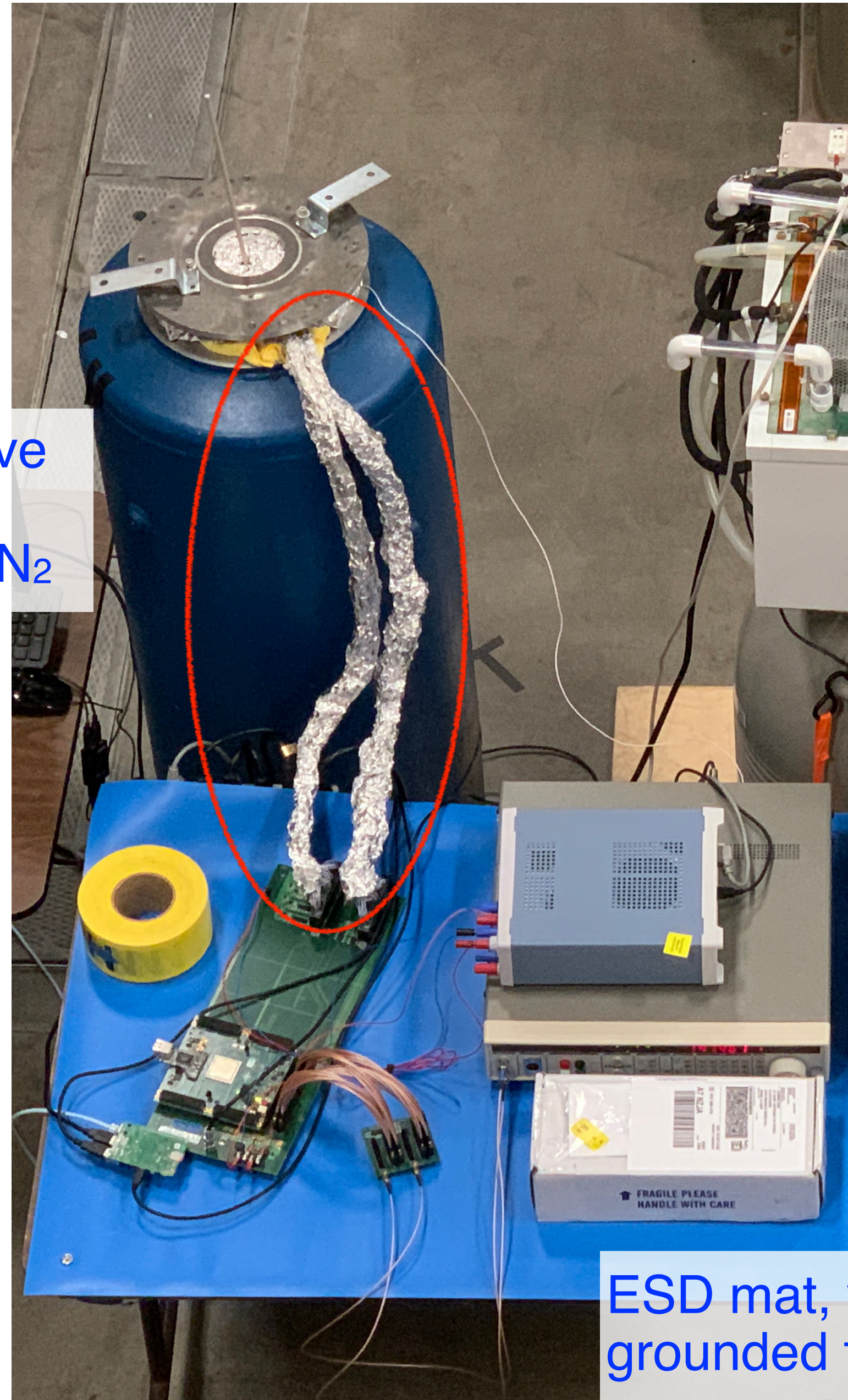 - With USB interface, the setup can be remotely operated

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Testing setup

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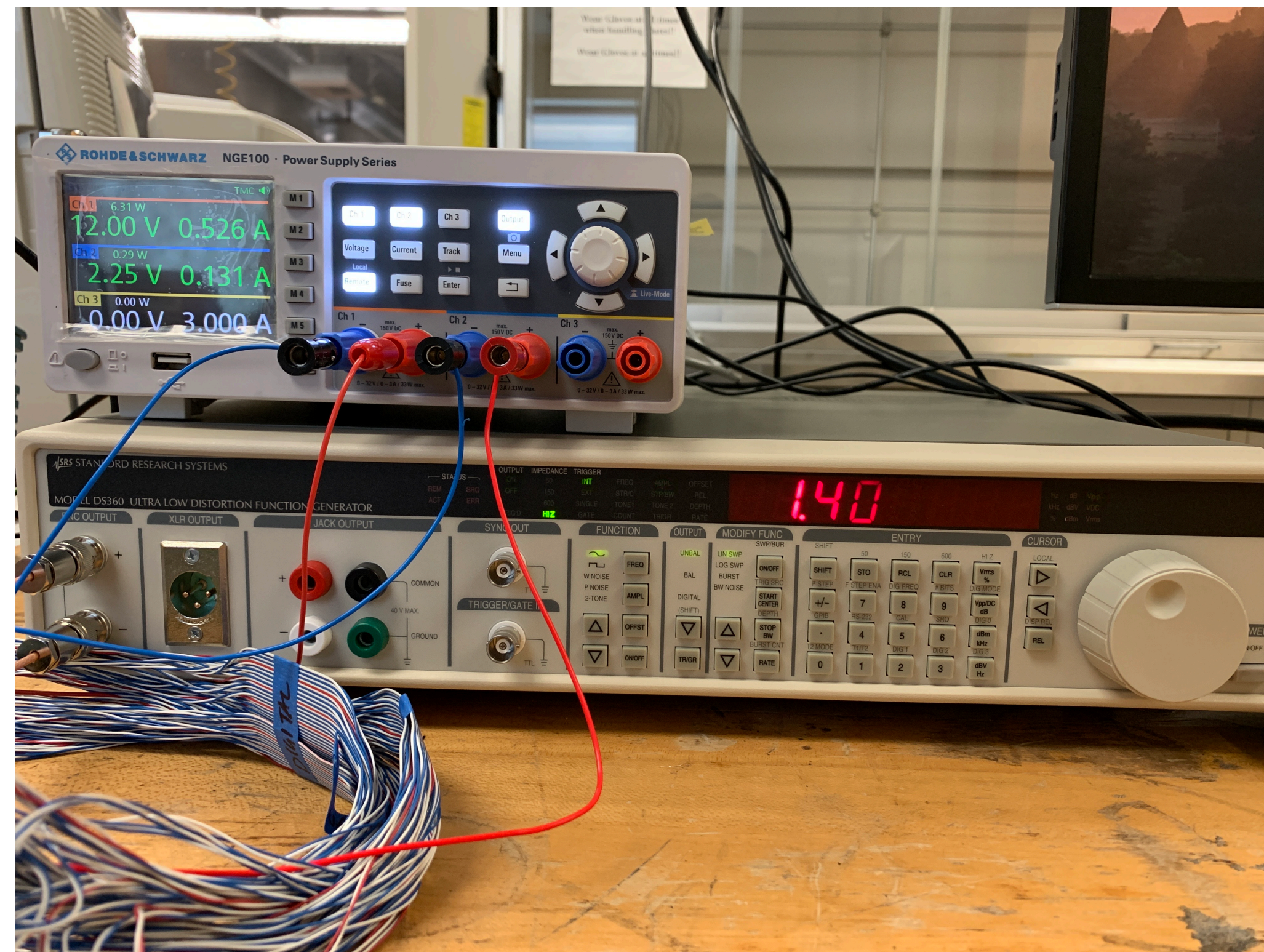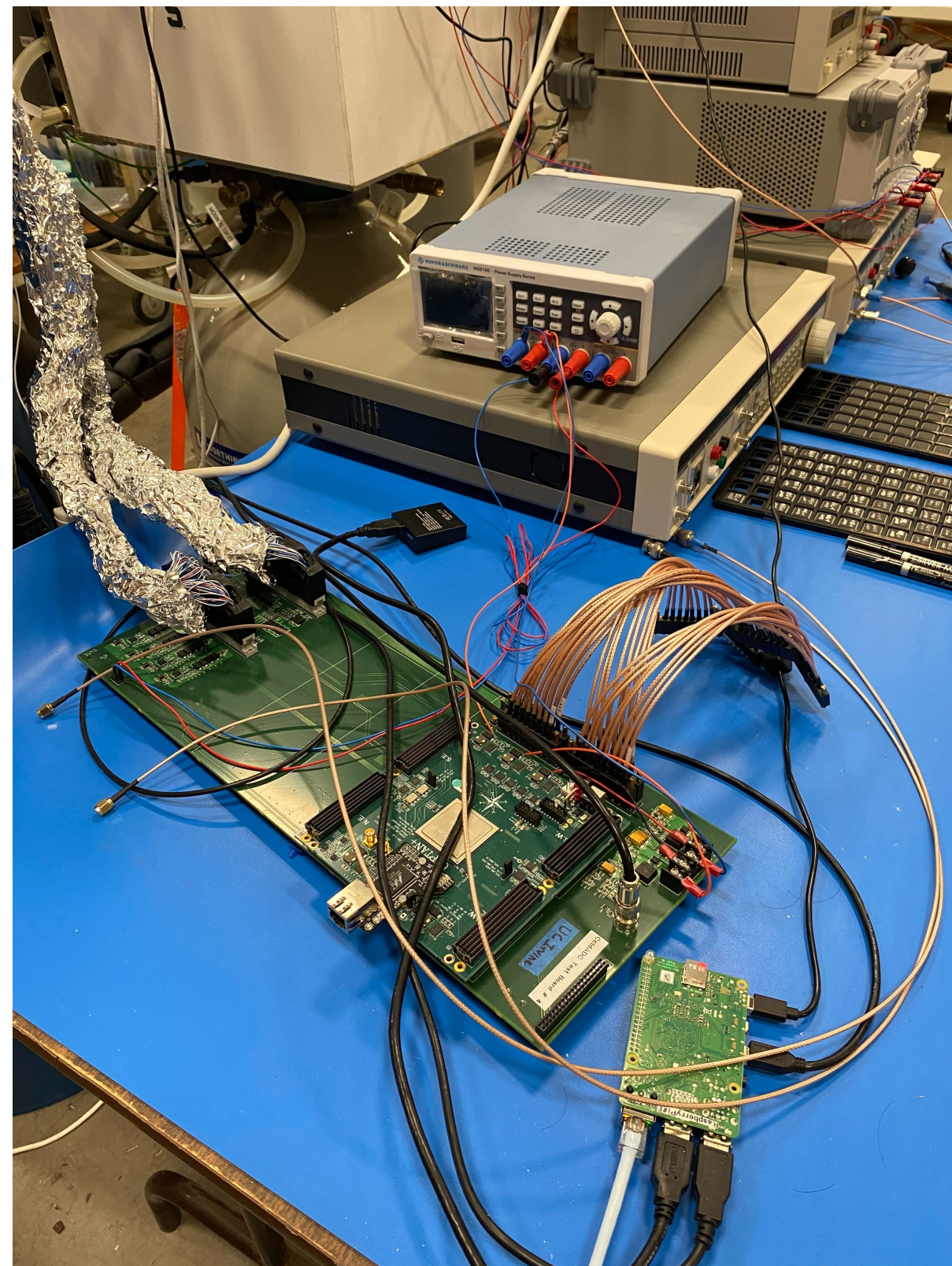
Test stand

Test stand at Irvine: we have the long cable in order to deploy the ColdADC into LN_2

ESD mat, w/ wrist strap, grounded to the electrical outlet

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Lifetime study: Methodology

- Accelerated lifetime measurement

  - ColdADC normally work at 2.25 V for long-term reliability. The lifetime at 2.25 V is at the level of decades.

  - In order to perform the lifetime study, we purposely increase the working voltage, such as 4.2 V and study the lifetime of ColdADC under the high voltage, then extrapolate the results to low voltage.

*Measurements of the Cold COTS ADC for SBND TPC Readout from H. Chen*
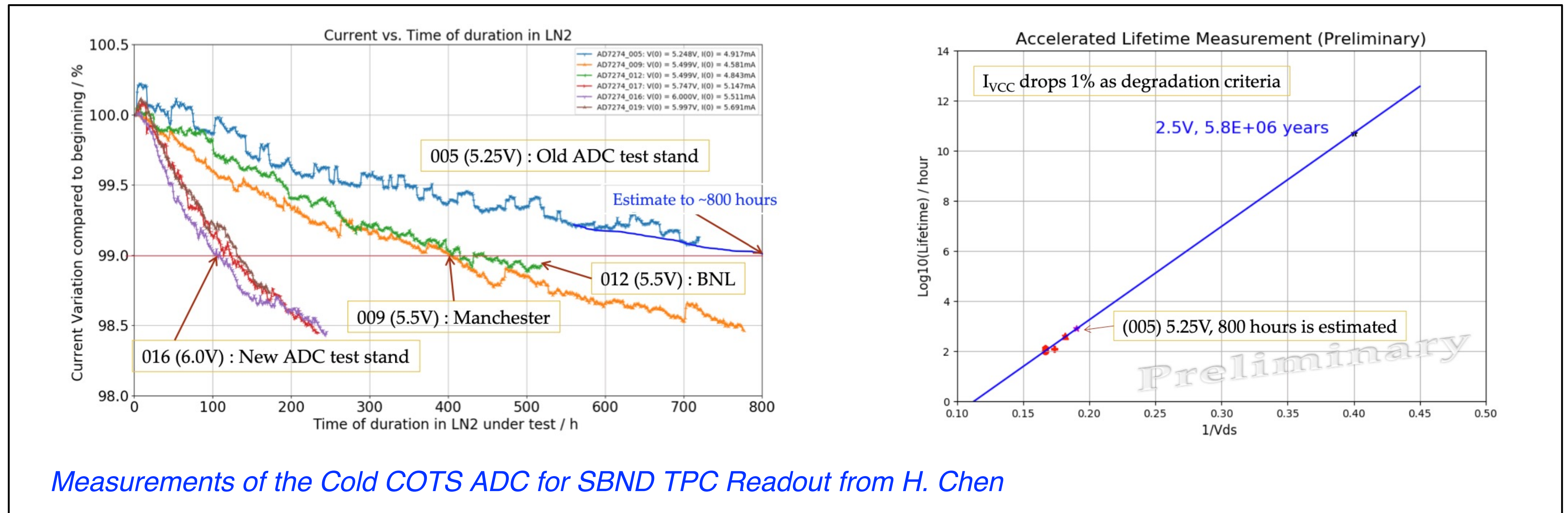
Lifetime study

- We improved the test stand and stabilized the data acquisition as the preparation for the lifetime study

  - Tuned the parameter to truncate ADC code in order to exclude outliers of DNL

  - Using averaged FFT results to alleviate the fluctuation of ENOB

  - Shielded the long cable and the dewar with aluminum foil

  - Adjusted the hanging position of the ADC

- Monitoring parameters

  - Dynamic linearity: effective number of bits (ENOB)

  - Static linearity: differential nonlinearity (DNL) and integral nonlinearity (INL)

- Status

  - The method to test lifetime is to increase the stress voltage (4.2V, 4.0V, 3.8V, 3.6 V) and study the degradation of performance

  - Two chips were stressed at 4.2 V, another three were stressed at 4.0 V, 3.8 V and 3.6 V respectively for the last year
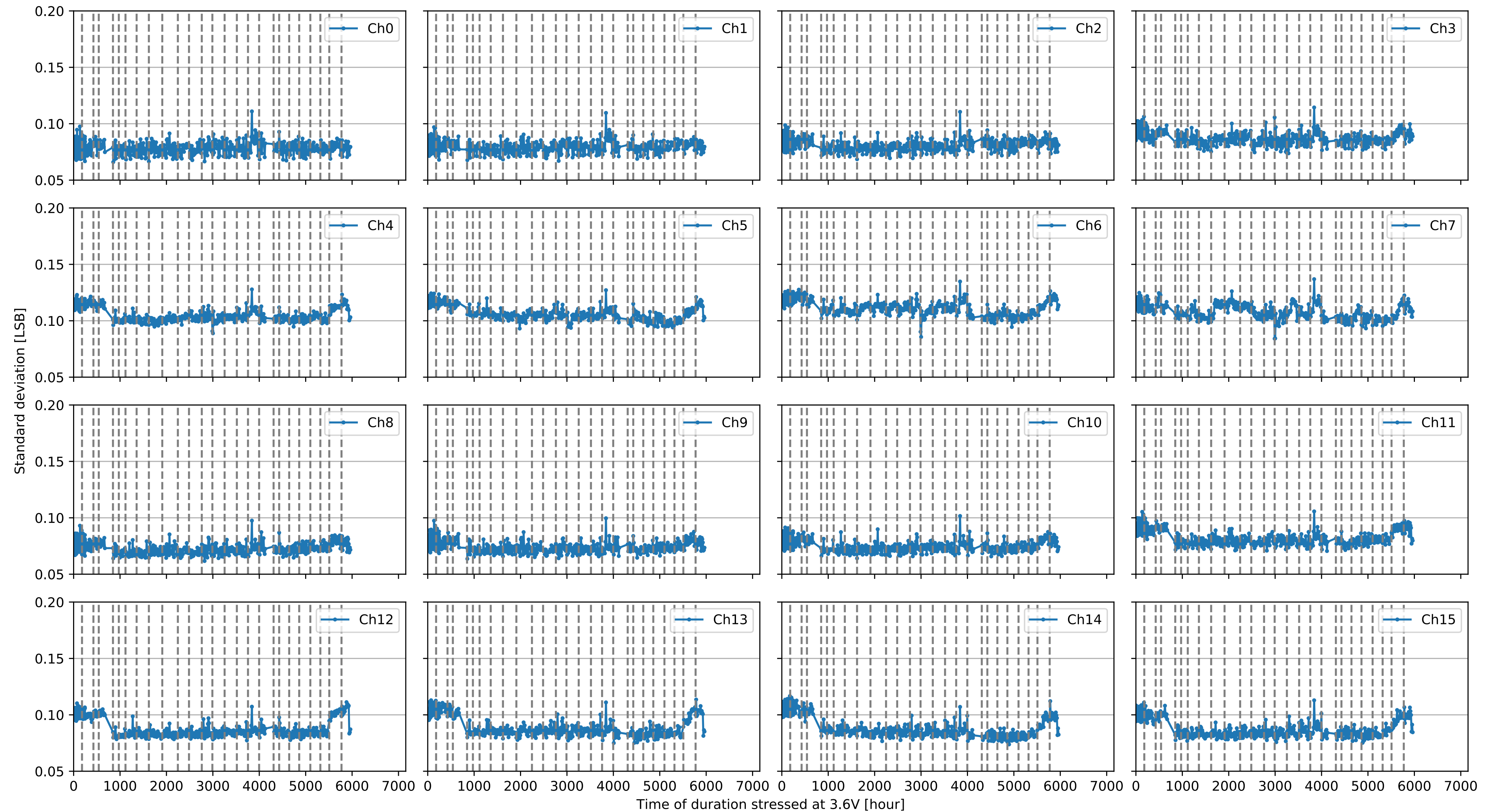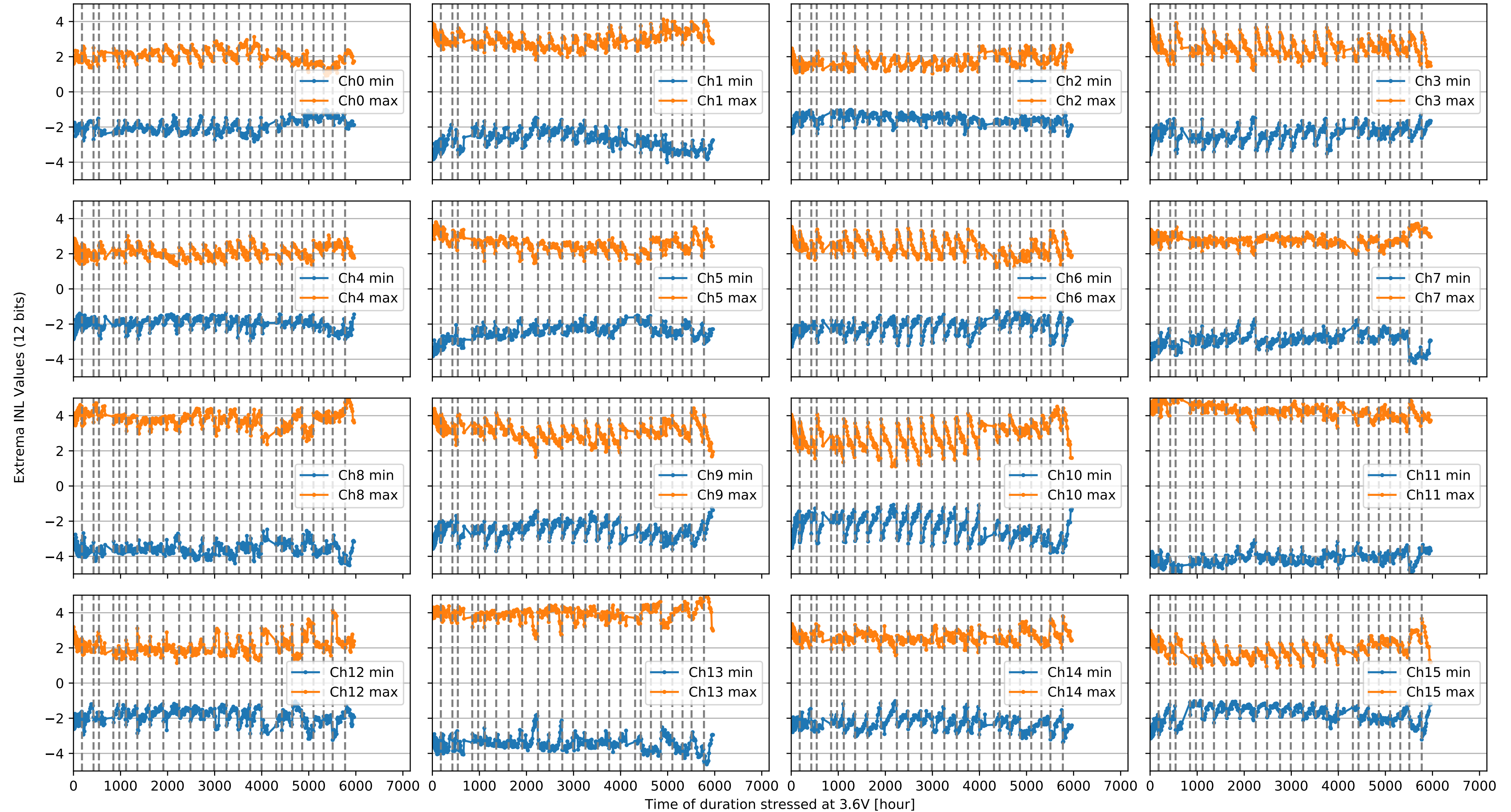
ENOB

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DNL: Extrema

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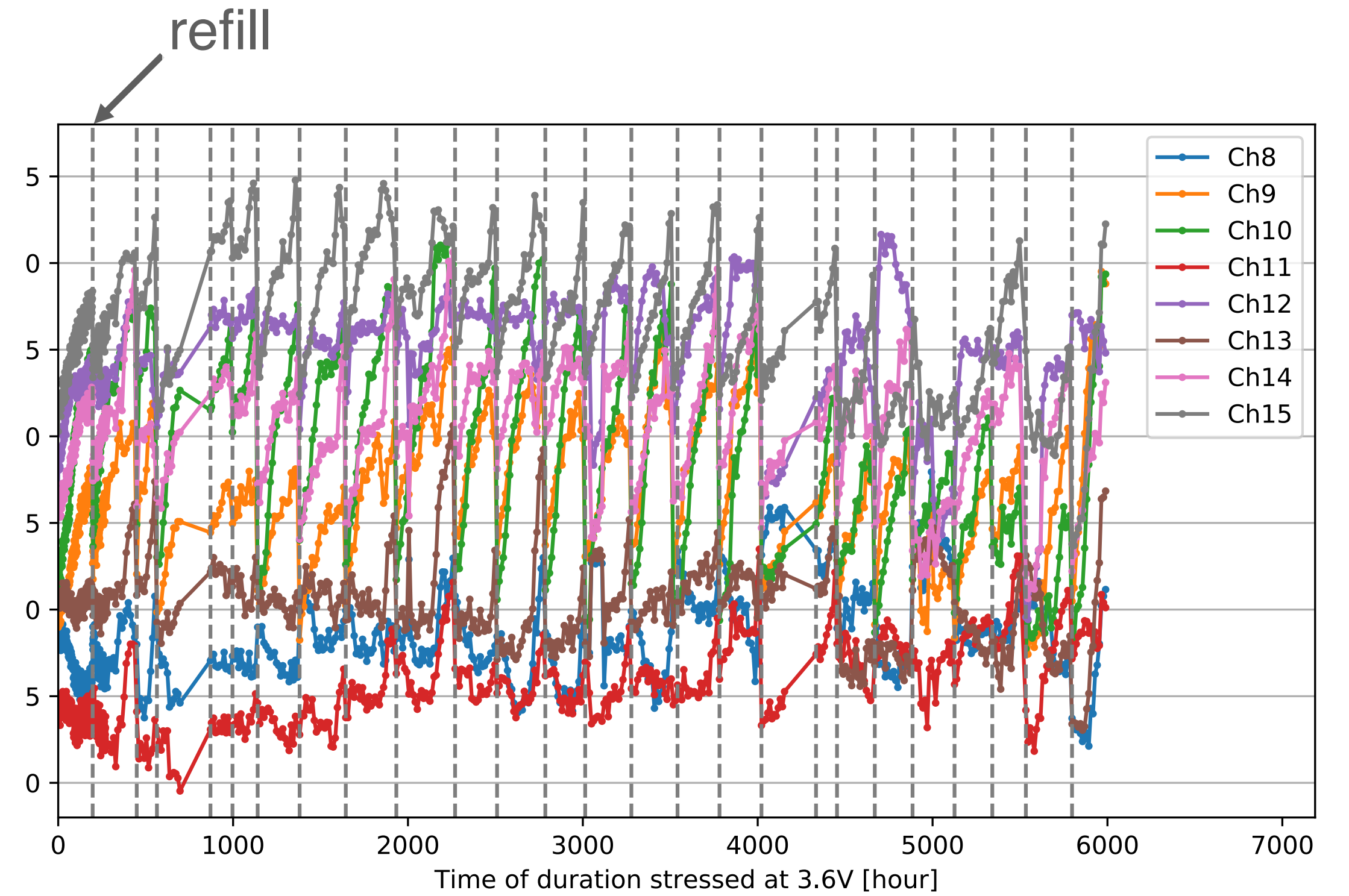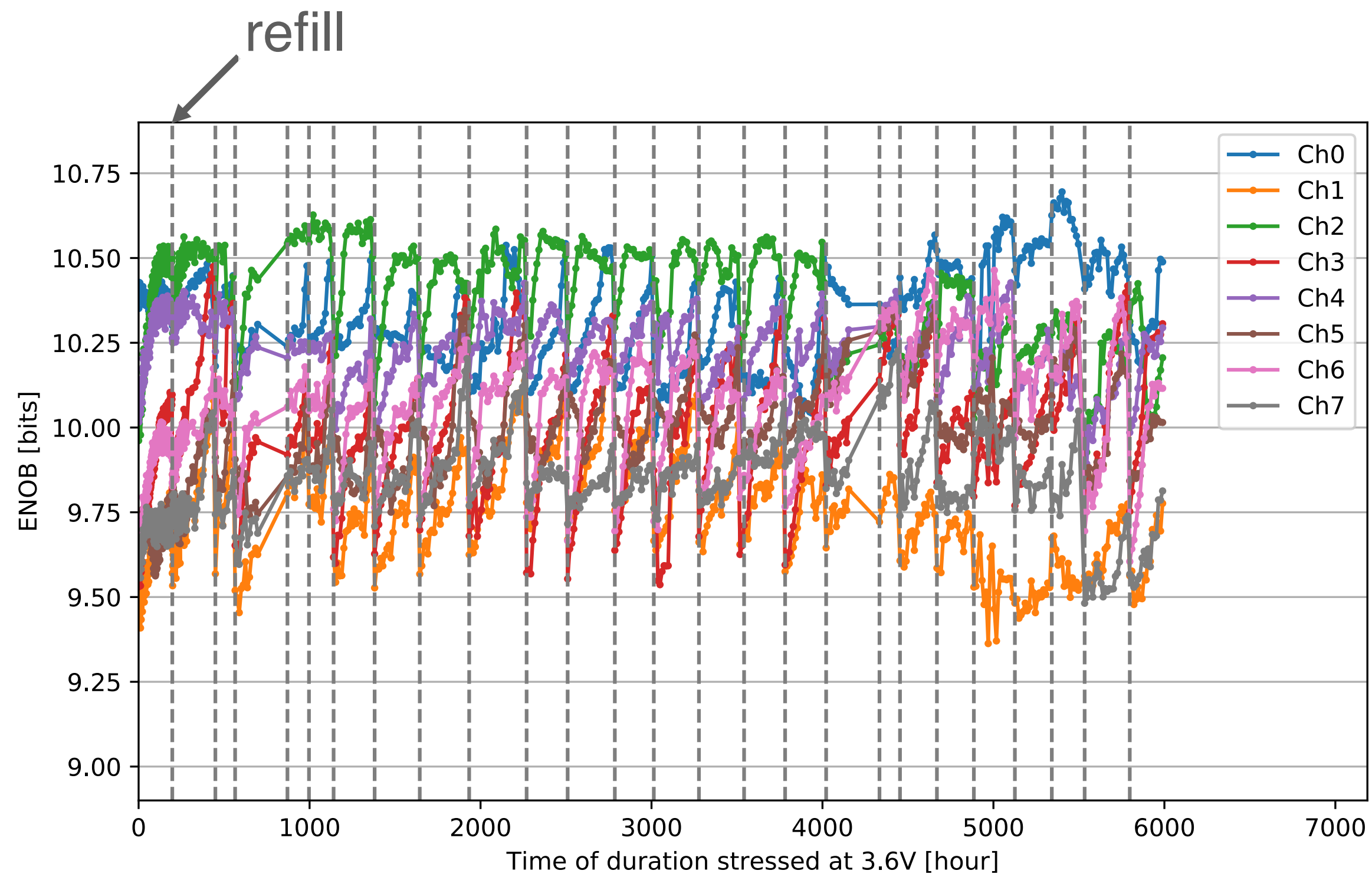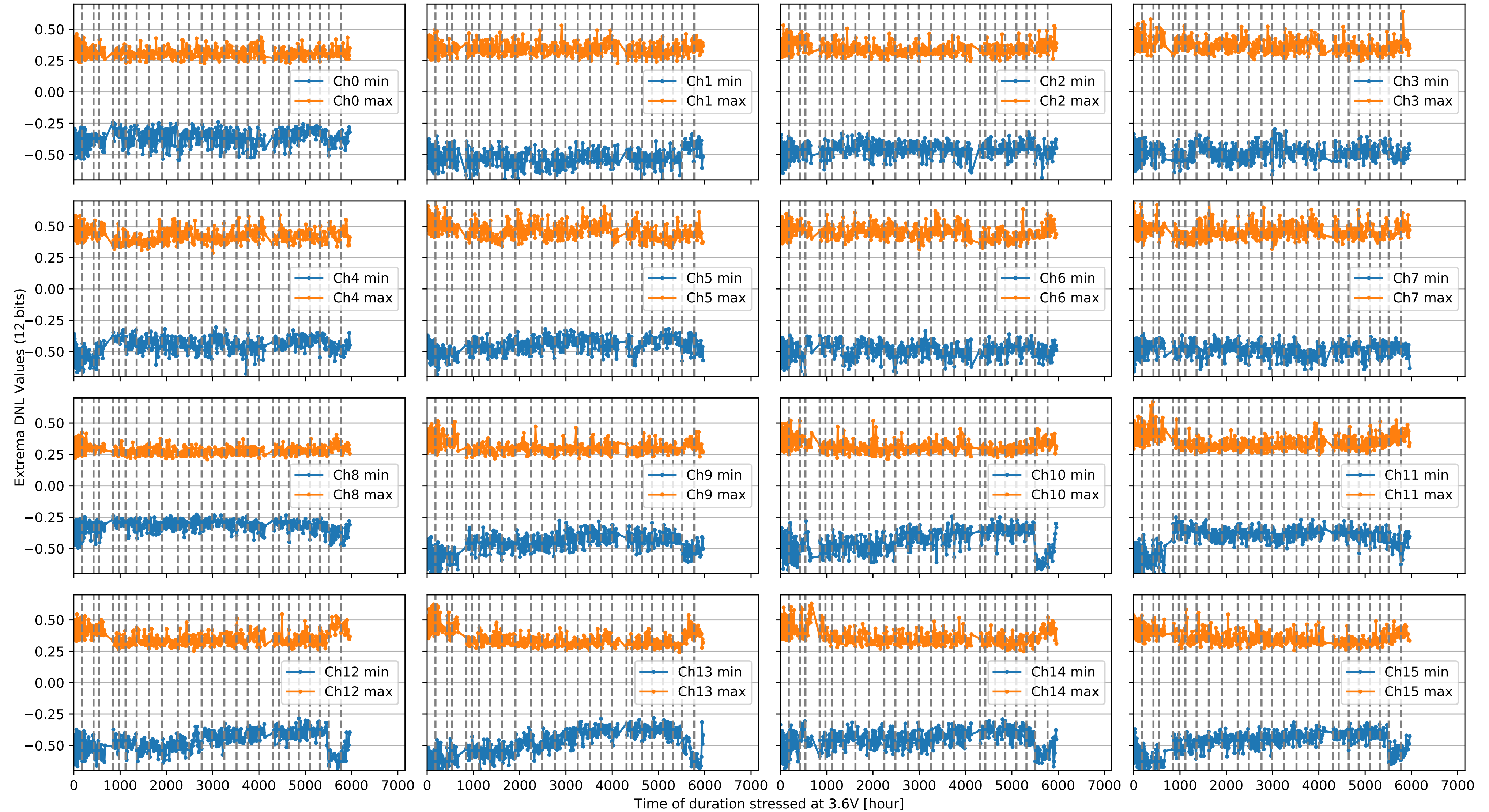
DNL: Standard deviation

INL: Extrema

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Calibration weights

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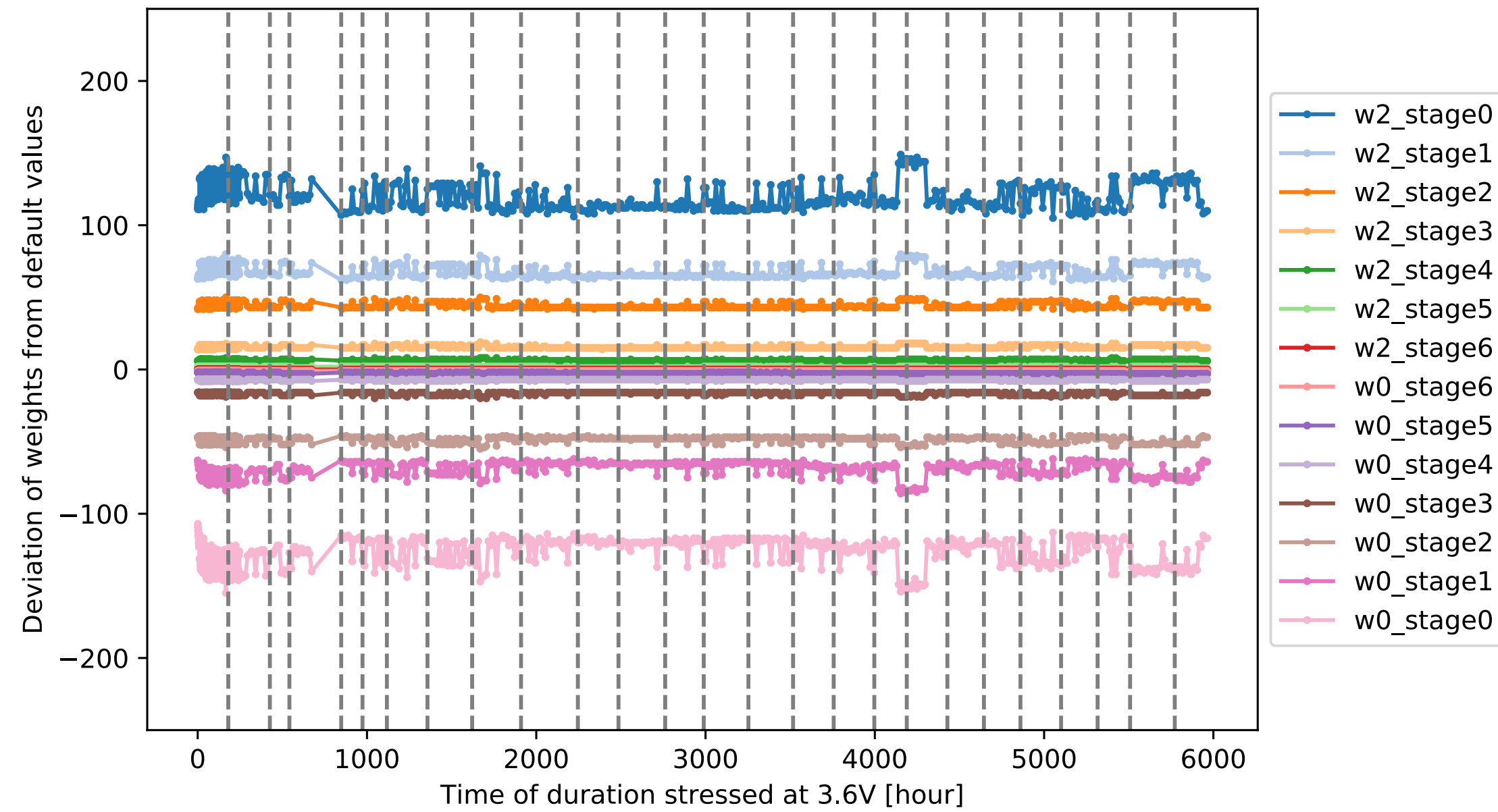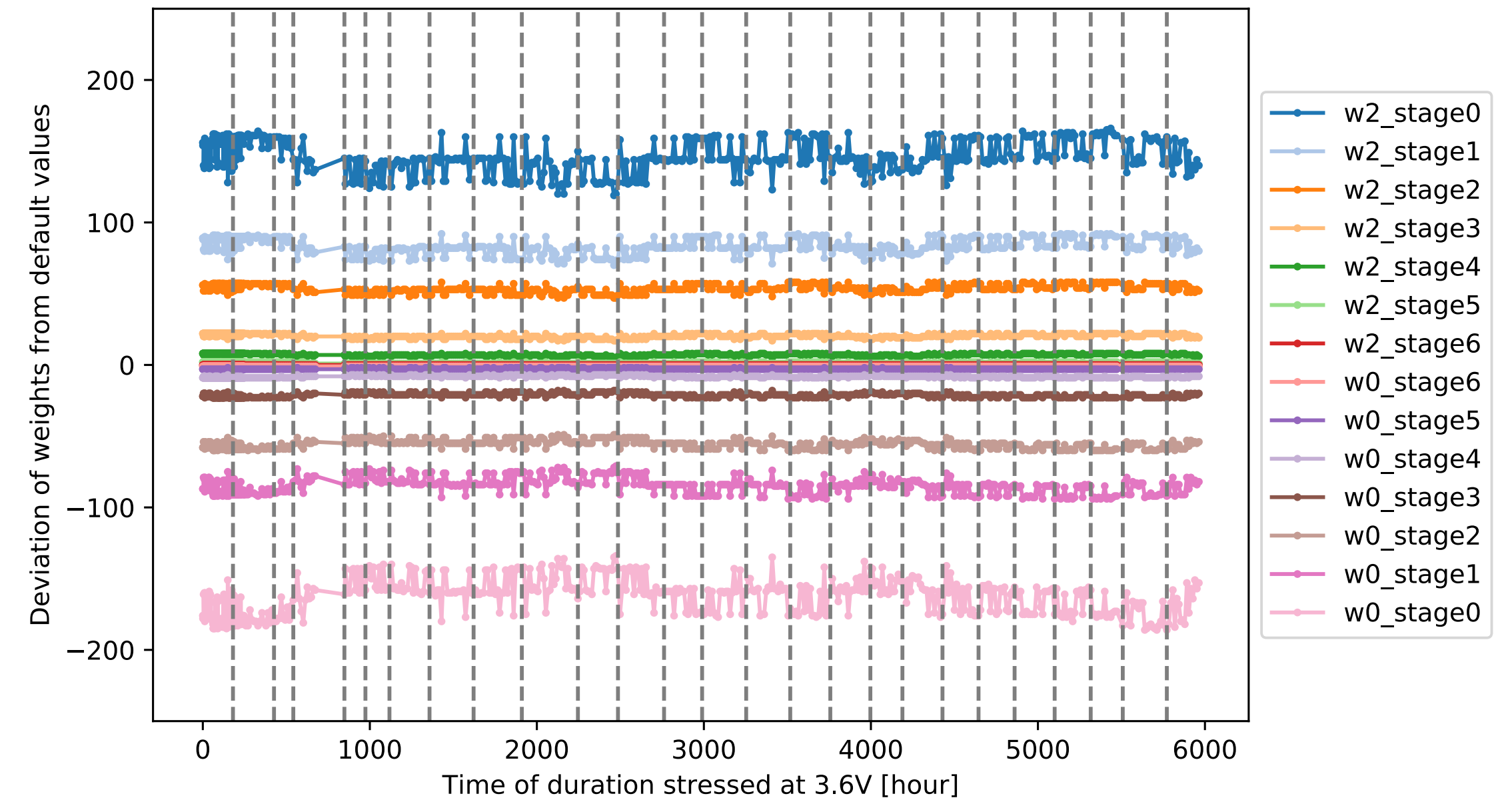
Current at 2.28V VDDA (current flowing through the VDDA2P)

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Current at 2.28V VDDA

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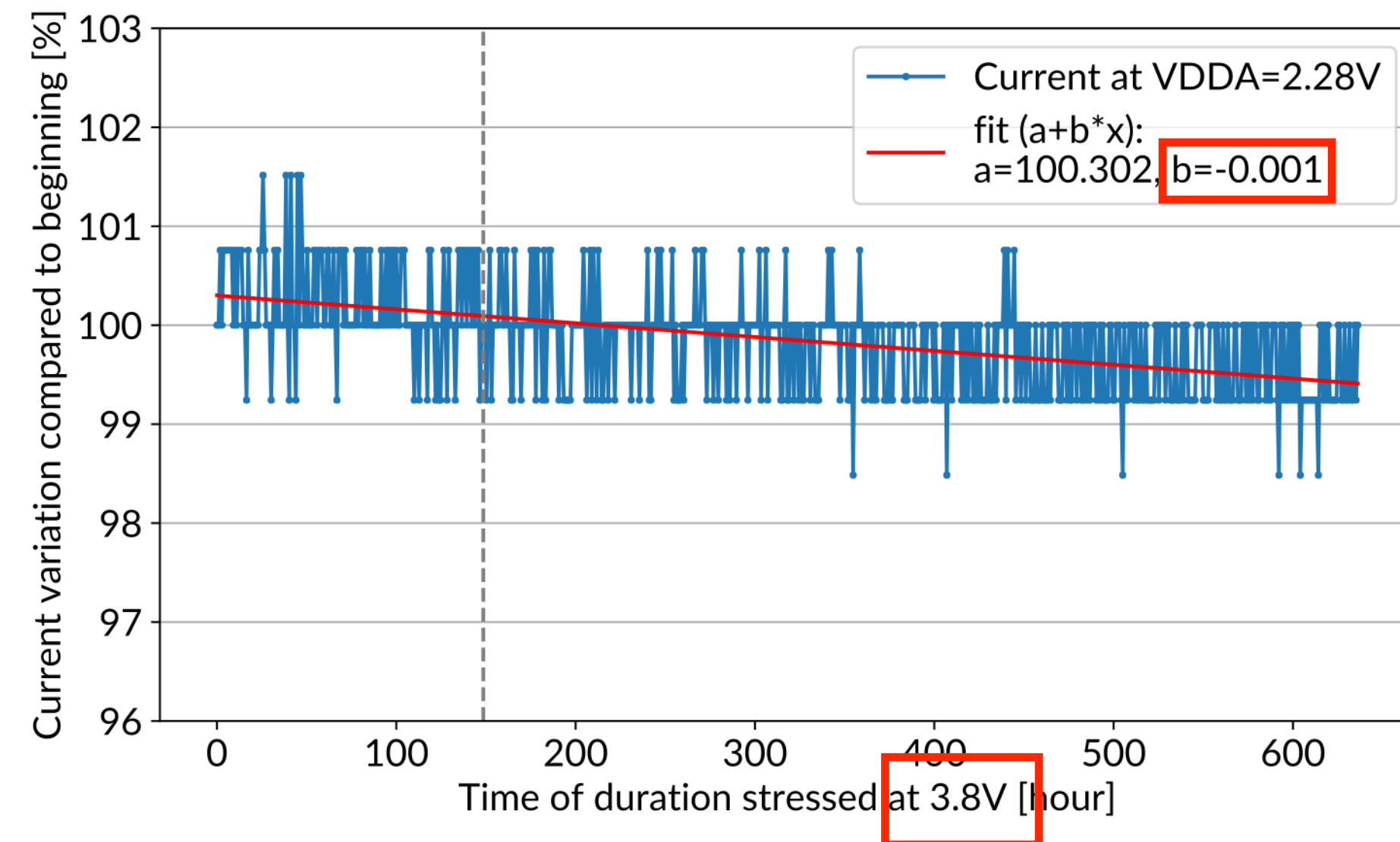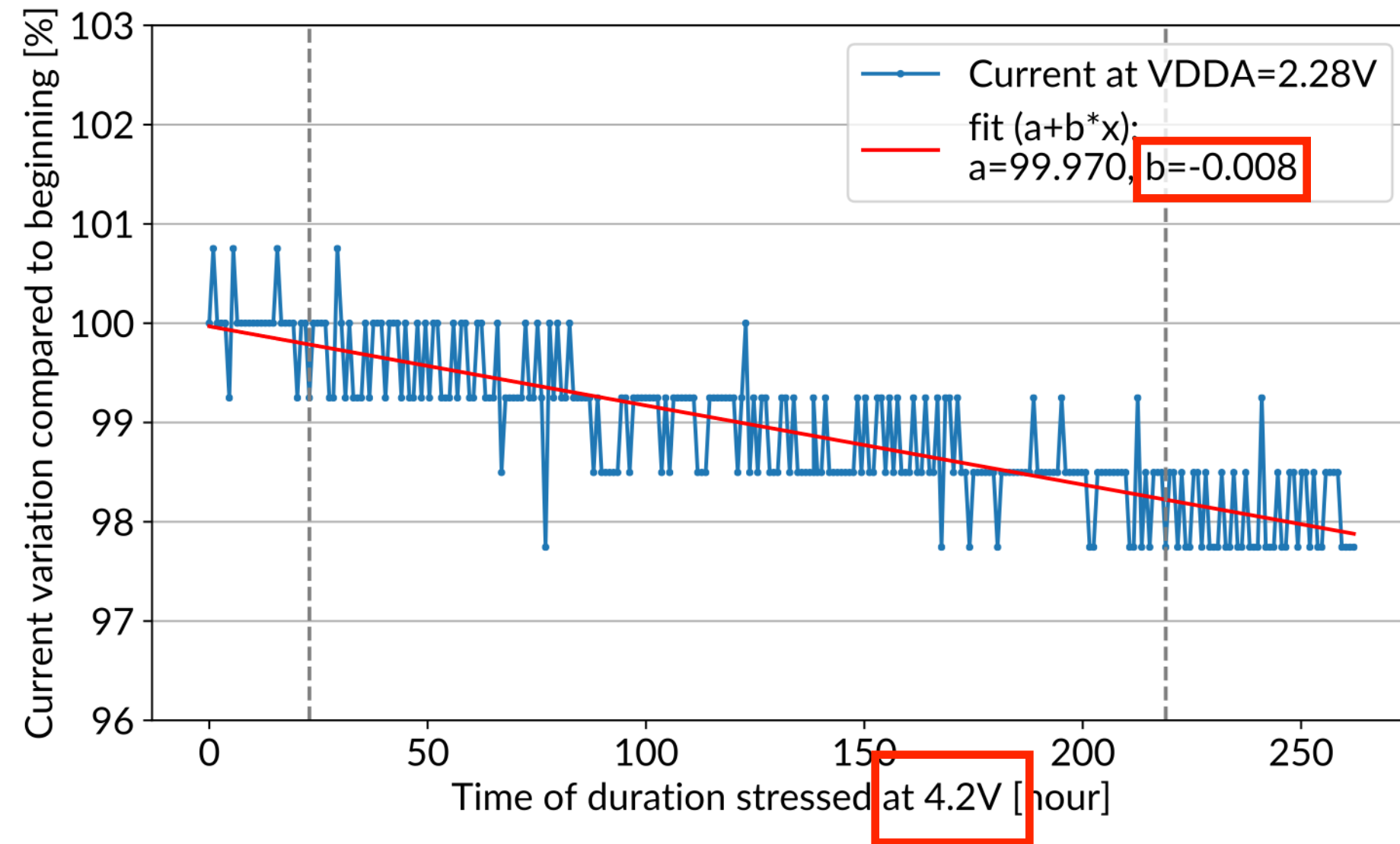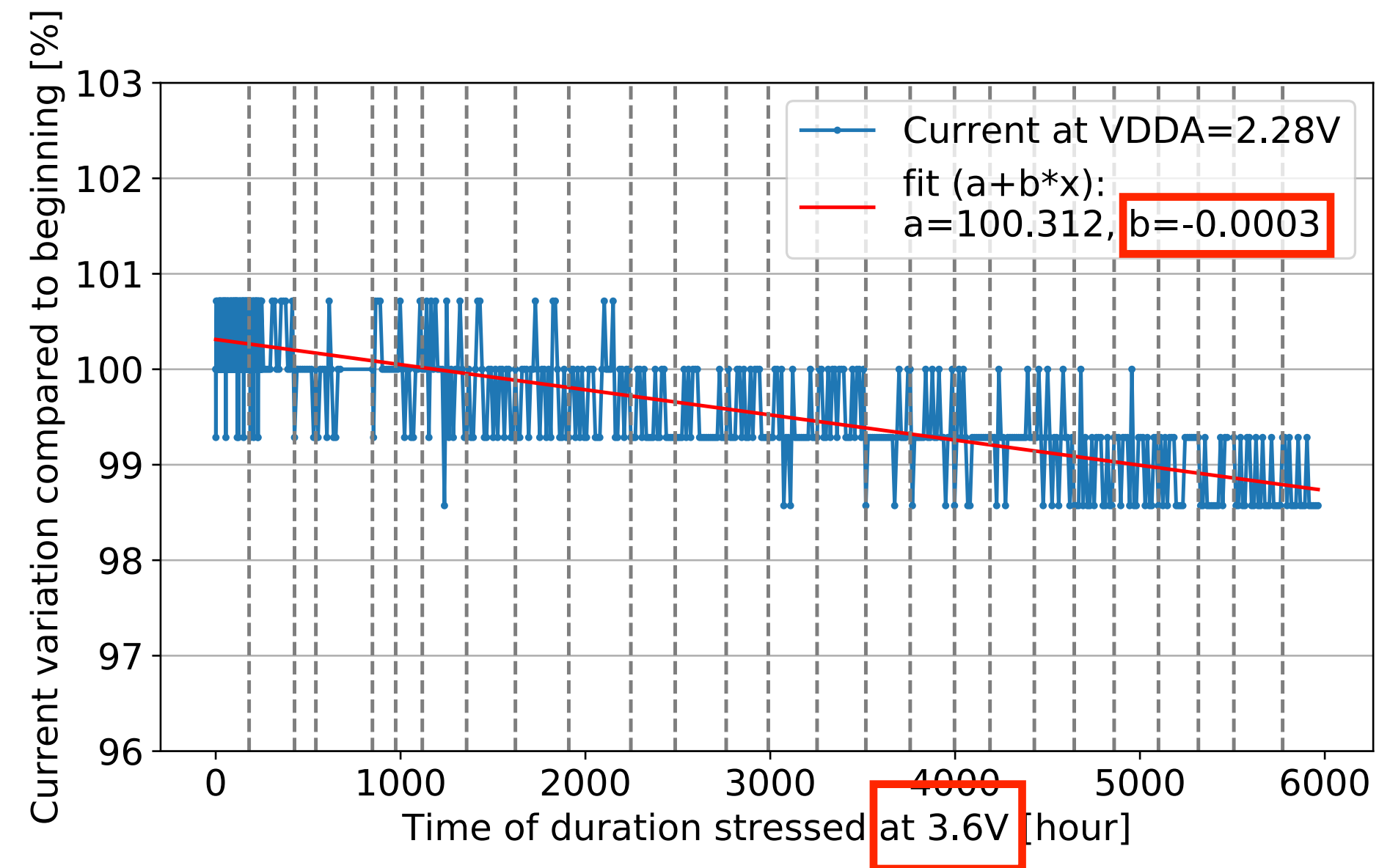
Lifetime

- **No obvious degradation of the performance (ENOB, DNL, INL) after hundreds of hours testing**

- Given no ADC failed the stress test at the moment, a conservative lower bound on lifetime is extracted by using "current drop of 1%" as the failure threshold (note: ADC performs fine at 1% current drop)

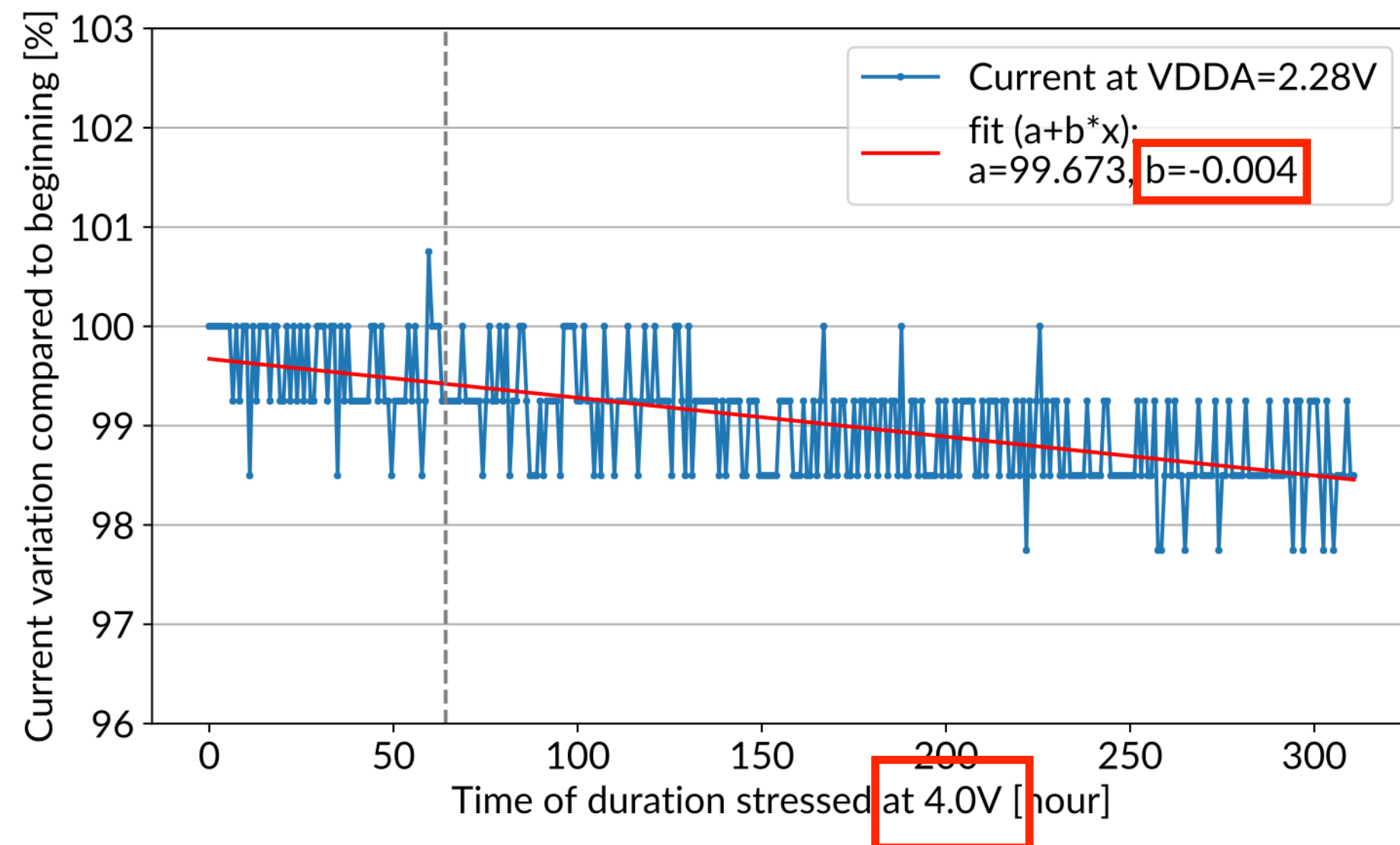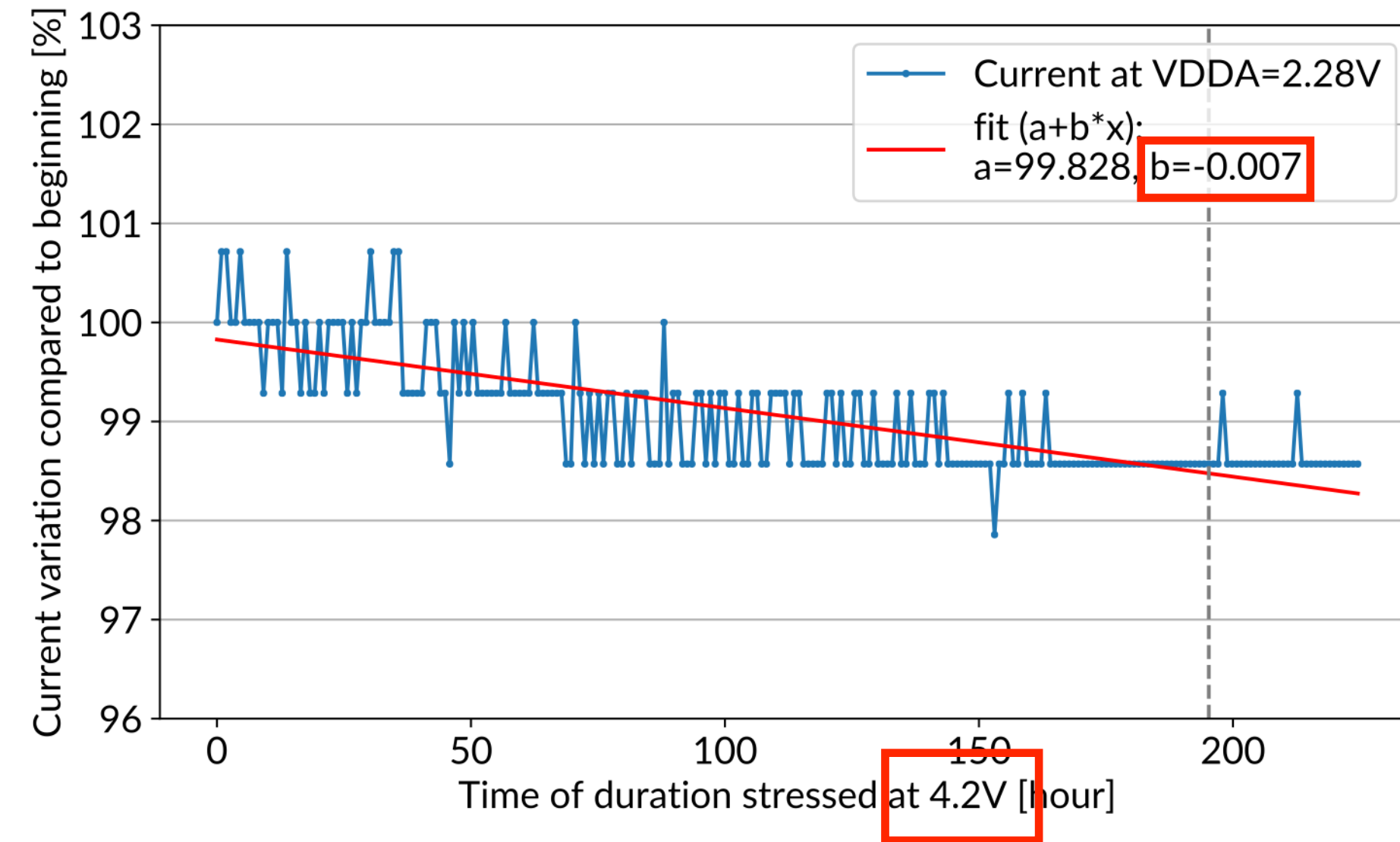- Use the difference between two measurements stressed at 4.2 V as the uncertainty from chip-to-chip. Use the error output from the fitting as the uncertainty of the measurements. Treat them as uncorrelated

- **It gives a lifetime of 3.02×10^5 years at 2.25 V**

Linear fit assuming $log_{10}\tau \propto 1/V$

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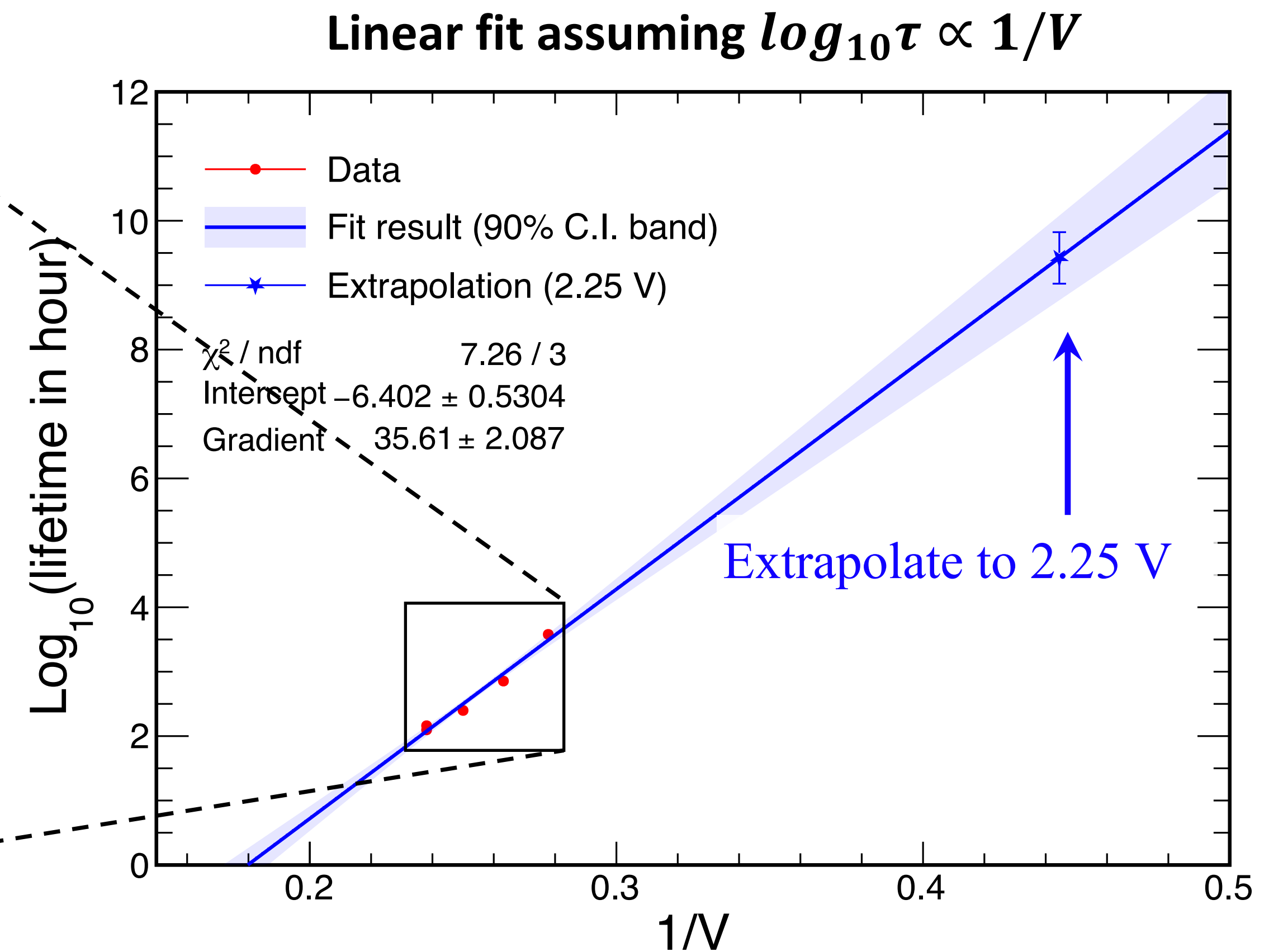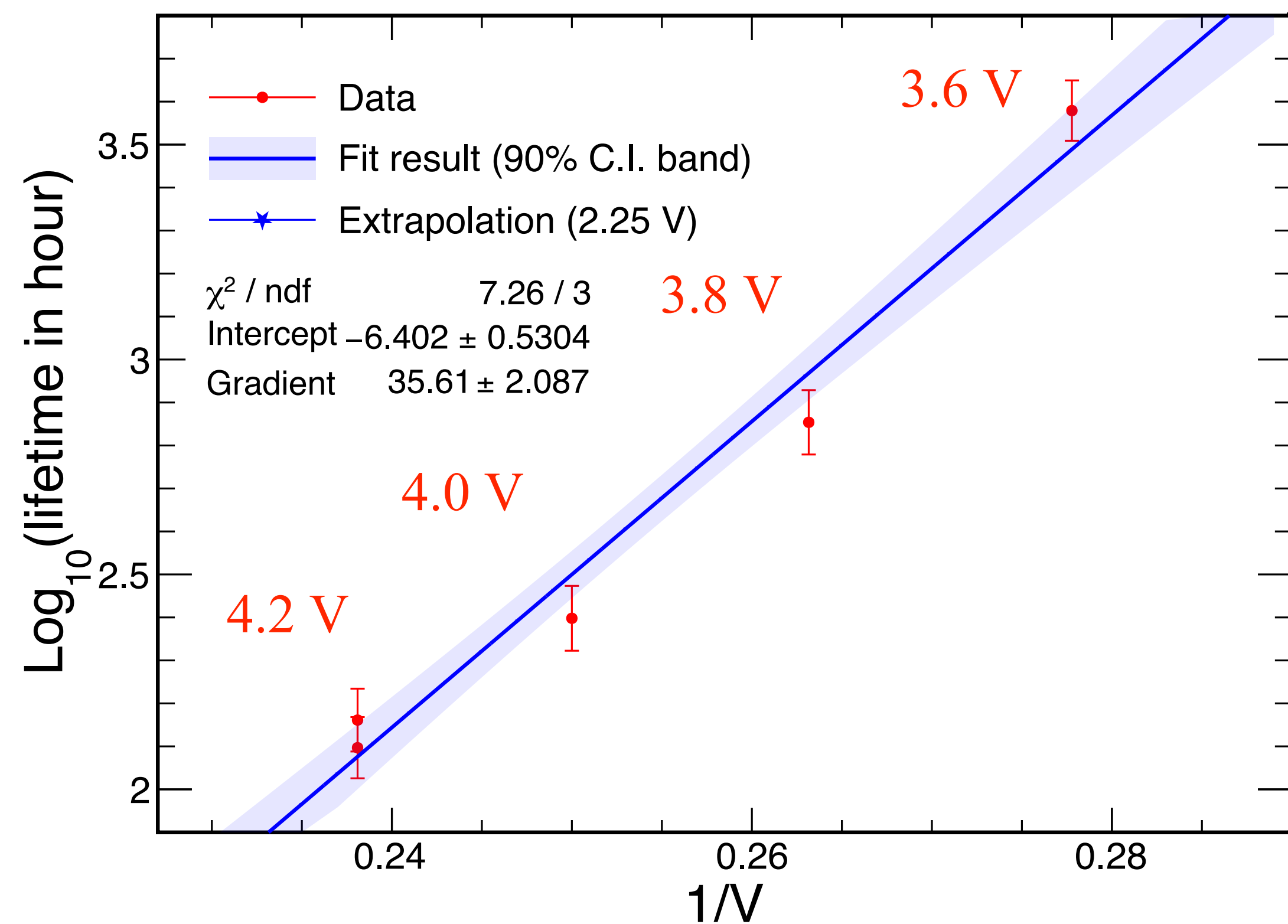
COLDATA lifetime study - Outline

- Reminder of hot carrier effect – caused by ionization of silicon by the most energetic carriers

  - Affects nMOS much much more than pMOS (electrons gain much more KE than holes)

  - Effect is proportional E field in channel & thus to Vgs → Analog circuits and high speed digital circuits are most vulnerable

  - **Affects shortest transistors most (because E is highest for a given Vgs)**

- TSMC 65nm CMOS

  - Standard transistors (1.2V)

  - Thick oxide transistors (2.5V)

- ColdADC

  - 2.5V transistors used for analog circuits

  - 1.2V transistors used for digital circuits (level translators required to control circuits in the 2.5V domain)

  - No minimum length (60nm) transistors used (min length used = 90nm)

  - Digital design uses custom standard cell library (with 90nm transistors instead of 60nm)

  - Designed to operate at 90% of nominal bias voltage (2.25V/1.1V)

- COLDATA

  - **Only 1.2V transistors used**

  - **No minimum length transistors used; custom digital library used**

  - Designed to operate at 1.1V

COLDATA lifetime study

- Careful study by FNAL/SMU ASIC groups concluded that the shortest TSMC 65nm 1.2V transistors have >20 yr lifetime at 77K even if operated at 1.3V bias.

- Explicit lifetime tests using elevated bias voltage at ~80K underway.

  - Focused on PLL (analog and 2.5 GHz digital circuits) and Serializer/Output links (1.25 GHz digital)

  - Measured PLL locking range and 1.25 Gbps link eye diagram.

  - No degradation measured in 3 samples stressed at 2.5V for up to ~300 hours.

  - Decline in the current drawn from analog bias supply observed (consistent with increased threshold voltage of nMOS transistors).

Summary for the lifetime study

- Accelerated lifetime test at cryogenic temperature were performed for both ColdADC and COLDATA (well-established by foundries)

  - transistor is placed under a severe electric field stress (large V), to reduce the lifetime due to hot-electron degradation to a practically observable range

- A conservative lower bound on lifetime for ColdADC was measured to be 3.02×10^5 years

Backup

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LArASIC Lifetime study

- The remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature is the degradation (aging) due to channel hot carrier effects (HCE)

- **LArASIC is designed for long lifetime at cryogenic temperatures**

  - Low voltage and current in each transistor

Measurement Type II: Substrate Current Density I_{sub}/W vs $1/V_{ds}$
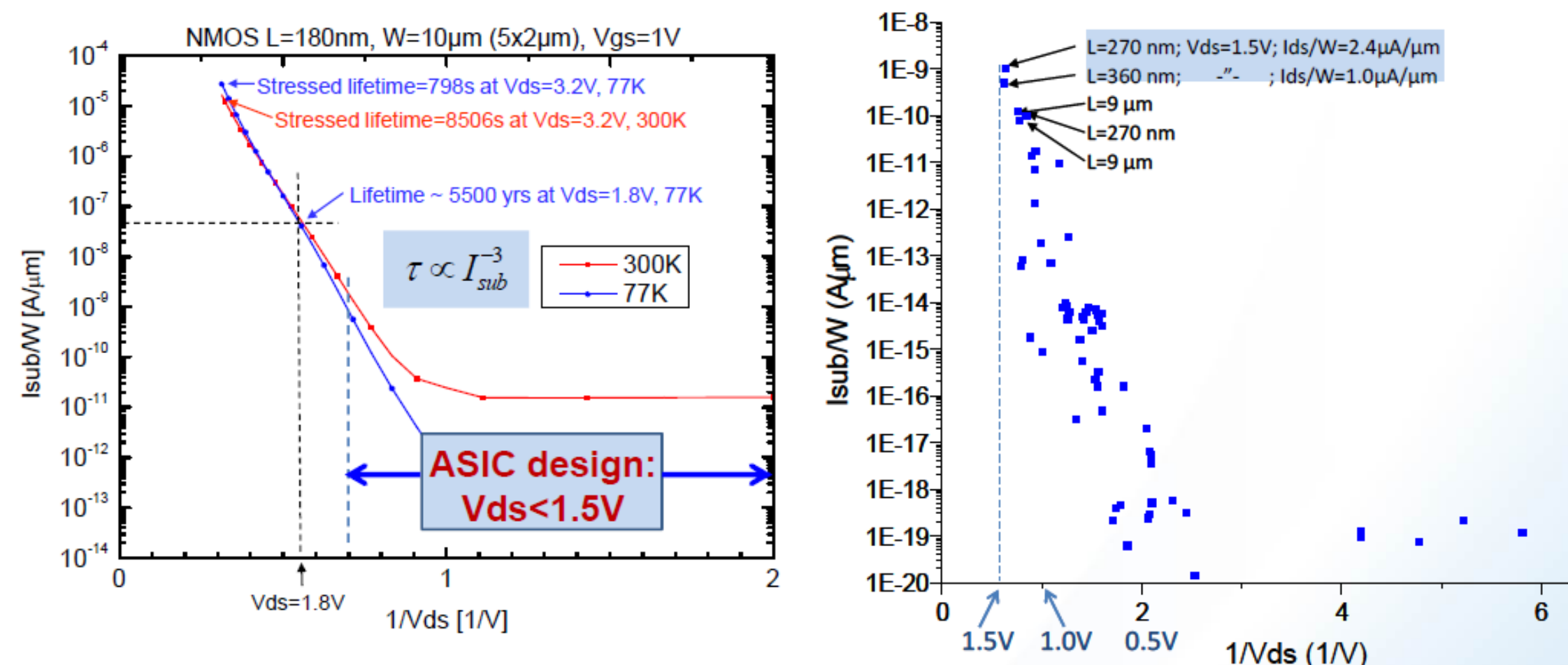
- One order of magnitude in substrate current I_{sub} corresponds to *three orders* of magnitude in lifetime. At 77 K, V_{ds} = 1.8 V projects a lifetime of ~5500 years.

- I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC (TSMC 180nm, 1.8V node) shows that all transistors are well below nominal voltage of 1.8V and at low I_{sub}; *Reduced V_{ds} < 1.5 V results in essentially making HCE negligible and a very long extrapolated life time.*

Brookhaven Science Associates

To alleviate the lifetime risk, **custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years**

Any transistor falling in the region V_{ds} <1.5 V and I_{sub}/W < 10^{-9} A/m should have a very long lifetime

S. Li, et al, "LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Transactions on Nuclear Science, Volume: 60, Issue: 6, Part: 2, Pages: 4737-4743 (2013)

LArASIC Lifetime study

- LArASIC in MicroBooNE: **No observable change after seven years**
- ProtoDUNE-I (SP): No measurement degradation is observed over a year
  - The measured gain shift is around 0.13% and 0.4%RMS, with an excellent agreement between 2018 and 2019 (around 0.01% shift with 0.3% RMS)
- The lifetime study of LArASIC will take place in two different phases, the exploratory phase and the validation phase. Before that, we will need to prepare the test stand to make it suitable for lifetime study, which is the preparation phase. The most time and effort will focus on the exploratory phase, we will gain (or lose) confidence based on the test results in this phase. Validation phase will be useful to validate what we would learn in the exploratory phase, and collect more information to prepare for future review(s)
  - **A P5 LArASIC was stressed at 3.0V over 300 hours in liquid nitrogen, no significant change in current drawn is observed.**
  - The recommended voltage for CM018/G is 1.8 V + 10%, which limits the stress voltage
    - commercial chips designed in TSMC 180 nm, e.g., AD9265 and AD9650, the absolute maximum rating is 2.0 V which is consistent with 1.8V + 10%
  - Test setup will be optimized with the dual-dut test board to observe more performance parameters
  - More tests are being done for P5 B @ BNL

APA: Histogram of Difference between Area Gain of (09/23/2018) and Area Gain of (12/17/2019)
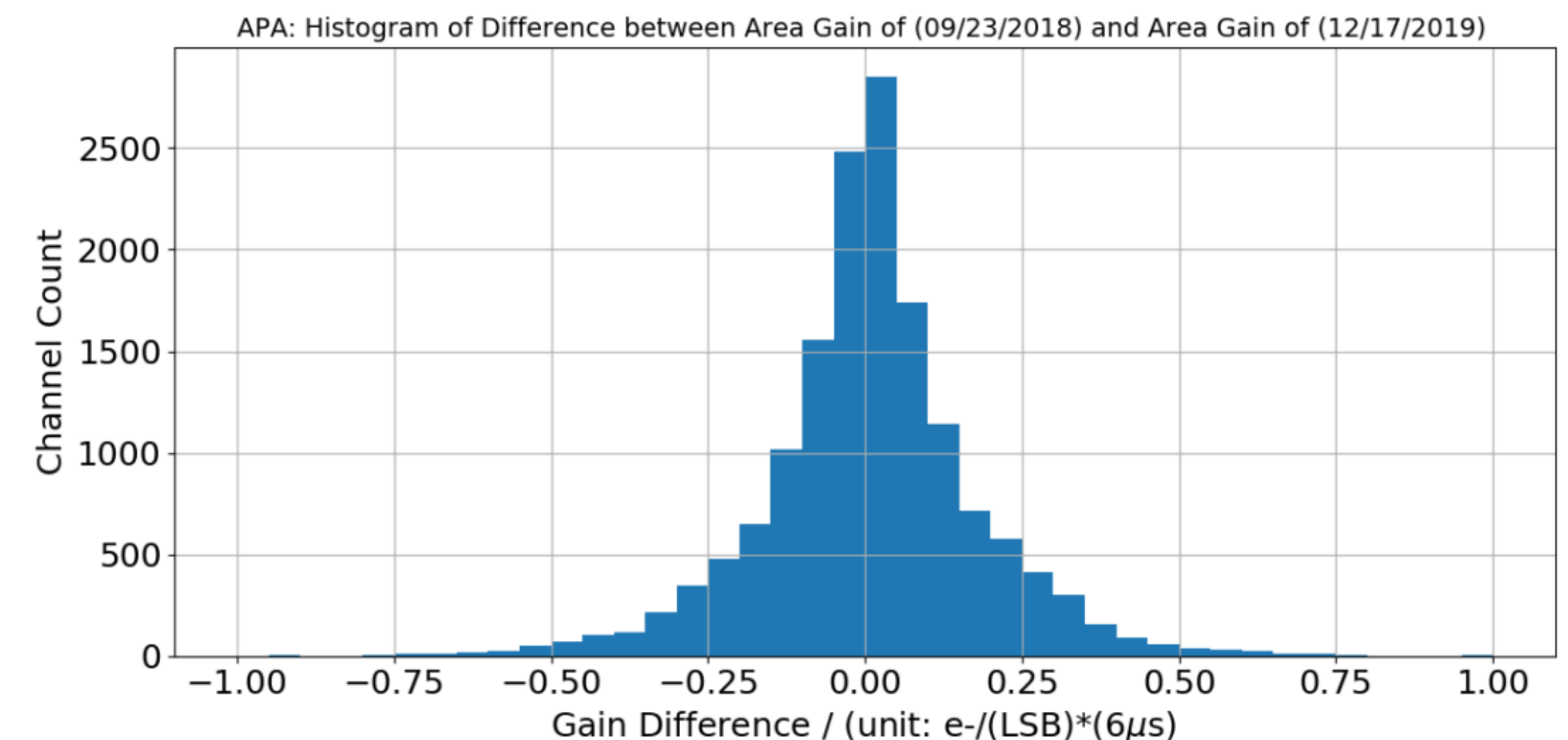
ProtoDUNE-SP: Good reliability over a year operation

Monitoring parameters

- Static linearity: differential nonlinearity (DNL) and integral nonlinearity (INL)

  - DNL is the deviation of the code transition width from the ideal width of 1 LSB. All code widths in the ideal ADC are 1 LSB wide, so the DNL would be zero.

  - INL is the distance of the code centers from the ideal line. If all code centers land on the ideal line, the INL would also be zero
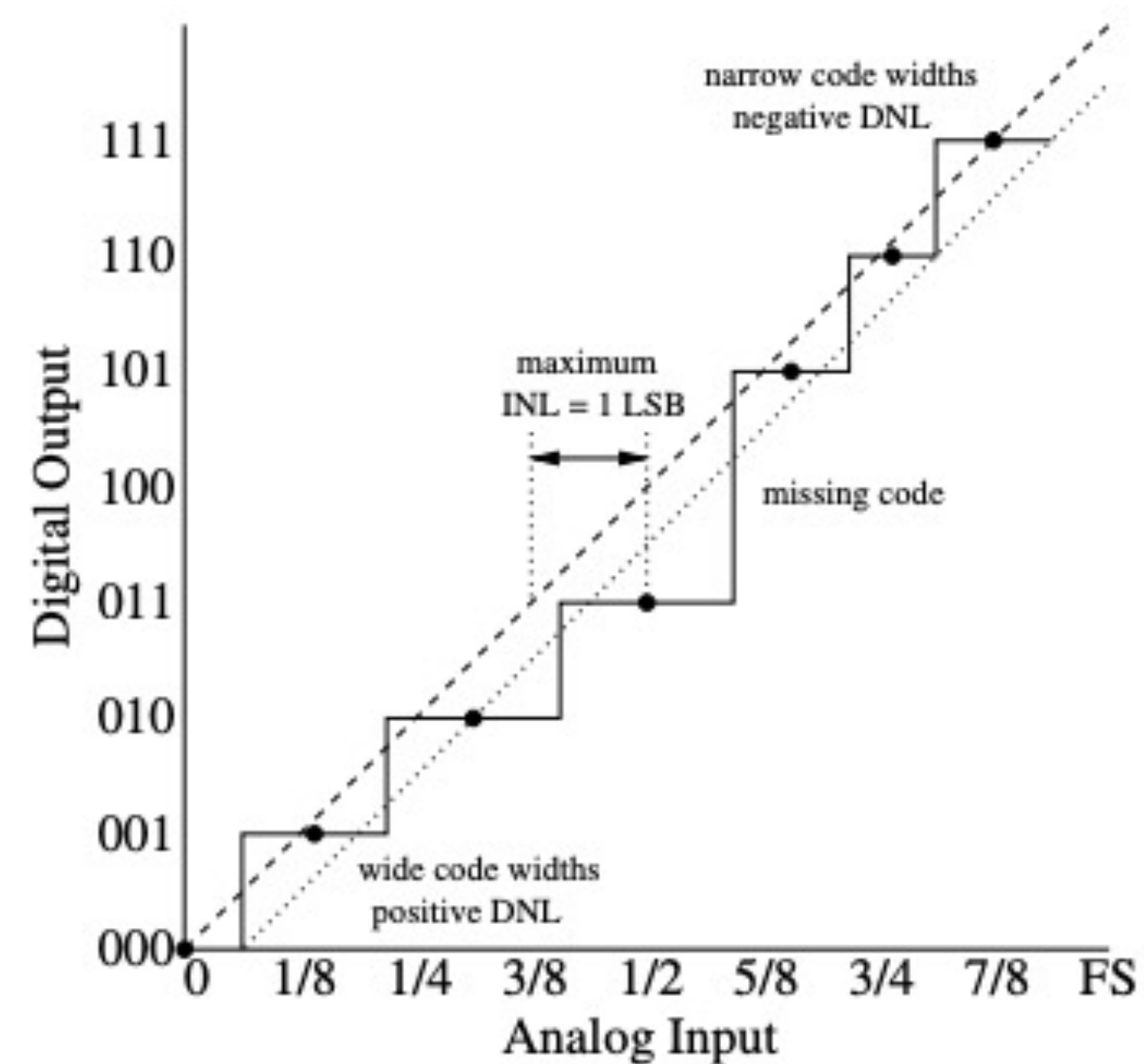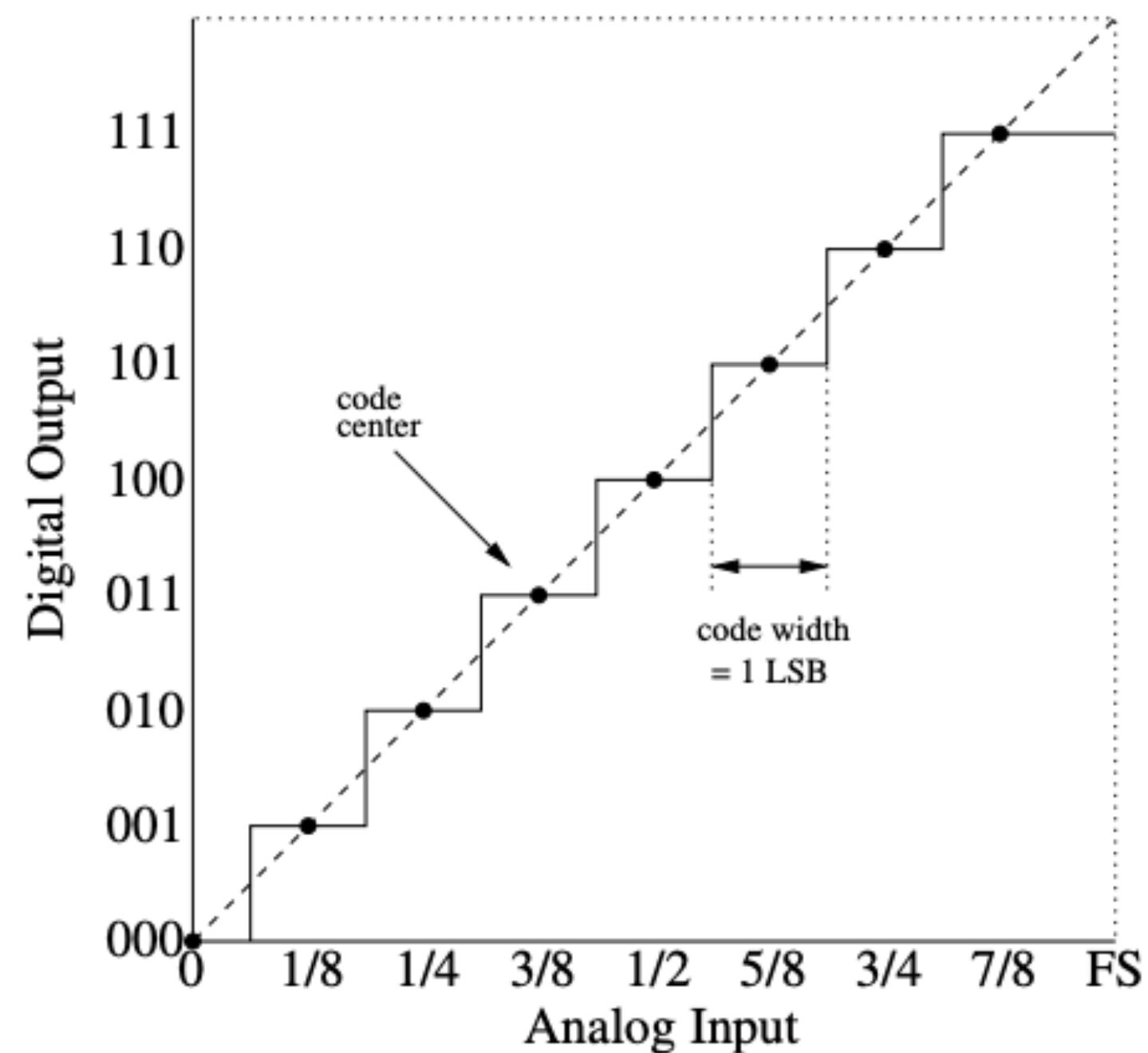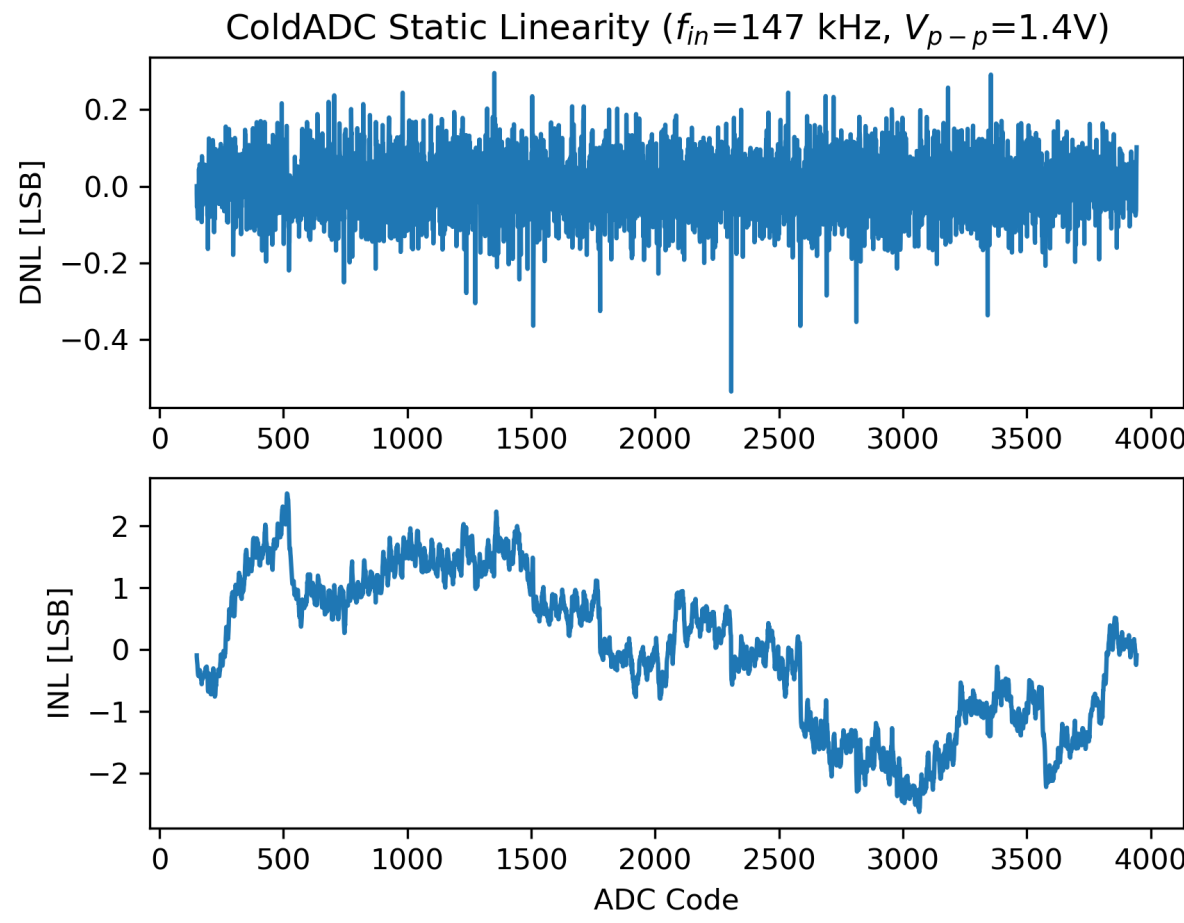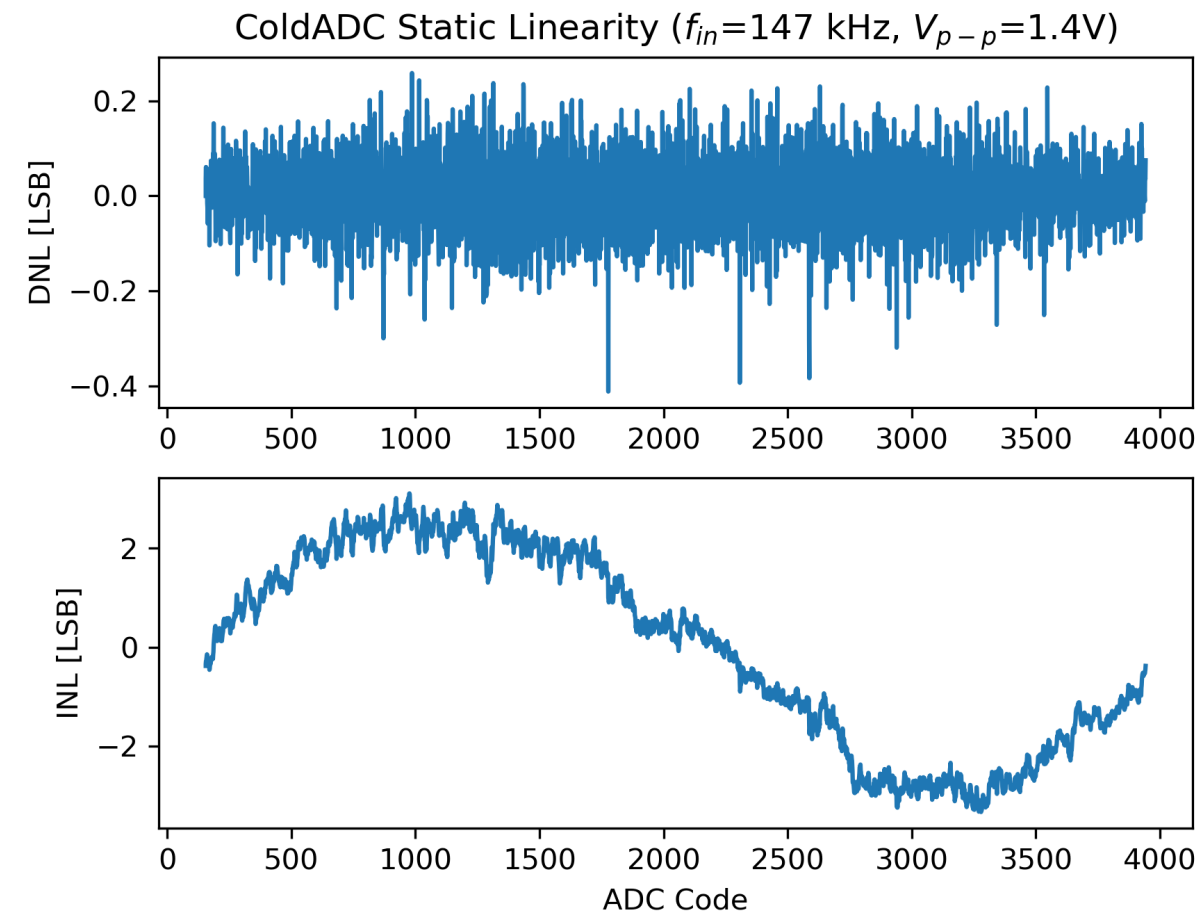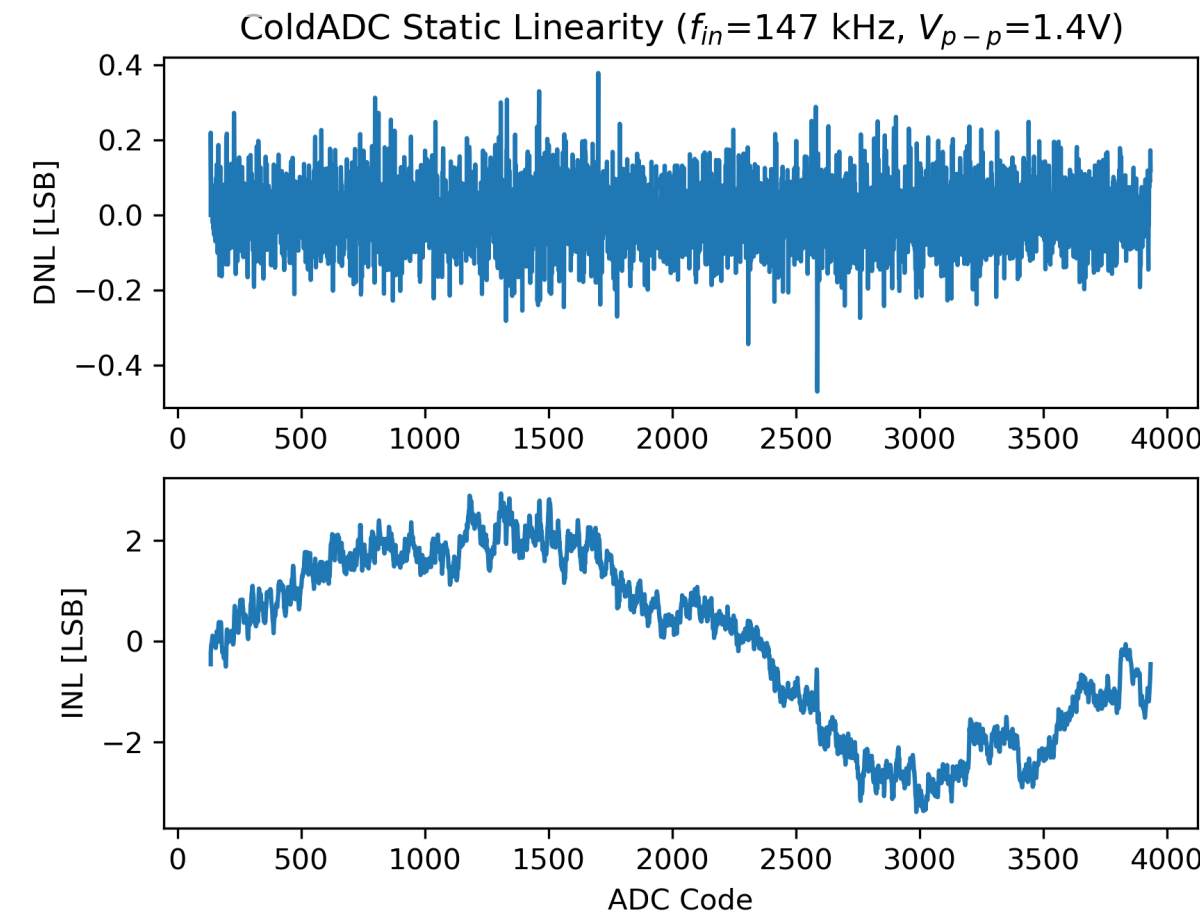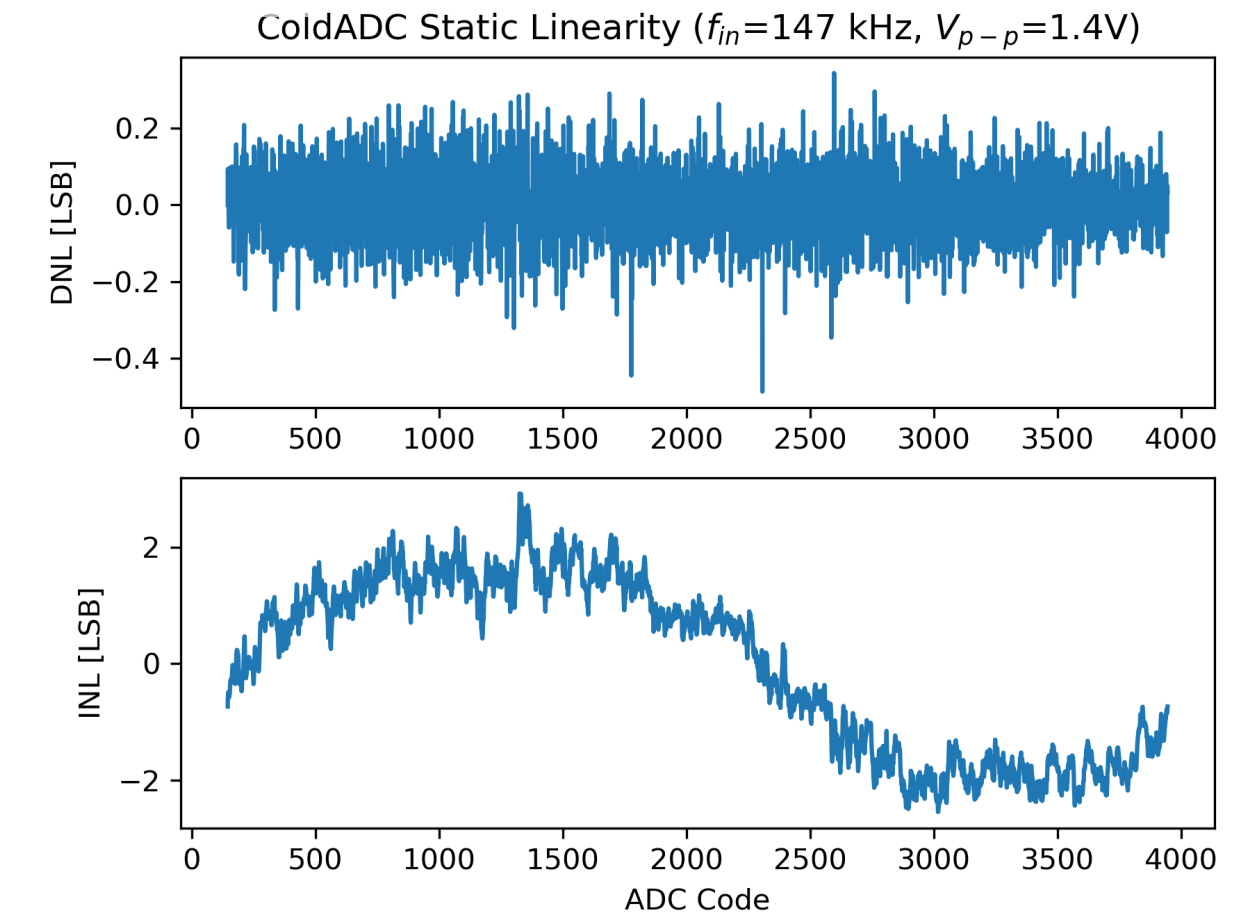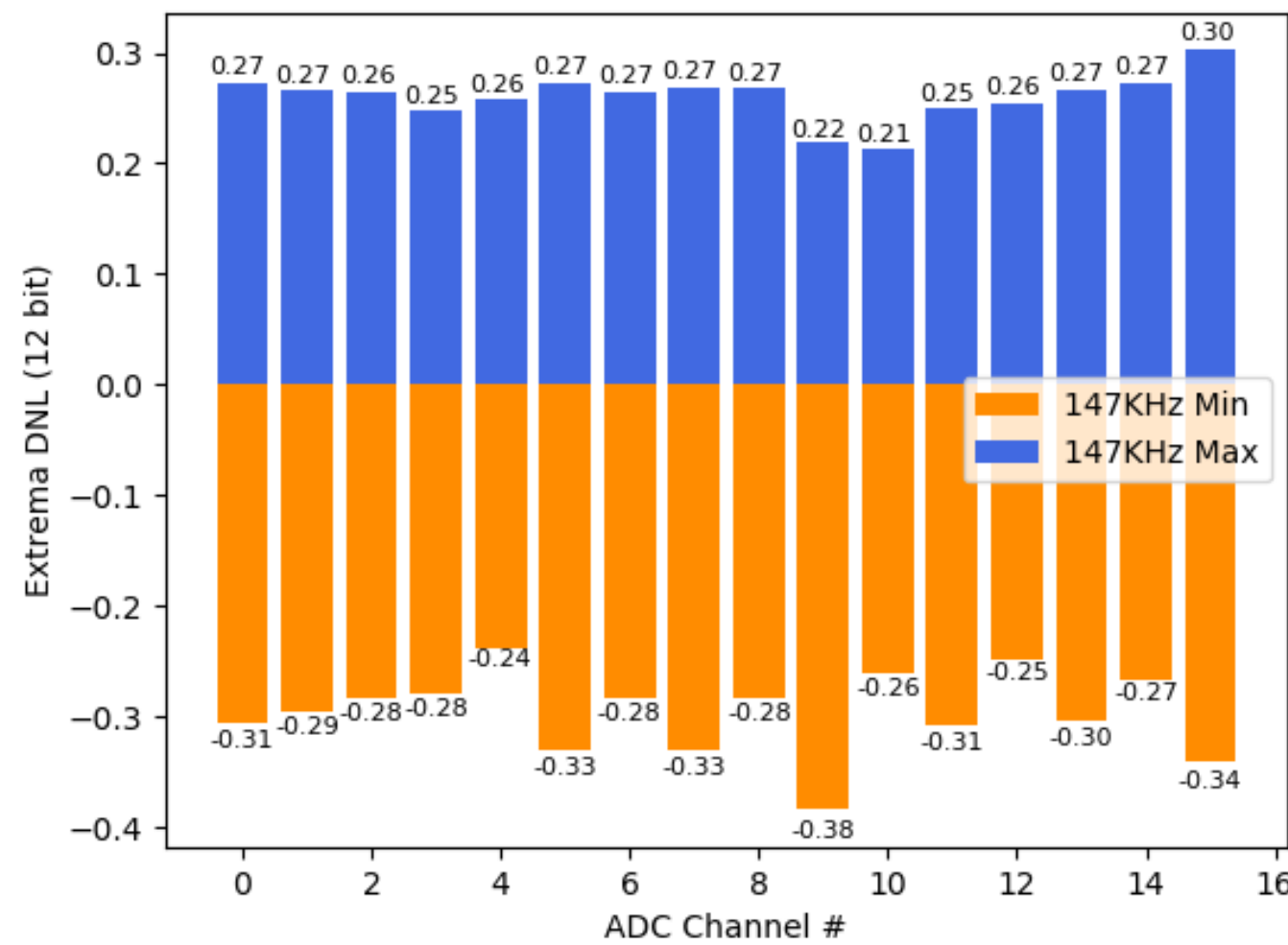

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Monitoring parameters

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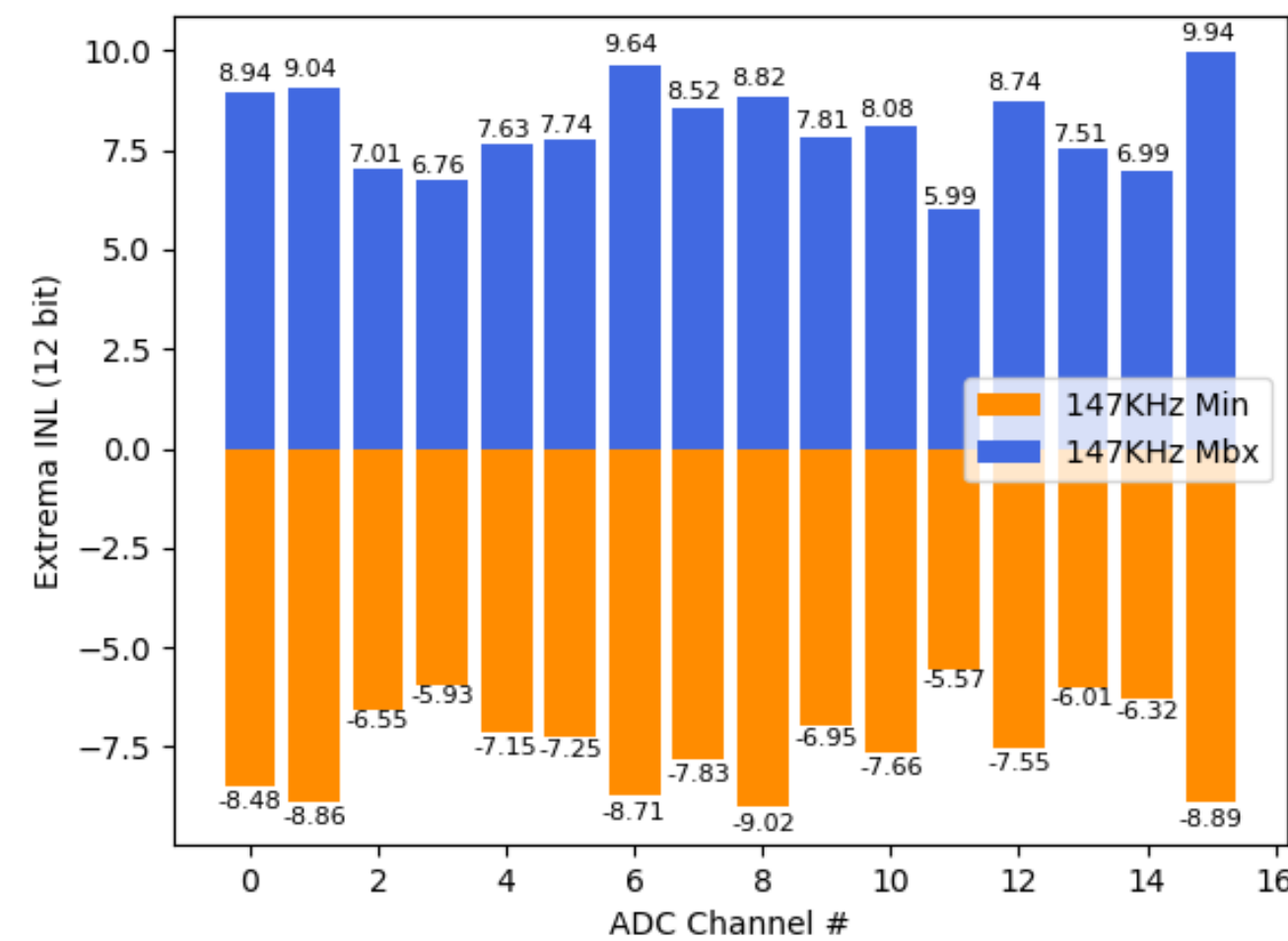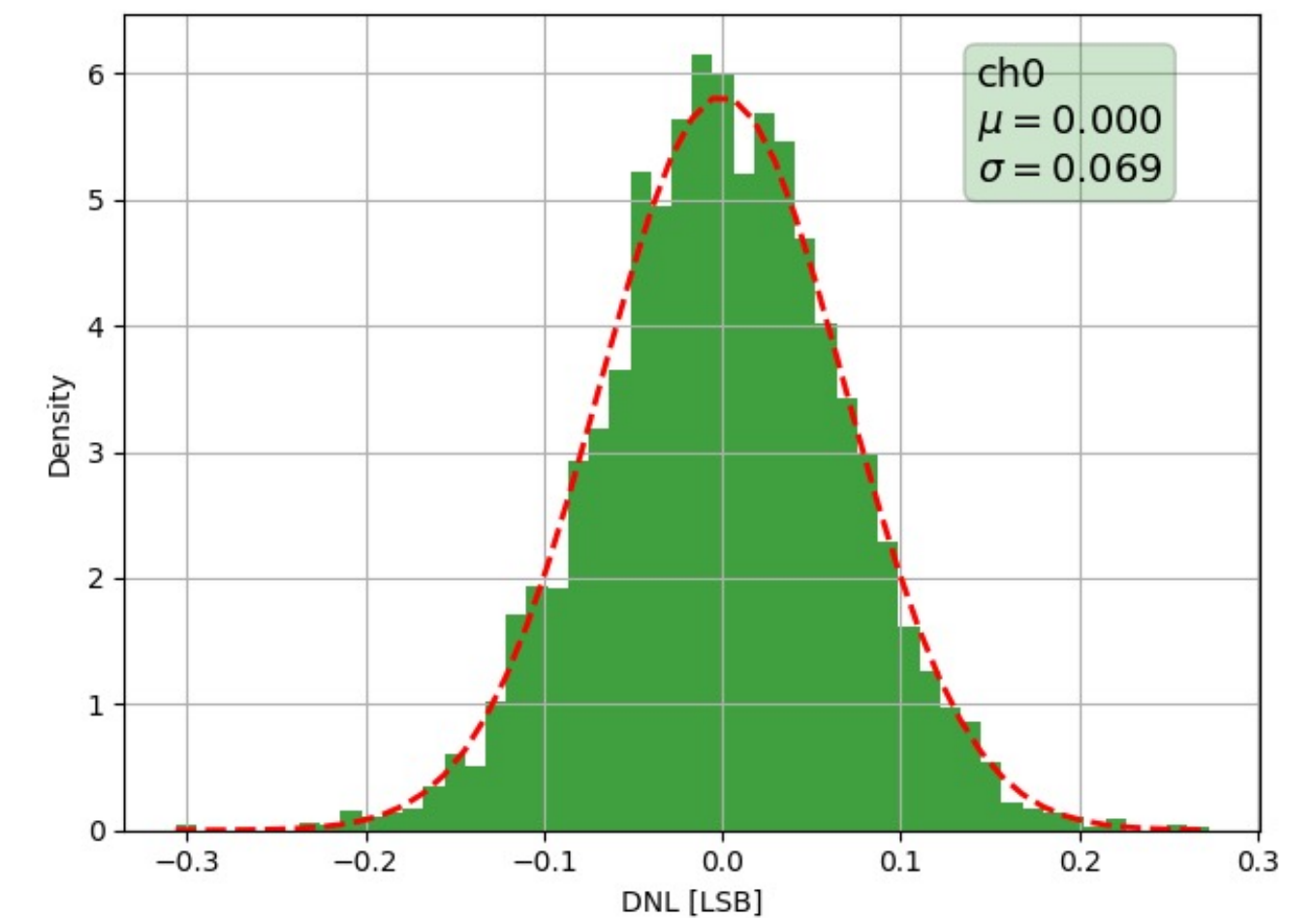
Monitoring parameters

- Dynamic linearity: effective number of bits (ENOB)

  - It's the ratio of the input signal amplitude to the rms sum of all other spectral components

  - It's a measure of the combination of nonlinearity and noise

Sinusoidal Input (147.461kHz; Vp-p 1.4V)

N = 2048
SNDR = 63.51 dB
ENOB = 10.35 bits
SNR = 66.26 dB
SFDR = 72.17 dB
THD = -66.78 dB
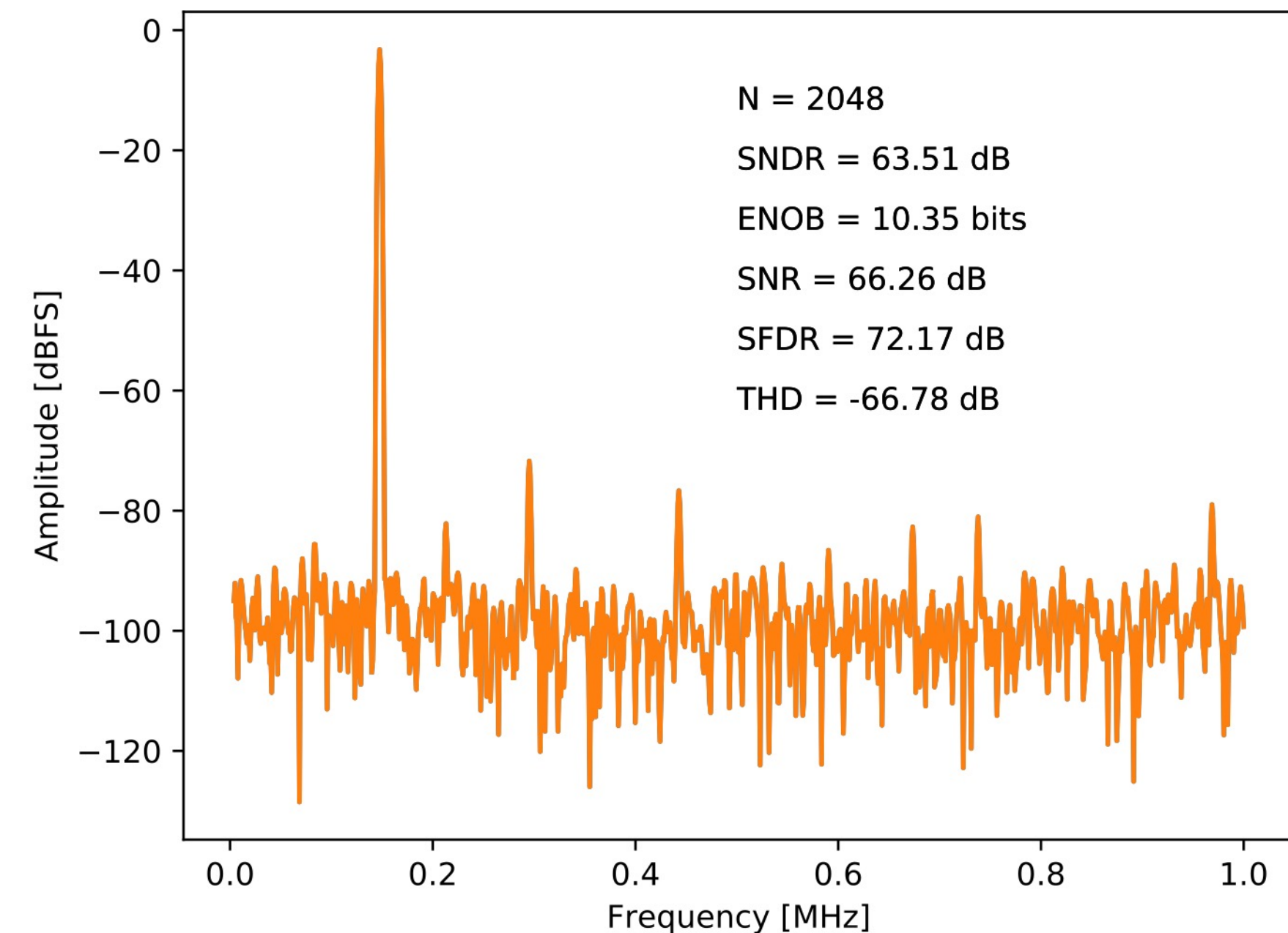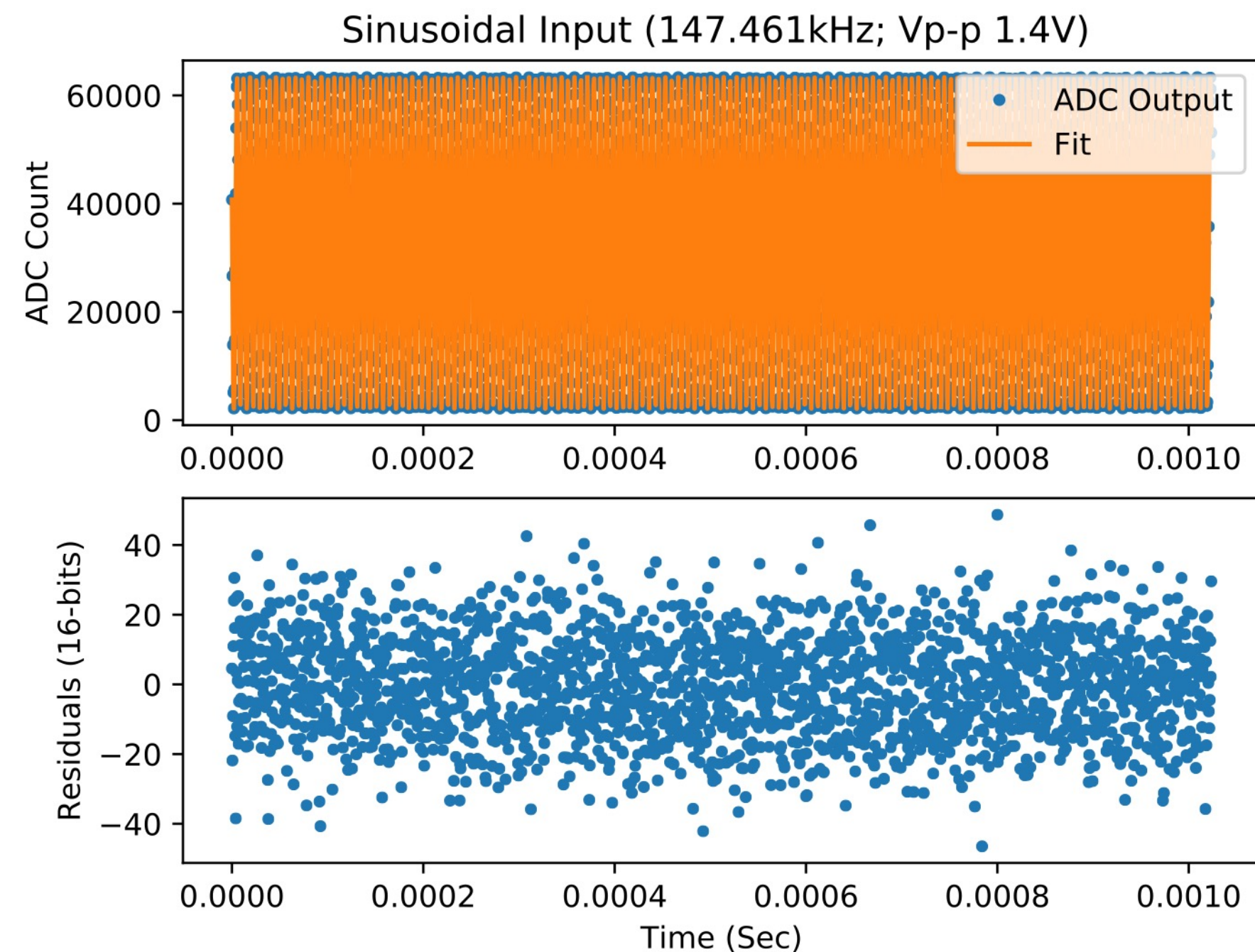
Overview of Basics on Hot-electron effects (HEC) and NMOS lifetime (1)

● In deep submicron NMOS (L<0.25μm) electrons can become "hot" at any temperature, by attaining energy *E>kT*.

● Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \cong 1.3 eV$ resulting in *impact ionization*. Electrons proceed to the drain. The *holes* drift to the substrate. The **substrate current**,

$$I_{sub} = C_1 I_{ds} e^{-\varphi_i / q\lambda E_m} \qquad (1)$$

● A very small fraction of hot electrons exceeds the energy required to create an **interface state** (e.g., an acceptor-like trap), in the Si-SiO$_2$ interface,   for electrons (~4.6*eV* for holes). This causes a change in the transistor characteristics (transconductance, threshold, intrinsic gain). The time required to change any important parameter (the changes in different parameters are correlated) by a specified amount (e.g., gm by -10%) is defined as the **device lifetime**. It can be calculated as,

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it} / q\lambda E_m} \qquad (2)$$

$$\varphi_{it} \geq 3.7 eV$$
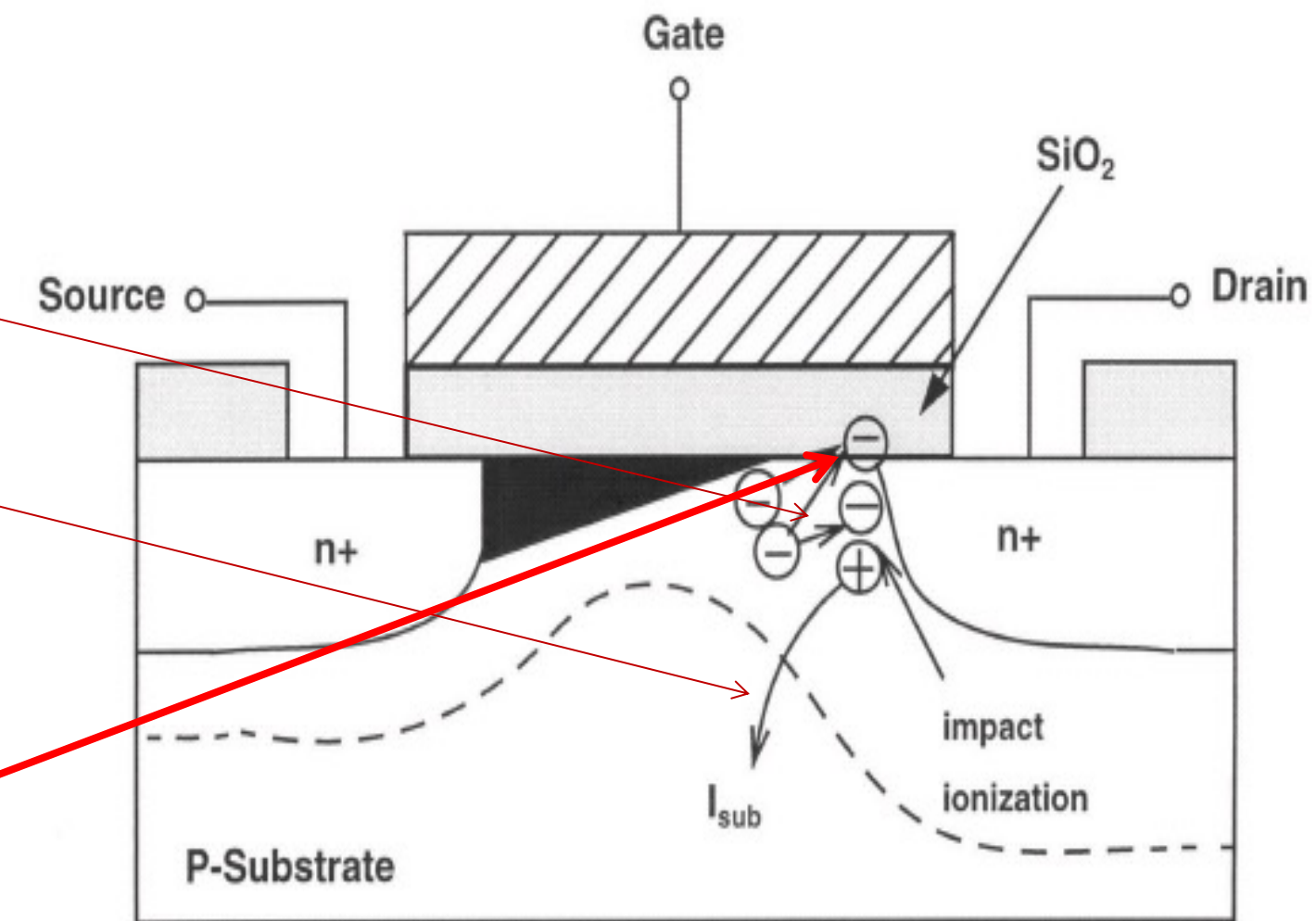
q = electron charge

λ= electron mean free path

E$_m$= electric field
q λ E$_m$= mean hot electron energy

I$_{ds}$= drain-source current
W= channel width
C$_1$, C$_2$ - constants

Id is the total resistive drain current (including that which flows to the bulk) and Ids is just that between drain and source

Overview of Basics on Hot-electron effects (HEC) and NMOS lifetime (2)

•**It has been widely recognized in the literature (e.g., [1] and [2]) that I_{sub} is a monitor for all hot-electron effects and it is the best predictor of device lifetime.**

•The reason that device lifetime or degradation may be predicted from the substrate current I_{sub} is that both observable hot electron effects (electrical and optical) are driven by a common driving force – the channel electric field, or more specifically the maximum channel electric field E_m , which occurs at the drain end of the channel.

•The *substrate current is connected to the lifetime* (defined by any arbitrary but consistent criterion) by the relation {obtained by cancellation of **$q\lambda E_m$** between Eqs, (1) and (2)},

$$\tau = H \frac{1}{\left(I_{ds}/W\right)} \left(\frac{I_{sub}}{I_{ds}}\right)^{-\varphi_{it}/\varphi_i} \qquad (3)$$

• The constant H [As/μm] is a function of the channel length L, the device technology (interface quality, *details of drain doping*, etc.) and the criterion used for definition of the lifetime (e.g., 10% decrease in transconductance, g_m, as used in industry).

Why is the dependence of Lifetime on V_{ds} so strong?

The lifetime is given by,

$$\tau = C_2 \frac{1}{(I_{ds}/W)} e^{\varphi_{it}/\varphi_{he}} \propto \frac{1}{(I_{ds}/W)} e^{\varphi_{it}/\varphi_{he}}$$

Electrons in the MOS channel reach energies well above thermal both at 300K and at 77K . However the **mean electron energy,** $\varphi_{he} = q\lambda E_m \sim 100 meV$, at the electric field in the range $E_m \geq$ 100kV/cm. At 77K it is slightly higher, $\varphi_{he77K}/\varphi_{he300K} \approx 1.06$

Only a tiny fraction of "hot" electrons reaches the much higher energy $\varphi_{it} \approx 3.7eV$ required to create an **interface state**. This makes the exponent in the relation for the lifetime very large,

$$\frac{\varphi_{it}}{\varphi_{he}} = \frac{\varphi_{it}}{q\lambda E_m} \sim 40 \pm 4$$

Since $E_m \propto\sim V_{ds}$, the ratio of lifetimes for two slightly different values of V_{ds} is given by,

$$\ln \frac{\tau_1}{\tau_2} \approx \frac{\varphi_{it}}{\varphi_{he}} \cdot \left[\frac{V_{ds2}}{V_{ds1}} - 1 \right]$$

$$for \; \frac{V_{ds2}}{V_{ds1}} = 1.06 \Rightarrow \frac{\tau_1}{\tau_2} \sim 10$$