DUNE PRR: FD1 TPC Electronics (Cold ASICs + FPGA)

WIB Development and FPGA Procurement

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Outline

[Charge Question: #10]

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Introduction

- WIB development has been described in the support document for FD1 TPC Electronics FDR on September 29, 2022
  - https://edms.cern.ch/document/2782297/
- WIB for ProtoDUNE-I
  - Intel/ALTERA Arria V FPGA 5AGTFD3H3F35I5N
  - 30 WIBs were installed in 6 WIECs to read out 6 APAs for ProtoDUNE-I operation from 2018 to 2020 successfully
- WIB for ProtoDUNE-II HD & VD
  - AMD/Xilinx Zynq UltraScale+ MPSoC XCZU6CG-1FFVB1156E
  - 20 WIBs were installed in 4 WIECs to read out 4 APAs for ProtoDUNE-II-HD in 2022
  - 12 WIBs are being installed in 2 WIECs to read out 2 CRPs for ProtoDUNE-II-VD in 2023
- WIB for DUNE FD1-HD & FD2-VD
  - AMD/Xilinx Zynq UltraScale+ MPSoC XCZU6CG-1FFVB1156E
  - 750 WIBs will be installed in 150 WIECs to read out 150 APAs for FD1-HD
  - 480 WIBs will be installed in 80 WIECs to read out 80 bottom CRPs for FD2-VD

FPGA Selection

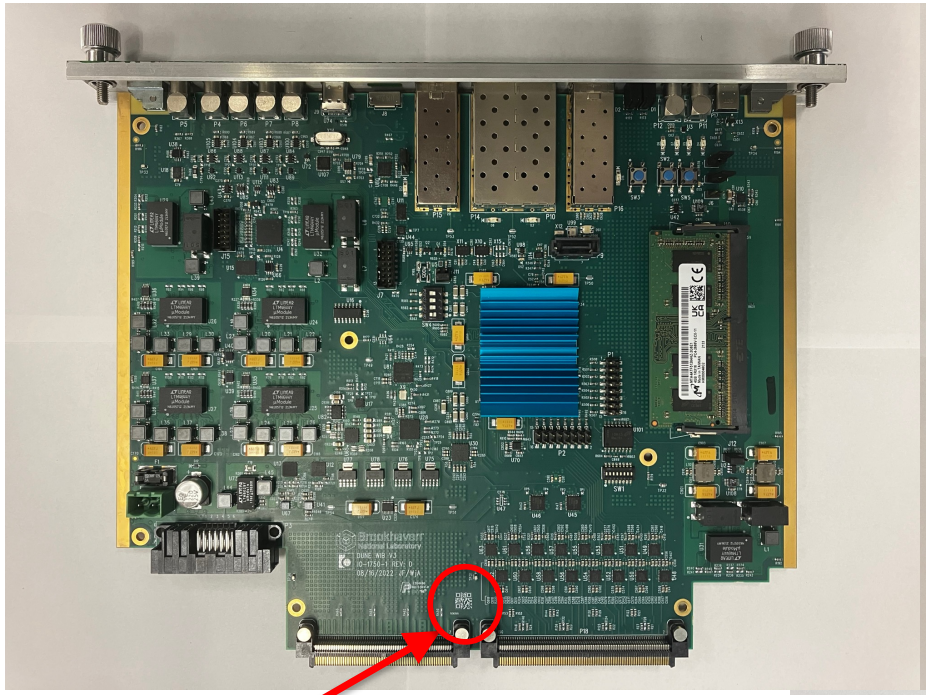
- A market survey was carried out after ProtoDUNE-I construction to identify a proper FPGA for DUNE far detector WIB design
- This was discussed during the DUNE collaboration meeting at CERN in January 2019
  - https://indico.fnal.gov/event/16764/contributions/39509/attachments/24693/30763/BNLCEUpdate.20190129.pdf
- The MPSoC XCZU6CG offers a cost effective alternative, with additional features, e.g. ARM processor, TCP/IP etc.

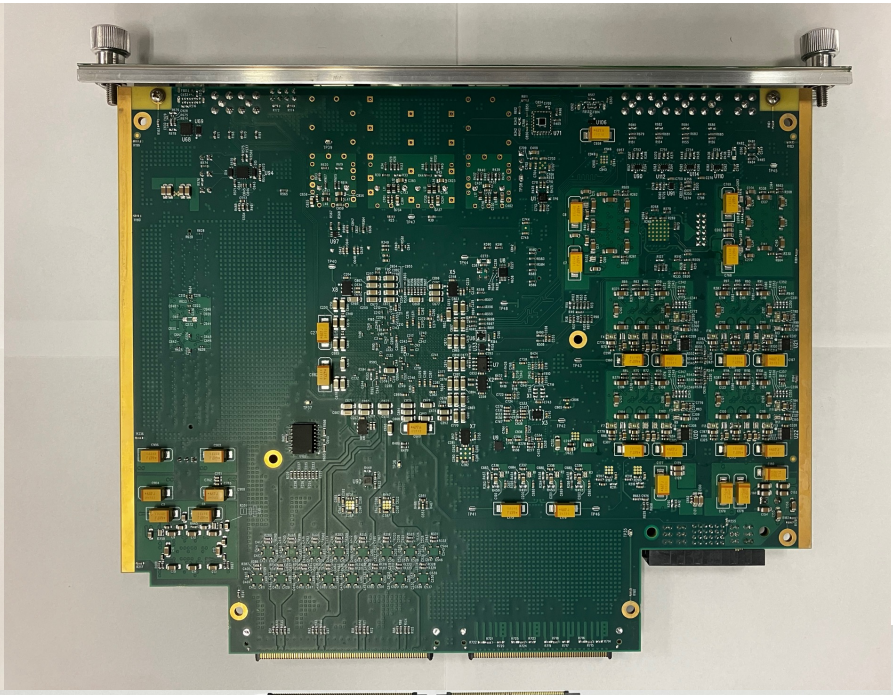
	WIB	WIB	WIB	WIB	WIB	WIB	WIB
Manufactures	Intel/Altera	Intel/Altera	Intel/Altera	Xilinx	Xilinx	Xilinx	Xilinx
Series	Arria V	Arria 10 GX	Arria 10 GX	Kintex UltraScale	Kintex UltrScale+	Kintex UltrScale+	Zynq UltraScale+
FPGA	5AGTFD3H3F35I5N	10AX032H4F34E3SG	10AX048H4F34E3SG	XCKU040-1FFVA1156I	XCKU9P-1FFVE900E	XCKU11P-1FFVA1156E	XCZU6CG-1FFVB1156E
LEs (K)	362	320	480	530	600	653	469
M10K/M20K Memory Blocks	17.26 (M10K)	17.82 (M20K)	28.62 (M20K)	-	-	-	-
MLAB Memory (Mb)	2	2.7	4.2	-	-	-	-
Max. Distributed RAM (Mb)	-	-	-	7	8.8	9.1	6.9
Total Block RAM(Mb)	-	-	-	21	32.1	21.1	25.1
UltraRAM(Mb)	-	-	-	-	0	22.5	-
DSP	1045	985	1368	1920	2520	2928	1973
GPIO(3.3V/HR/HD +	544 + 0	48 + 336	48 + 444	104 + 416	96 + 208	48 + 416	120 + 208 + 214
XCVR	24 (10 Gb/s)	24(17.4 Gb/s)	24(17.4 Gb/s)	20 (12.5 Gb/s)	28 (12.5 Gb/s)	20 (12.5 Gb/s) + 8 (25 Gb/s)	24 (12.5 Gb/s)
Size (mmxmm)	35 x35 (F1152)	35 x35 (F1152)	35 x35 (F1152)	35 x35 (A1156)	31x31 (E900)	35 x35 (A1156)	35 x35 (B1156)
Price($)	1360.6 for 744-1000 pcs quote	$1016.00 for 100-1000 pcs	$1550.00 for 100-1000 pcs	$1010.14 for 51-300 pcs quote and $769.45 for 301-1000 pcs	$1000.04 for 51-300 pcs quote and $760.84 for 301-1000 pcs	$1410.97 for 1-499 pcs and $1074.57 for 500-1000 pcs	$1050.88 for 36-249 pcs quote and $799.77 for 250-1000 pcs

WIB Design Evolution

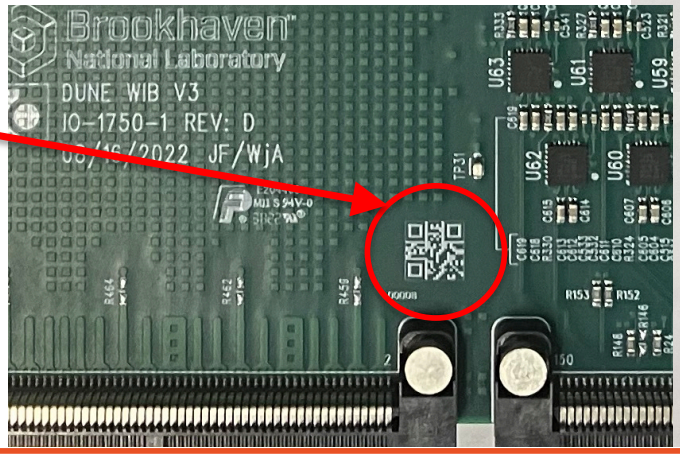
- The WIB with Zynq UltraScale+ MPSoC ZU6CG has been developed since 2019
- Prototype design (WIBv2: IO-1750-1/-1A) in 2019/2020 has been tested extensively
  - Bench test and integration test at BNL
  - Firmware development at Florida and Penn
  - Integration test with ICEBERG at Fermilab
- Final design (WIBv3: IO-1750-1B/-1C/-1D) in 2022 for APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN
  - Design changes from WIBv2 to WIBv3 described in the FDR support document (https://edms.cern.ch/document/2782297/)
  - Minor updates of WIBv3 to address few cosmetic issues
    - IO-1750-1C: Micro-USB to USB-C; MicroSD socket and location
    - IO-1750-1D: QR code; current monitoring
- FPGA firmware is fully compatible among WIBv3 boards

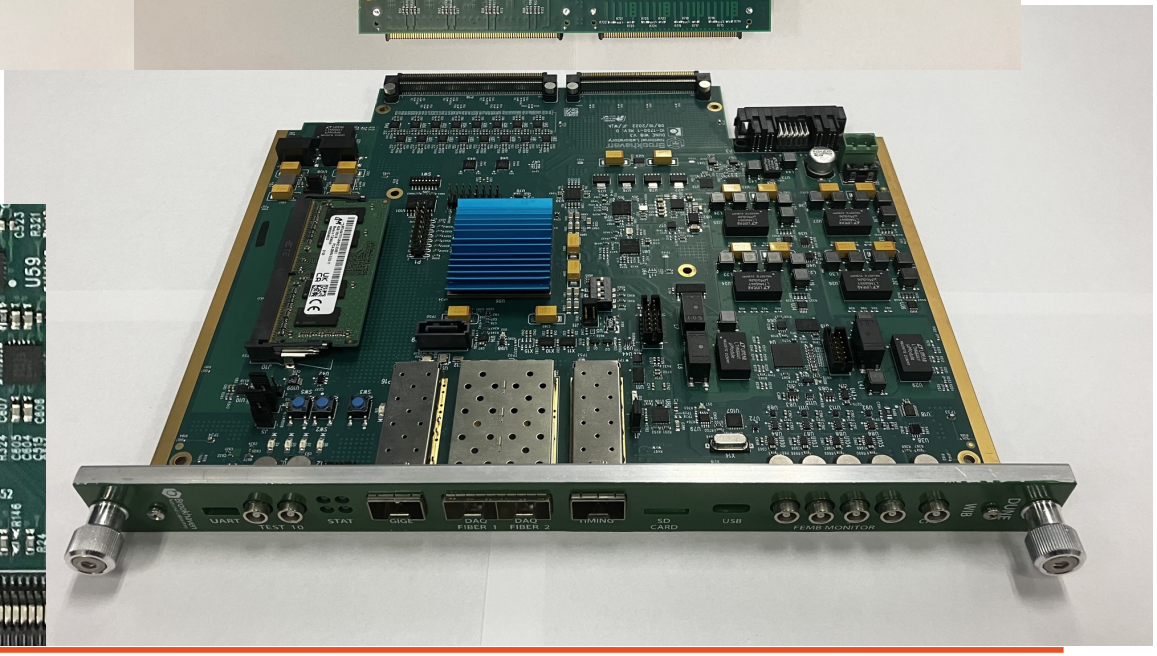
WIBv3 IO-1750-1D





QR code





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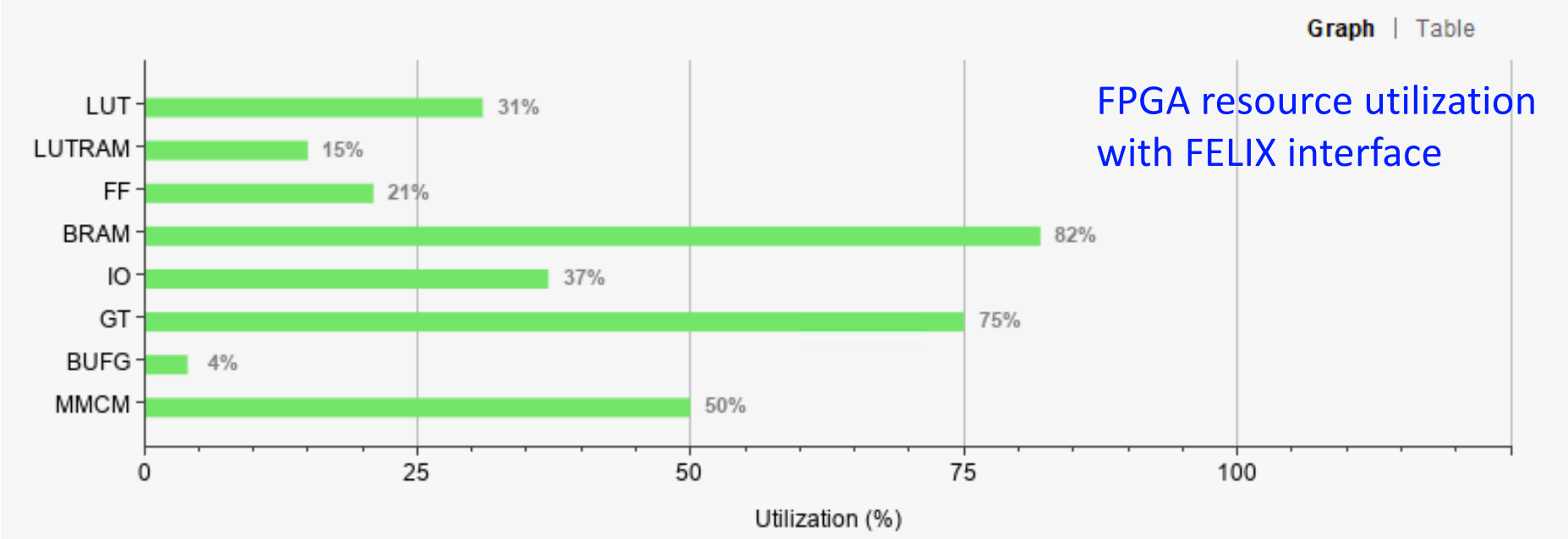
WIB Operational Experience

- WIBv3 has been used extensively for APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN
  - 5 WIBs for APA cold box test
  - 20 WIBs for ProtoDUNE-II-HD
  - 6 WIBs for CRP cold box test
  - 12 WIBs for ProtoDUNE-II-VD
  - Spare WIBs for VST
- ProtoDUNE-II-HD has been read out by WIBv3 through FELIX successfully since 2022
  - APA cold box test has been read out by WIBv3 through FELIX since 2022
  - CRP cold box test has been read out by WIBv3 through FELIX since 2022
  - VST is being used to test WIBv3 Ethernet readout, later to be deployed for ProtoDUNE-II-HD/VD
  - Please see Roger's talk for more details

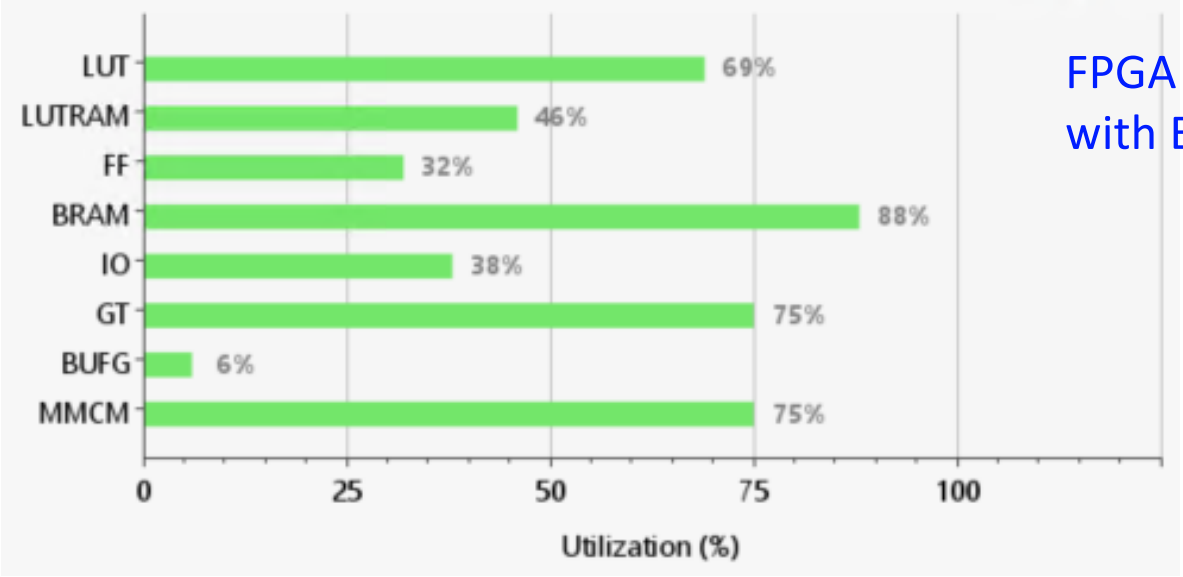
Technical Justification for CD-3A Procurement (1)

- WIB firmware used in ProtoDUNE-II so far has the interface for the FELIX readout, which has been working reliably since 2022
  - The FPGA resource utilization of WIB firmware is quite reasonable, with < 35% LUT usage
  - The usage of BRAM is relatively high, which is due to the ILA cores for debug purposes in the current firmware build



Technical Justification for CD-3A Procurement (2)

- The DUNE DAQ system is migrating to Ethernet based readout in 2023. A preliminary build of the WIB firmware with Ethernet interface is being tested
  - The FPGA resource utilization of WIB firmware is quite reasonable, with < 70% LUT usage
  - The LUT usage can be further optimized with improved design of the data alignment module if necessary
  - The usage of BRAM is relatively high, which is due to the ILA cores for debug purposes in the current firmware build
- WIB FPGA ZU6CG has sufficient resources for the production needs of DUNE far detector cold electronics readout system.



FPGA resource utilization with Ethernet interface

FPGA Procurement Plan

- The quote of XCZU6CG-1FFVB1156E was updated in early 2023 by Avnet
  - Step 2 price of $1,322.31 each (up to 125 pieces)
  - Step 3 price of $444.92 each (after 125 pieces)
  - 23 pieces will be consumed in Step 2 before unit price moves to Step 3
- For CD-3A procurement for FD1-HD, a total 800 WIB FPGAs will be ordered
  - The total cost will be 23 x $1,322.31 + 777 x $444.92 = $376,115.97
- The order was processed at BNL with expected long lead time
  - Initial delivery date is December 2023, has been updated to August 2023

Charge Question

- 10. Has the current design of the Warm Interface Board (WIB) been sufficiently tested and exercised to be confident that a particular FPGA can be procured without risk?
  - Yes
  - WIBv3 has been used in the APA/CRP cold box tests and ProtoDUNE-II HD/VD at CERN since 2022
  - Firmware builds with both FELIX and Ethernet interfaces have confirmed the FPGA ZU6CG has sufficient resources
  - FPGAs can be procured to meet production needs of DUNE FD1-HD cold electronics readout system with no identified risk