DUNE PRR: FD1 TPC Electronics (Cold ASICs+FPGA)

ASIC QC Test Stand and ESD Discussion

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Brookhaven National Laboratory, Michigan State University

05/08/2023

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Content

- **Charge Questions**
- DAT Design and Status
- RTS Status
  - R&D is conducted by MSU
- ESD Discussion
- Summary

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Charge Questions

7. Has the handling procedure of ASICs to minimize ESD been defined and documented?

   Yes. Please refer to EDMS#2782612.

8. Have the designs and production of the ASICs QC stations been completed?

   DAT and RTS status is presented.

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Content

- Charge Questions
- **DAT Design and Status**
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Hardware: DUNE ASIC Test Board (DAT)

- DUNE ASIC Test (DAT) Board

  - Unified ASIC test board for LArASIC, ColdADC and COLDATA QC

    - Compatible power and data interface with WIB. It acts as exactly as a FEMB to WIB
    - Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU new RTS
    - Aim for DUNE-FD1 & FD2 ASIC QC carried out in several test sites

  - A single big board solution with ASIC socket mezzanines

    - ASIC socket suffers mechanical degradation through thermal cycling
    - More commercial semiconductor devices have been identified for cryogenic operation
      - Such as Analog MUX: SN74LV4051, Power Monitoring Chip: INA226, I2C Bridge device: PCA9306, DAC: AD5675ARUZ

  - Unified ASICs and FEMB QC with the same software suite

    - Can benefit directly from the WIB, back-end DAQ, **analysis software developments**
    - Some extra software effort for ASIC QC can be implemented as a widget to the available software

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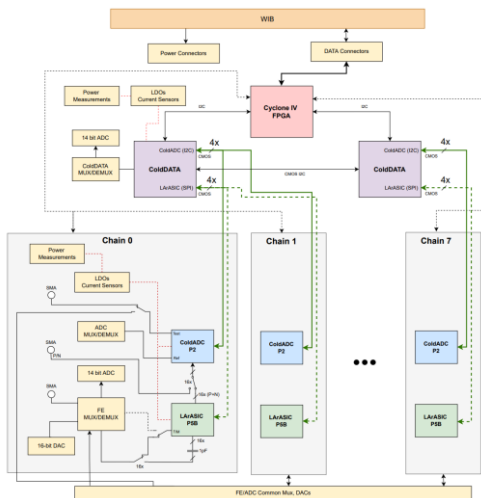
Power Measurement

Power Rail	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA	V /V	I /mA
	COLDATA#1								COLDATA#2							
VDDA	1.193	9.3							1.193	9.1						
VDD_LArASIC	1.786	0.0							1.783	0.0						
VDDCORE	1.089	9.2							1.088	9.2						
VDDD	1.089	19.5							1.086	19.5						
VDDIO	2.234	66.9							2.228	67.6						
	ColdADC #1		ColdADC #2		ColdADC #3		ColdADC #4		ColdADC #5		ColdADC #6		ColdADC #7		ColdADC #8	
VDDA2P5	2.190	132.6	2.185	133.0	2.184	132.3	2.181	134.6	2.184	125.0	2.184	132.8	2.186	121.1	2.189	135.4
VDDD2P5	2.206	5.2	2.206	5.3	2.206	5.3	2.206	5.3	2.210	5.0	2.211	5.1	2.211	5.2	2.211	5.2
VDDIO	2.205	17.2	2.206	17.7	2.205	17.5	2.205	15.6	2.210	17.5	2.209	16.4	2.209	17.1	2.210	14.7
VDDD1P2	1.095	1.5	1.095	1.4	1.094	1.5	1.094	1.5	1.094	1.4	1.098	1.4	1.099	1.4	1.099	1.5
	LArASIC #1		LArASIC #2		LArASIC #3		LArASIC #4		LArASIC #5		LArASIC #6		LArASIC #7		LArASIC #8	
VDDA	1.778	21.5	1.778	21.4	1.776	21.7	1.776	20.5	1.771	21.4	1.771	21.5	1.773	21.4	1.771	21.5
VDDO	1.781	0.0	1.780	0.0	1.780	0.0	1.781	0.0	1.776	0.0	1.776	0.0	1.776	655.3	1.775	0.0
VDDP	1.776	32.5	1.775	32.6	1.775	32.4	1.774	32.2	1.769	32.2	1.770	32.3	1.769	32.3	1.771	32.4

➢ Total 66 power rails are measured independently by 66 INA226 chips
- ▪ Each COLDATA: 5 power rails
- ▪ Each ColdADC: 4 power rails
- ▪ Each LArASIC: 3 power rails

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Monitoring through COTS ADC

- COLDATA
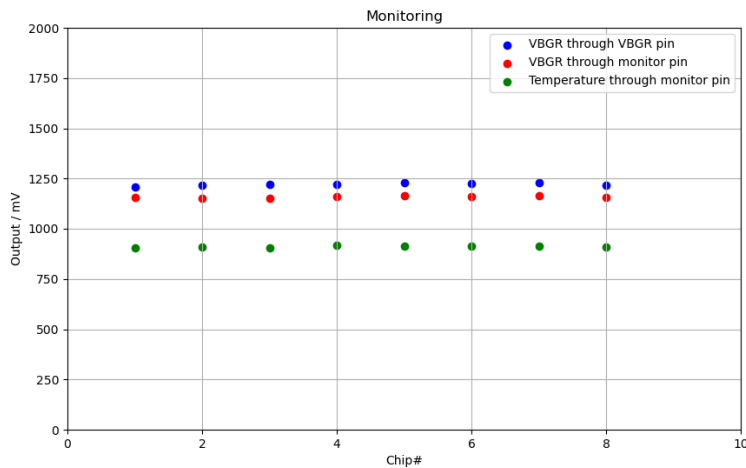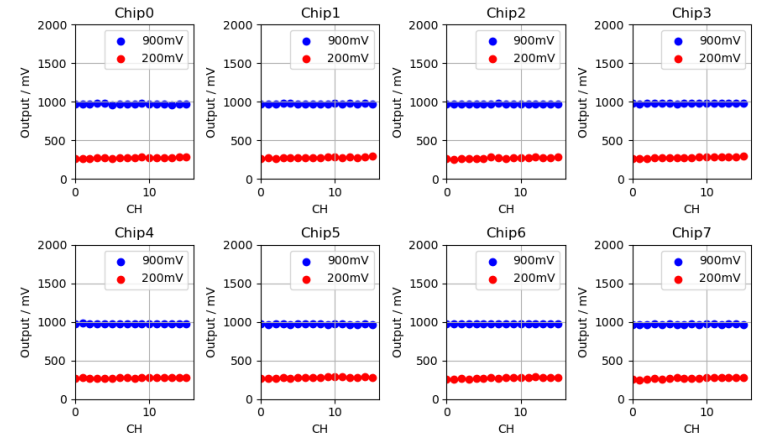 - VCEXT, VDDIO, VDDCORE, VDDD, ATO, LOCK
- LArASIC
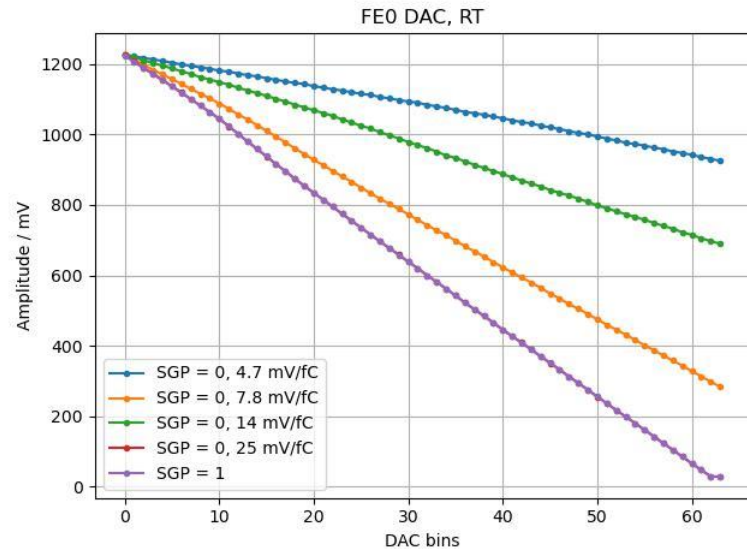 - VBGR (1.18V), Temperature, inner-DAC, LArASIC output
- ColdADC
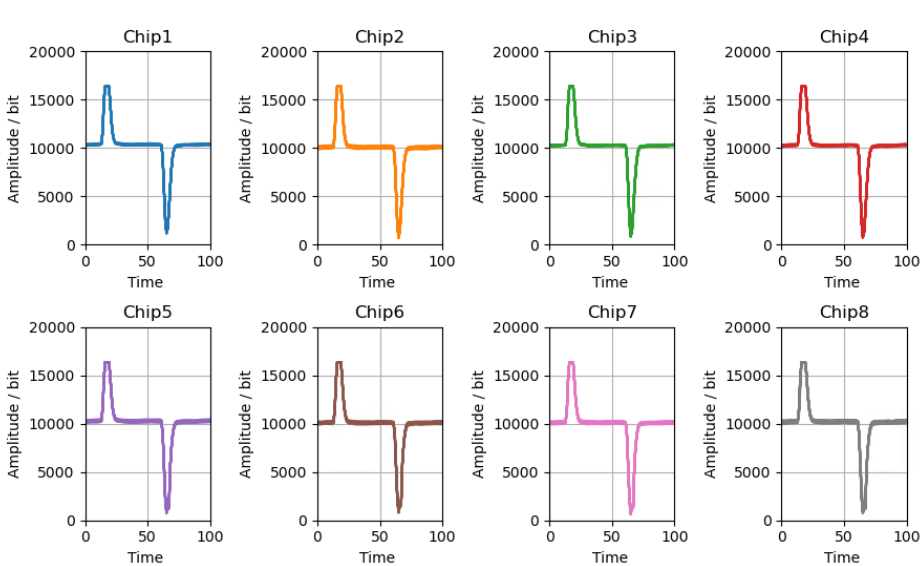 - VOLTAGE_MONITOR, CURRENT_MONITOR, AUX_VOLTAGE, VREFP, VREFN, VCMI, VCMO, AUX_ISINK, AUX_ISOURCE

FE Baseline through monitoring pin (note: monitor output waveform is available though not implemented yet)

Monitoring (FE Bandgap Reference & Temperature)

Each LArASIC 6-bit DAC will be measured independently

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LArASIC Pulse Response

Single-ended Interface Between LArASIC & ColdADC
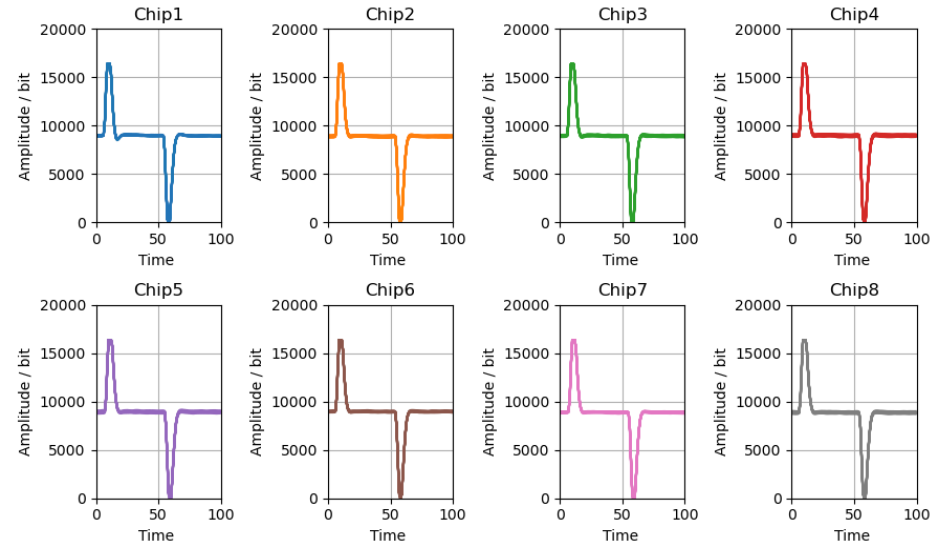
Differential Interface Between LArASIC & ColdADC

➢ ## DAT is fully compatible with WIB firmware

- Unify ASIC and FEMB QC test stand
- Benefit directly from FEMB QC scripts development
- Multiple onboard calibration can perform all LArASIC QC items
- Onboard 16-bit DAC can characterize ColdADC static performance (INL/DNL)
- ColdADC dynamic performance (ENOB) can be done with external signal generator (SMA interface)
- All COLDATA QC items can be performed with DAT revision

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LArASIC QC Items

Test Item	Description	Reference chips	Chips for QC	DAT doable
Power Consumption	Measure the power consumption on the three rails of LArASIC (VDDP, VDDA, VDDO), for each of six configurations (two baseline references: 200 mV and 900 mV; three configurations of the output buffer: bypassed, single ended, differential)	Required	Required	Yes
Power Cycling	a number (>5) power on/off cycles, measure the pulse response with a certain configuration (e.g., 14mV/fC, gain, 2.0us peak time, 200mV baseline, 500pA leakage current)	Required	Required	Yes
Register configuration	check through SPI interface for register configuration W/R	Required	Required	Yes
Bandgap	Measure the bandgap reference voltage	Required	Required	Yes
Temperature sensor	Measure the voltage of embedded temperature sensor	Required	Required	Yes
Channel response monitoring	Check response of each channel through the monitor pin	Required	Required	Yes
Internal DAC measurement	measure INL/DNL of 6-bit DAC (4 ranges for 4 gains)	Required	subset	Yes
baseline measurement through monitoring pin	Measure baseline through the monitoring pin (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	Yes
baseline measurement	Measure baseline with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	Yes
Noise measurement	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents). A reference capacitive load of ~150 pF at the inputs.	Required	subset	Yes
Calibration with internal-DAC	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	subset	Yes
Calibration with external precise source	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	No	Yes
Crosstalk [1]	Measure with ColdADC (1 gains x 4 peak times)	No	No	no
Internal calibration capacitor measurement	Measure the capacitance of the calibration capacitor	Required	No	Yes

[1] crosstalk test should be done on FEMB only

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ColdADC QC Items Recommendation

| Item	Description	FEMB doable	DAT doable
Power consumption and power cycling	Voltage and current of each power rails should be recorded	No	Yes
I2C Write/Read	Check all default register values	Yes	Yes
Chip reset		Yes	Yes
Reference voltages measurement	VCMI, VCMO, VREFN, VREFN	Yes	Yes
Pulse 16 channels	Either at once or individually automatically. Needs external signal generator to get INL/DNL, ENOB, DC noise	No	Yes for INL/DNL No for ENOB [1] Yes for DC noise
Overflow checkout	Needs external signal generator	No	Yes
Coupled with LArASIC	Full-chain test. Needs automatically switch sources (LArASIC or signal generator) for ADC inputs	Yes	Yes
16-bit mode	COLDATA doesn't support 16-bit mode	No	No, 14-bit
Ring oscillator	Measure the frequency	No	Yes
UART	Not used in FEMB design	No	Yes

[1] It is doable with external ultra-low distortion function generator and extra coaxial cable connection

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COLDATA QC Items Recommendation

Item	Description	FEMB doable	DAT doable
Power consumption and power cycling	Voltage and current of each power rails should be recorded	No	Yes
I2C Write/Read	Check all default register values	Yes	Yes
Fast commands	Verify all Fast Commands	Yes	Yes
PLL, 8b10b Encoder, Serializer, & Line Driver		Yes	Yes
Data Capture, Frame Formation, Switchyard		Yes	Yes
General Purpose I/O		Yes	Yes
Master/Slave operation	I2C LVDS, I2C CMOS and ADC I2C addressing	no	Yes
EFUSE	Add EFUSE programming into DAT revision	no	Yes

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DAT Cold Testing

- A stainless-steel box for EMI shielding and LN2 containment, with DAT board inside
  - The outer plywood box with foam provides thermal insulation
  - This box is intended for FEMB QC in future
    - It has the capability to hold multiple FEMBs (CE boxes)
  - Got ESR approval for the cold operation
- DAT 1st run at cold
  - All commercial components survive (we did cold screening to choose cryogenic-eligible components)
  - Reliable communication between DAT and WIB
  - Unreliable connection between chips and sockets
    - Cooldown may cause misalignment between chip pins to socket pads (sometimes poking the chips slightly can fix it sometimes not)
    - Observed channel response
- 2nd cold run with chip mezzanines is scheduled

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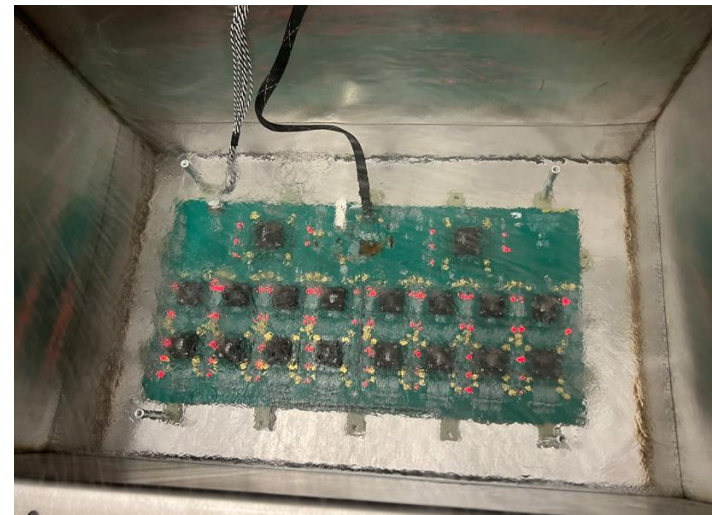
DAT Revision is Under Review

- 1st DAT satisfies 3-ASIC QC requirement, a minor revision is required for

  - Fix some FPGA IOs assignment issue

  - Add support of COLDATA EFUSE programming

  - Power measurement for COLDATA chips

    - SCL and SDA lines are going into the wrong pins on INA226s

  - V_{REF} of Two COTS ADCs for COLDATA monitoring should connect to Reference

- Revision of schematics and layout are done, waiting for approval

  - PCB fabrication was hold until we fully characterize the current DAC capability for 3-ASIC QC testing.

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Content

- Charge Questions
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- **RTS Status**
  - R&D is conducted by MSU
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Hardware: DUNE Robotic Testing Station
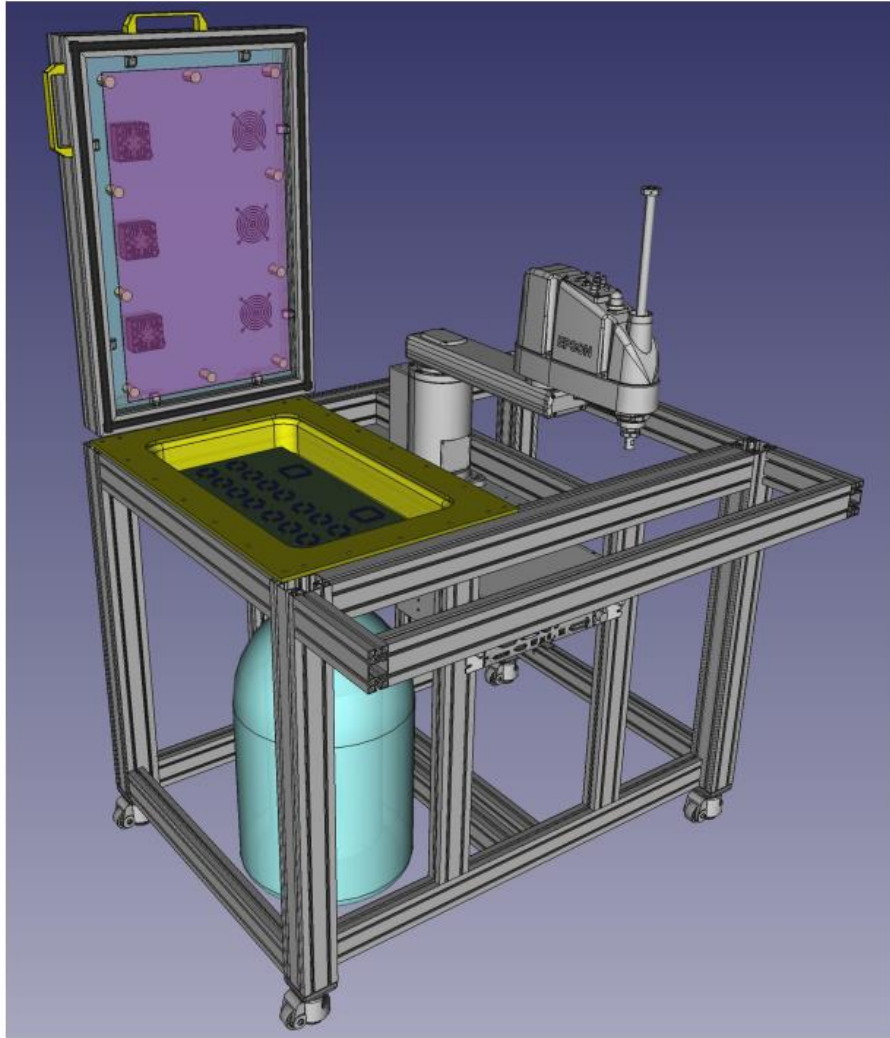
The RTS comprises:

A commercial robot to pick and place the ASICs from trays to test sockets

Test chambers that support the testing hardware.

Test chambers are also Faraday enclosures.

A cryogenics system that can fill and drain the test chambers.

An aluminum strut framework to hold this all together.

An upper level to the strut framework to provide a safety enclosure with access doors (not shown).

RTS system has two test chambers, only one is shown here.

RTS is designed by Dean Shooltz, Kendall Mahn, Carl Bromberg from Michigan State University

"Foam insulated kitchen sink"
...*quote from FNAL safety review*

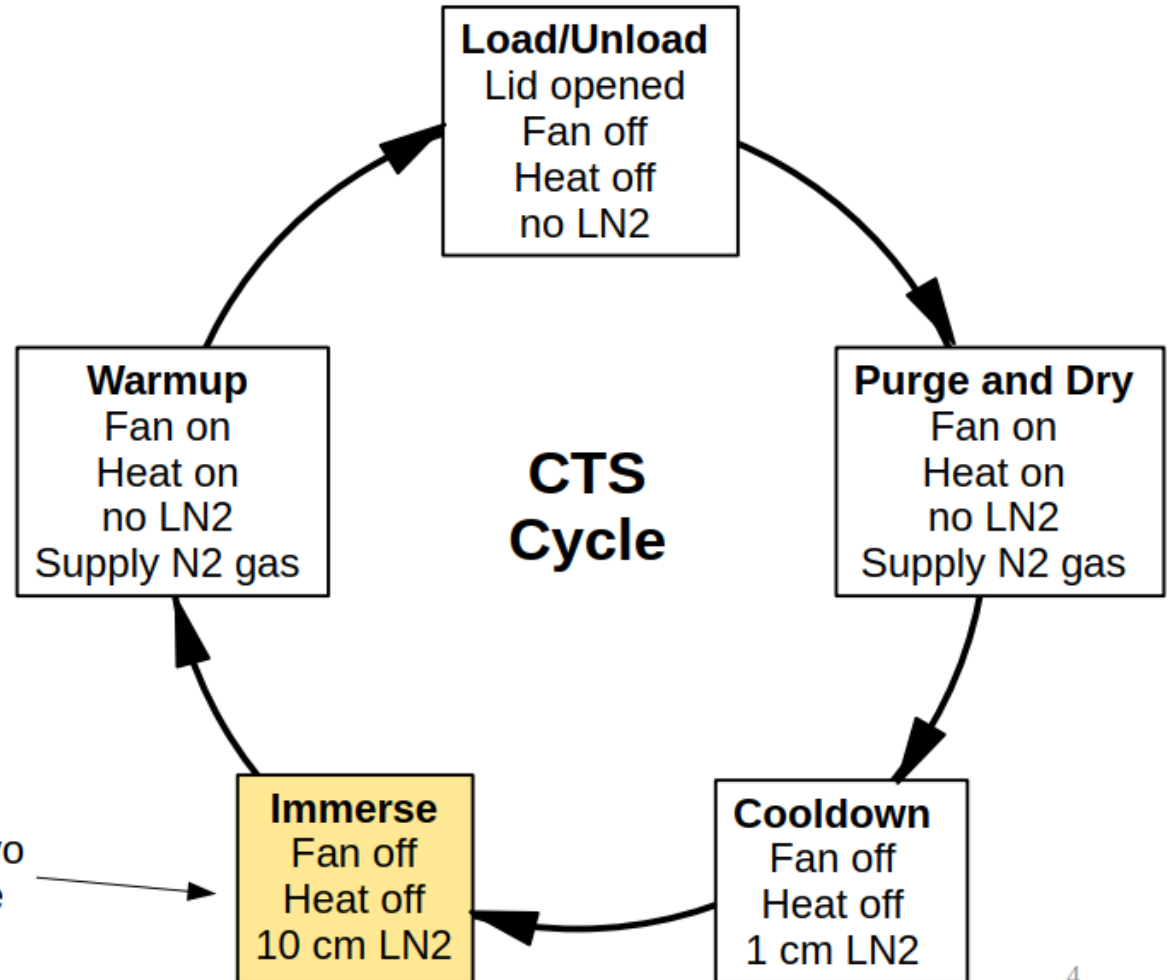Fans/heaters

DAT board

LN2 Dewar

Cryo Testing Station

– Cycle time is roughly one hour (plus electronics testing time)
– Fans and heaters are located inside test chamber headspace
– Slight pressure in Dewar used to raise LN2 into test chamber
– Relieve pressure and LN drains back into Dewar
– CTS cycle keeps DUT dry throughout the cycle

Load/Unload
Lid opened
Fan off
Heat off
no LN2

Purge and Dry
Fan on
Heat on
no LN2
Supply N2 gas

CTS Cycle

Warmup
Fan on
Heat on
no LN2
Supply N2 gas

Cooldown
Fan off
Heat off
1 cm LN2

Perform cryo testing here

Immerse
Fan off
Heat off
10 cm LN2

5/2/23

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Robotic ASIC handling

Camera-guided ASIC positioning is operating near the limit of the robot positioning (~ +/- 15 um)

Dummy ASICs with internal daisy chain connections allow for testing the robot chip handling with electrical validation of the ASIC:Socket interface

A simple readout system checks all ASIC connections (128 pins)

Interleaved daisy chains let us detect pin-pin shorts (can monitor half of all positions)
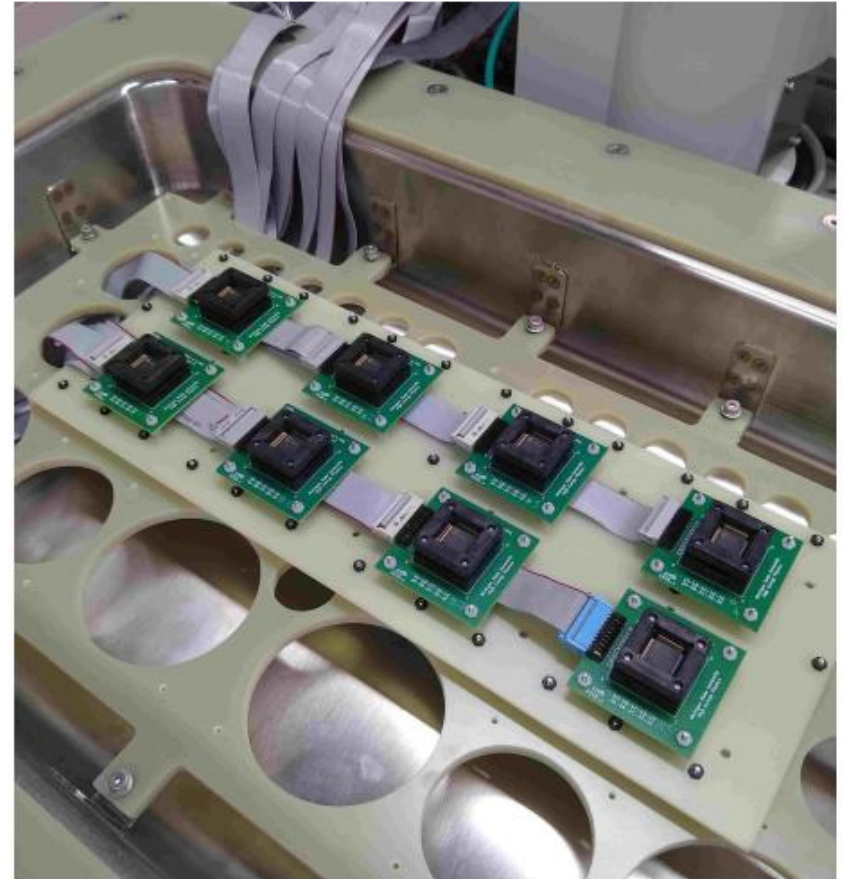

Results so far:
- 32 batches of 8 sockets reloaded. 256 total RTS socket load cycles measured.
- Contact resistance is ~ 30 milliohms (spec is 50 milliohm) (new sockets).
- All chains daisy chains conduct
- Zero short circuits found between the interleaved daisy chains.
- 256/256 successful socket loads (easy to do more)
- Hands-off operation: we only pushed a button to start each cycle.

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Video demos

A timelapse of the RTS swapping a batch of 8 chips in the sockets in the current prototype setup
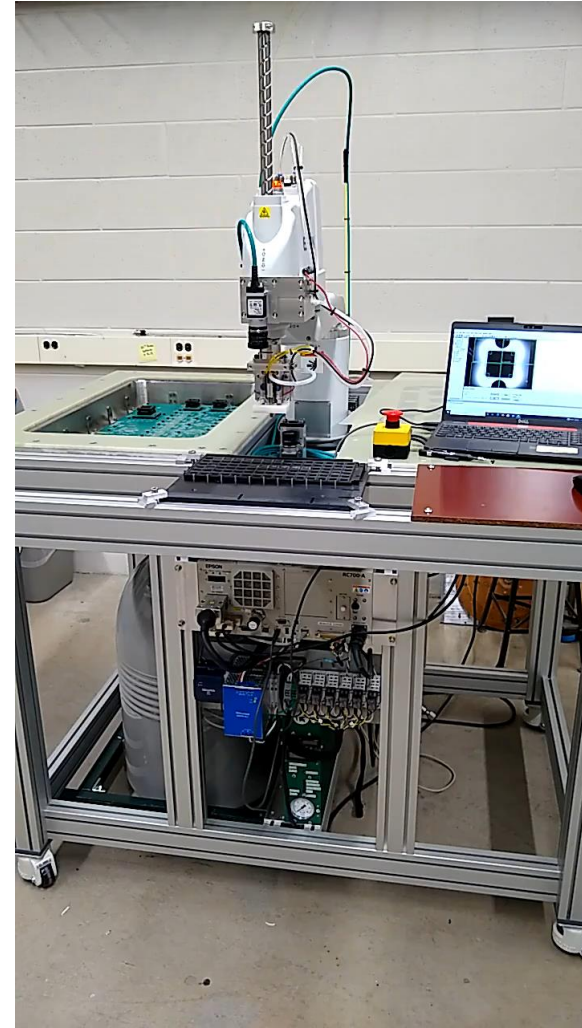
The motions of the RTS robot when moving chips from tray to chamber and back

RTS Current Status and Lead Time to Fully Operational Prototype

Cryogenics
- – First Cryo Cycle of unpopulated DAT board went well
- – Commercial sink warped slightly during welding (puddles); repair in process
- – Chamber lid design completed, expected to be operational by end of May

Robotic ASIC handling is performing well
- – Robust detection of ASIC positions; able to align with robot coordinates
- – 256/256 successful robotic socket loads with electrical validation
    (very easy to do more)
- – No chips damaged, no operator interventions were required

Down-facing camera
- – For ASIC identification, possibly also error detection/handling information
- – Mounted to robot, still need to set up image processing
- – Expected to be ready by end of May.

RTS prototype can be ready to support automated ASIC handling and cryo cycling approximately at the **end of May**.

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Content

- Charge Questions
- DAT Design and Status
- RTS Status
- **ESD Discussion**
  - Charge Question: Has the handling procedure of ASICs to minimize ESD been defined and documented?
- Summary

LBNF/DUNE-US Electrostatic Discharge control for TPC electronics

- Document number: EDMS#2782612

  - In DUNE, ESD can damage any of the electronics components mounted on the FEMBs, WIECs, the bias voltage supplies, or the power supplies.

    - **To avoid this type of damage, devices must be given continuous ESD protection, as outlined in** EDMS#2782612

    - Appropriate preventive measures must be taken during assembly, testing, installation, and shipping of all detector components provided by the TPC electronics consortium

      - These measures include using appropriate ESD-safe packing materials, appropriate clothing and gloves, wearing conducting wrist or foot straps to prevent charges from accumulating on workers' bodies, anti-static mats to conduct harmful electric charges away from the work area, and humidity control. All laboratories with detector components provided by the TPC electronics consortium will implement these measures, including SURF.

    - All personnel must be trained to take the appropriate preventive measures.

      - ESD monitor is highly recommended

LBNF LONG-BASELINE NEUTRINO FACILITY DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT		STANDARD
Title: LBNF DUNE Prevention and Control of Electrostatic Discharge (ESD)		
Author(s): James Mateyack	Approved: Kevin Fahey	Page: 1 of 40
Document ID: 2266860	Version: 0	Version Date: 26May2022

TPC electronics consortium comply with DUNE STANDARD

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ESD protection for ASICs / CE boards

- **Keep ASICs / CE boards (FEMB, WIB, PTC, etc.) and everything that comes in close proximity to them at ESD ground potential**.

  - Any person handling ASICs / CE boards must be grounded either with a wrist strap or ESD protective footwear, used in conjunction with a conductive or static dissipative floor or floor mat

  - The work surface where ASICs / CE boards are placed for handing, processing, testing, and so forth, must be made of static dissipative material and be grounded to ESD ground.

  - All insulator materials either must be removed from the work area or they must be neutralized with an ionizer.

  - Static generating clothes should be covered up with an ESD protective smock.

  - When ASICs / CE boards are being stored, transferred between operations or workstations, or shipped, they must be maintained in a Faraday shield container whose inside surface (touching the ASICs) is static dissipative.
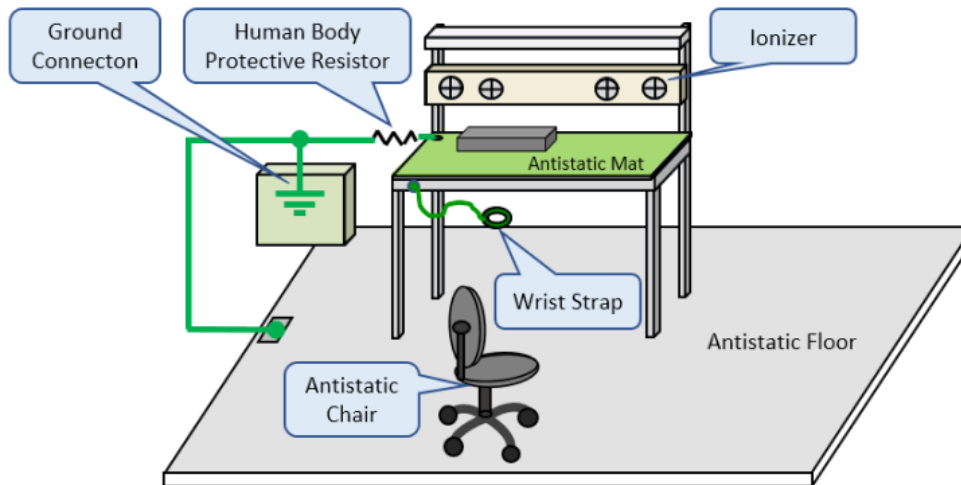
Standard ANSI/ESD S6.1 recommends

1. Grounding all components of the workstation and personnel to the same electrical ground point
2. Connecting the common point ground to the equipment grounding conductor or the third wire electrical ground connection

Any work on DUNE ASICs (installation in sockets, inspection, testing, etc.) must be performed only at ESD-safe workstation designed according to the above guidelines. The work must be performed by trained personnel.

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ESD Protected Area in Electronic circuit test

In the DUNE experiment, there are more than 100 k ASIC chips need to be tested. The ESD Monitors are used to constantly test the connection of the person, the wristband and the coiled cord to help ensure that people remain grounded.

To minimize the chance of damaging ESD sensitive devices, an ESD protected area, which is an area that is equipped with the ESD control items, is recommended to used as a standard test platform.

A protected area is also referred to a "static-safe" area, a permanent workstation within room or an entire factory. The main component include:

1 Bench Top Ionisers	13 Data Acquisition
2 ESD Packaging Containers	14 PCB Storage
3 Earth Bonding Point Bar	15 Signs and Labels
4 ESD Testers and Monitors	16 Floor Marking Tape
5 ESD tape	17 Floor Mats
6 Menda Probes	18 Wrist Straps
7 Menda Dispensing Bottles	19 Foot Grounders
8 Dissipative Worksurface Mats	20 Static Control Garments
9 Surface Resistance Meters	21 Floor Maintenance
10 Grounding Cords	22 Waste Bins and Liners
11 Overhead Ionisers	23 Document Handling
12 Shielding Bags	24 Floor Tiles
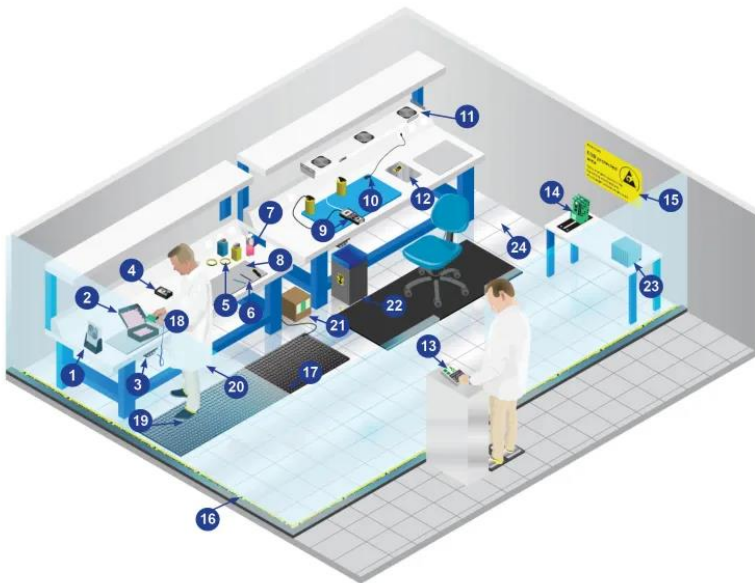
A fully ESD-safe workbench is being built and evaluated at BNL, which will help multiple test sites in future building the similar workbenches.

ESD monitor

- A typical ESD monitor is set in protection architecture and mainly includes monitor, remotes, power supply, mat cord and mechanical fixed part. The monitor powered by AC adapter and all GND cable snap to the ground. When operators start working, the wrist strap should link with the monitor on itself or the remote part. Then, the voltage status are under an effective monitoring.
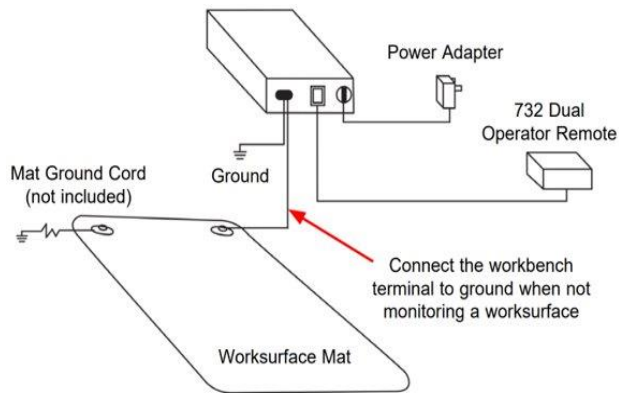
DESCO: 94391

For fixed workstation

SCS: 725

Carry on environment
(e.g. installation)

➢ SCS 725 was applied during Yale CRP4 CE installation. It is small, flexible, and sensitive.
➢ It receives positive feedback from the BNL CE installation team at Yale.

Summary

➢ DUNE ASIC Test Stand is being finalized

  ▪ All 3 ASICs show high yield at both warm and cold

  ▪ DAT can meet 3 ASICs QC requirements and a revision is ready

  ▪ RTS prototype can support automated ASIC handing and cryo cycling by end of May

  ▪ The current QC test stand built for ProtoDUNE will be kept in service for a while until DUNE ASIC test stand is deployed

➢ TPC electronics consortium complies with DUNE STANDARD

  ▪ Any work on DUNE ASICs (installation in sockets, inspection, testing, etc.) must be performed only at ESD-safe workstation designed according to the above guidelines. The work must be performed by trained personnel.

  ▪ A fully ESD-safe workbench is being built and evaluated at BNL, which will help multiple test sites in future building the similar workbenches.

  ▪ ESD monitor is recommended in future DUNE CE installation activities.

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backups

Charge Questions

2. Have life-time tests of all ASICs been done?

- LArASIC PRR review on Mar 7-8, 2022 has responded to this question.
  - https://indico.fnal.gov/event/53072/timetable/#20220307
  - https://edms.cern.ch/document/2314428/2
- LArASIC is designed with HCE tolerance
  - All transistors in LArASIC are well below nominal voltage of 1.8V and at low I_{sub}
  - All n-channel devices are either 270 nm or longer, at voltages 1.5 V or lower
  - Reduce V_{ds} by 6%, for each order of magnitude margin in the lifetime
- Two chips stressed under 3.1 V for over 900 hours
  - No significant degradation observed so far (< 1%), still under stressed
  - 3.1V down to 1.8V, there is over 8 orders of magnitude, predicted lifetime is ~1x10^7 years
- Oxide damage
  - >= 3.2V is much higher than the maximum voltage (~2V) allowed by TSMC 180 nm process, the degradation could be caused by oxide damage
  - If degradation is caused by oxide damage, LArASIC lifetime will be longer than the below projection plots.
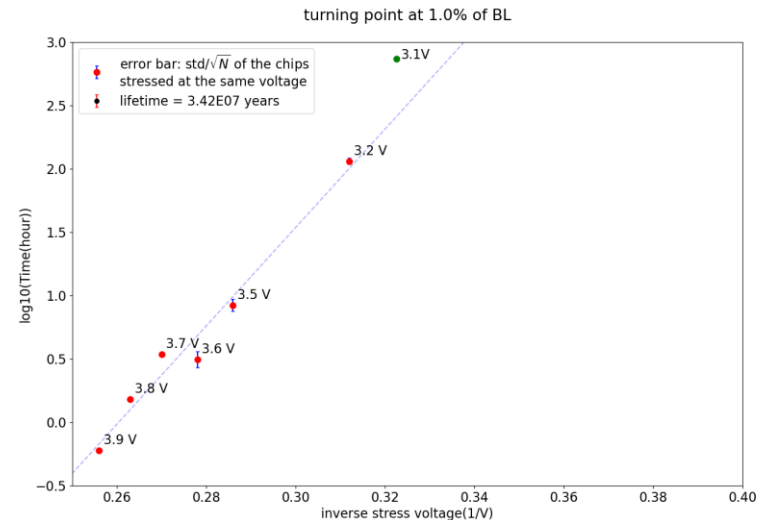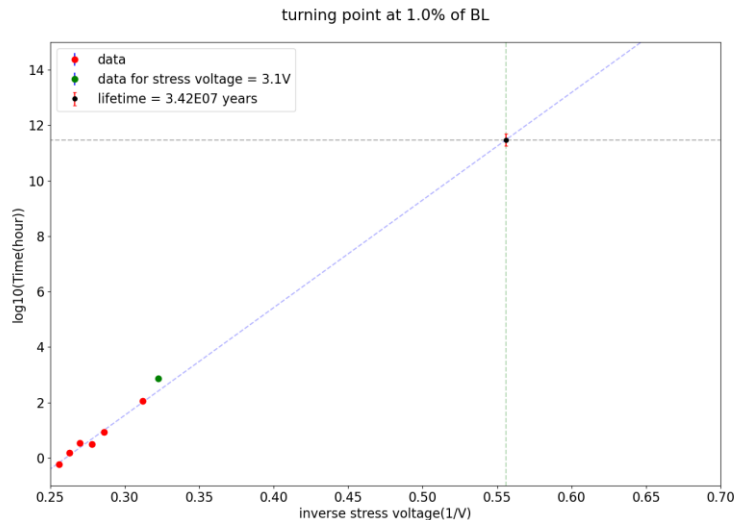
Plotted by Rado Razakamiandra

Charge Questions

5. Have the ASICs QC procedures been defined and documented? Have sufficient resources been allocated to successfully execute the QA/QC plan?

- LArASIC PRR review on Mar 7-8, 2022 has responded to this question.
  - https://indico.fnal.gov/event/53072/timetable/#20220307
  - https://edms.cern.ch/document/2314428/2

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