ColdADC/COLDATA Production Plan

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FD1 TPC Electronics (Cold ASICS+FPGA) PRR

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WIB FPGA procurement plan was covered in Hucheng's presentation

This presentation will focus on the ColdADC/COLDATA production

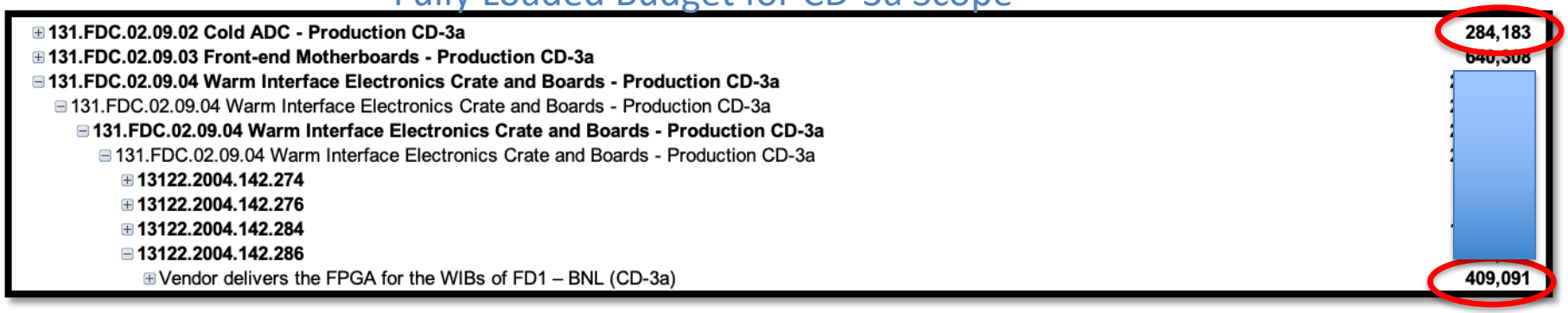
ColdADC/COLDATA Procurement for FD1

- FD1 has 150 APAs + 2 spares → Need 3040 FEMBs
- Add 10% spares of FEMB → 3,350 FEMBs to be fabricated
- Each FEMB needs 8 ColdADC and 2 ColdDATA
- Number of ASICs required:
  - 3350 FEMBs x 8 ColdADC = 26,800 ColdADC chips
  - 3350 FEMBs x 2 COLDATA = 6,700 COLDATA chips
- Assume conservative dicing/packaging yield of 95% and 95% passes LN2 test → final ASIC yield of 90.3%
- Factoring yield, we need:
  - 26,800/0.93 = 29,700 ColdADC chips
  - 6,7800/0.93 = 7,500 COLDATA chips
- Each wafer has 850 ColdADC and 276 COLDATA ASICs
- Need 35 wafers
- Production is in batch of 25 wafers → for FD1 need to procure 2 batches of 50 wafers

CD-3a Scope

- CD-3a includes the procurement of WIB FPGAs and ColdADC/COLDATA for FD1
- Received CD-3a ESAAB approval from DOE early this year

Fully Loaded Budget for CD-3a Scope



- Procurement of ColdADC/COLDATA is through CERN as part of the CERN/IMEC/TSMC frame contract
- CERN has been informed that we will place an order of 50 wafers in the coming months

Quality Control Resources

- Plan to have two QC sites per ASIC. LBNL and Louisiana State U. for ColdADC. FNAL and UC-Irvine for COLDATA
- Each site will have a Robotic Test System. Can test 16 ColdADCs or 4 COLDATA using two DAT boards
- For labor resources, assume 1.5 hrs per test cycle for ColdADC and 1 hr per test cycle for COLDATA. Also assumes 10% of the tests will need to be re-run
- Total ColdADC QC labor per site:
  - ~2,000 hrs of undergraduate students running QC tests
  - ~400 hrs of postdoc for supervising
  - 200 hrs of engineer
- Total COLDATA QC labor per site:
  - ~1,900 hrs of postdoc (FNAL) or undergraduate student (UC-Irvine) running QC tests
  - ~400 hrs of scientist (FNAL) or postdoc (UC-Irvine) for supervising
  - 200 hrs of engineer

Production Schedule

- Assuming we receive CD-2/3 ESAAB approval in Feb of 2024, assembly of the first batch of FEMB for FD1 will start in fall of 2024

- QC testing of the first batch of ColdADC/COLDATA need to start by May 2024

- Production schedule (from P6):
  - Jun 2023: Submit order for 50 wafers of ColdADC/COLDATA
  - Jan 2024: Receive 50 wafers of ColdADC/COLDATA from IMEC
  - Jan 2024: Submit ColdADC/COLDATA for packaging
  - Apr 2024: Receive packaged chips from ASE
  - May 2024: Start of ColdADC/COLDATA QC testing

Thank You !