Design Validation I:
Highlight results from VD PDS Prototyping Phase

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Prototyping Campaigns - CERN Coldbox

- Since December 2021: testing of the FD2-PDS system in realistic conditions
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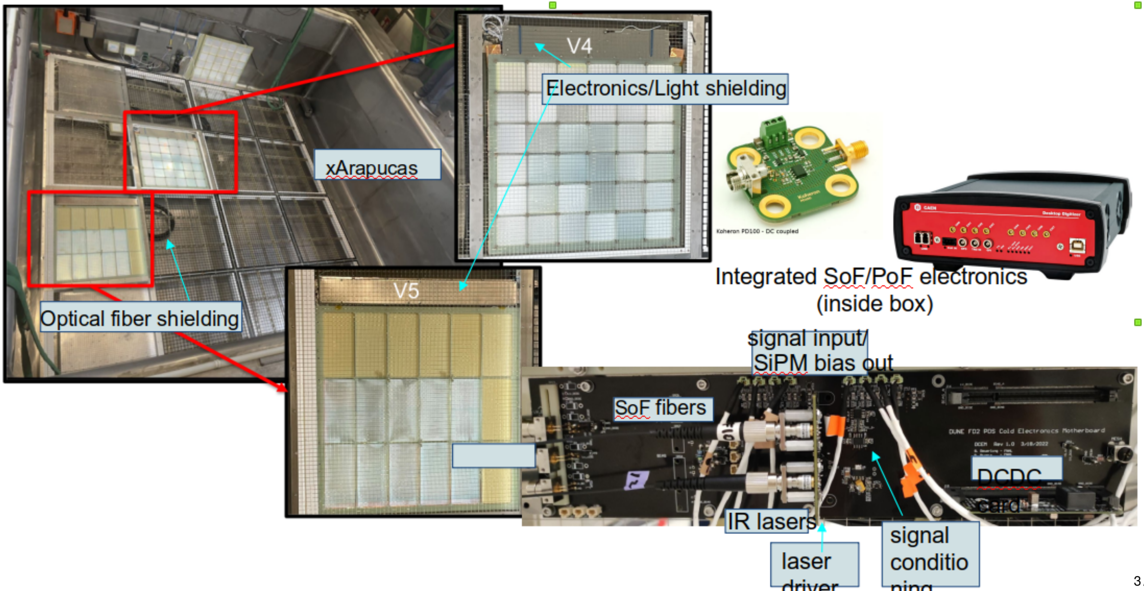
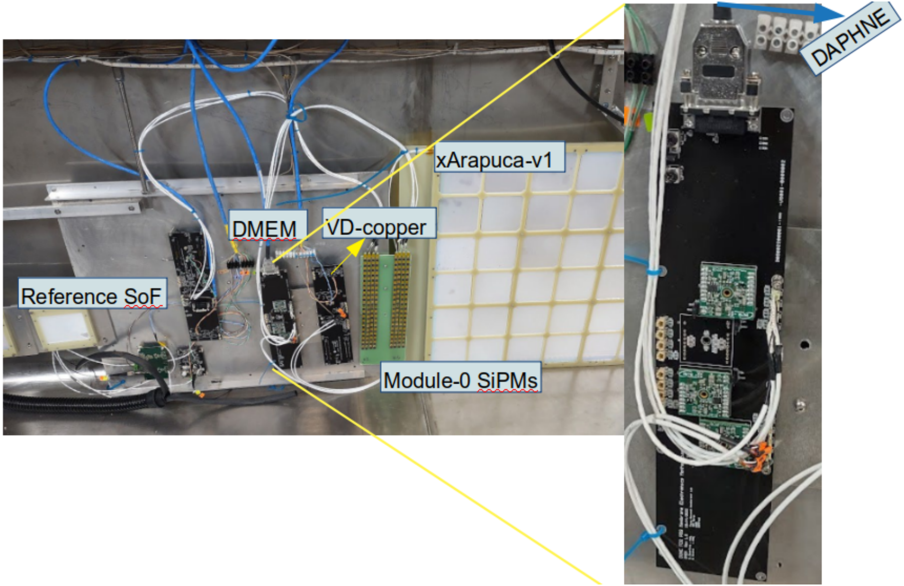
Purpose of the coldbox:

- Testing of the PDS system in realistic conditions
  → best/only way to validate the behaviour of certain components
- Integration to CRP systeam
  → coordinated data taking

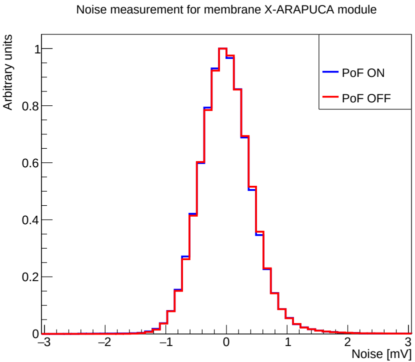
Coldbox Installation - Cathode

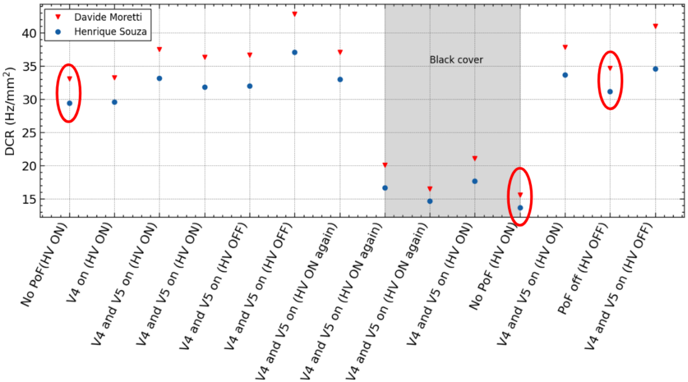


Coldbox Installation - Membrane



PoF and light leakage?





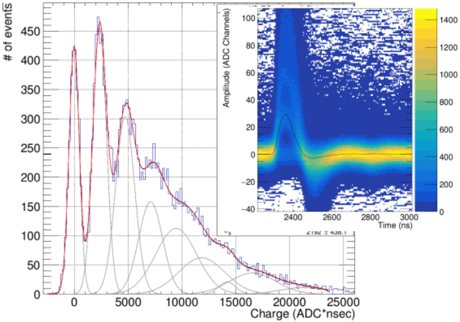
- fibers with black jacket
- black tubing
- cases for the electronics
- Still, light coming from oustide affects membrane measurements (tbd later)

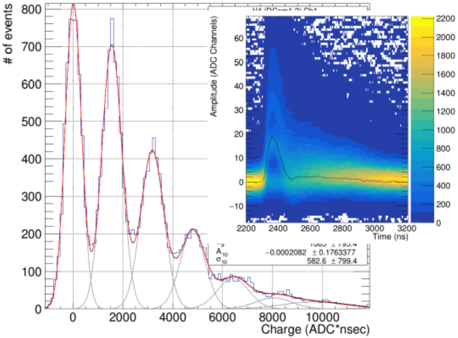
Result: no measureable light leakage from cathode system

Cold Electronics Tested: SoF

- Between December 2022 and March 2023: new implementation of integrated DCEM 1.2 SoF/PoF electronics
- Testing of fine tuning: gain, pairing with DCDC, laser selection
- what changed: extension of dynamic range (circuit modification), electronics in metallic boxes, all fibers have black jackets, powering with 2 OPCs proved

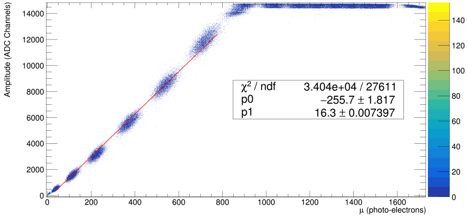
SoF results - SPE sensitivity



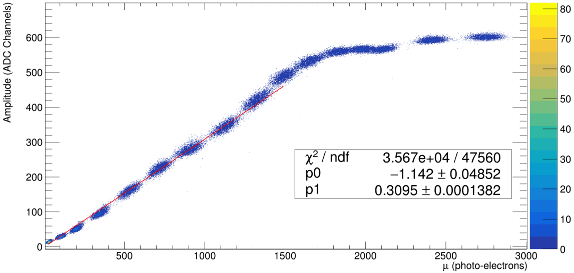


- SPE signals extracted for both modules, with slightly different readout electronics configurations.
- Rise time obtain is between 40 and 50 ns
- SNR is consistent over channels and modules, at ~ 5

SoF results - dynamic range and calibration



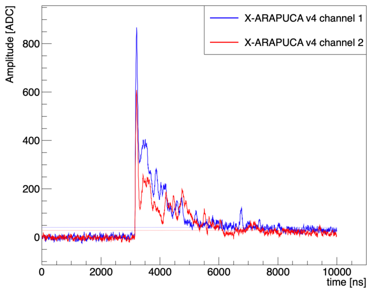
SPE amplitude ∼18 ADCs → warm side saturation at ∼780 PE

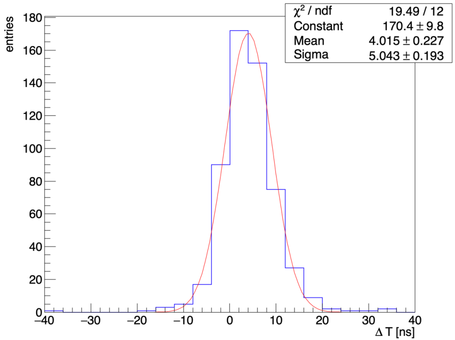


Using intercalibration, dynamic range of the cold electronics ∼

- Linearity limitations: LED light non linearities and commercial receiver saturation
- LED behaviour was checked by comparing with signals from cosmics
- A light attenuator was added on the warm side to explore the full dynamic range of the cold electronics
- On-going simulation-based studies to determine a physics-driven requirement for the dynamic range.
- Add a small linearity plot with cosmics to show that it's just LED effects?

SoF Time resolution





- Time resolution considers two channels of the same xArapuca (assumed to have same resolution)
- No fit/interpolation used to estimate the signal times

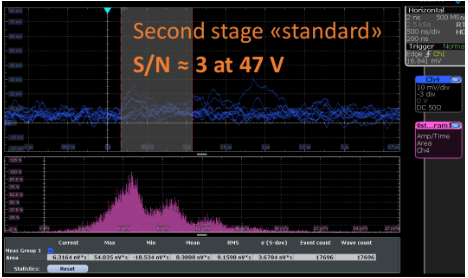
- $\sigma_T \sim \sigma(t_{ch1} - t_{ch2})/\sqrt{2}$
- Time resolution is consistent with digital sampling rate $\sim$ 4 ns

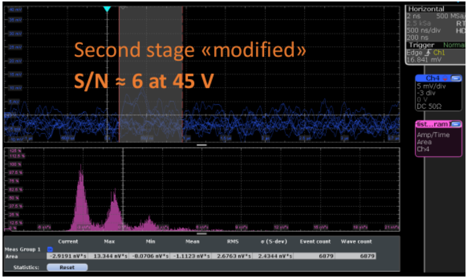
Cold Electronics Tested: HD - copper

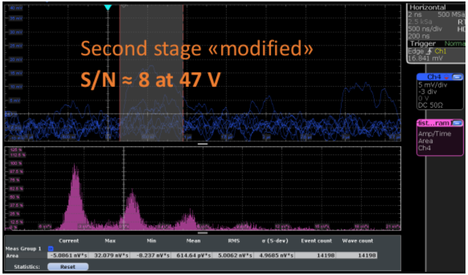
Same HD amplifier but in new context: SiPM hybrid ganging, new mother board. Tuning to be able to function. Succes.

- Above SiPM breakdown, high background rate, ≈100kHz (39Ar, Cosmics..)-¿ mention dark cover needed!

Membrane readout results



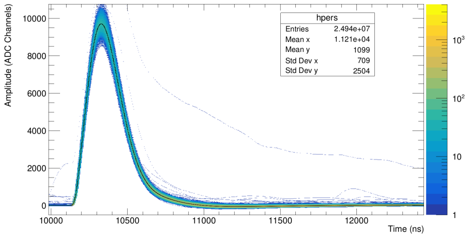


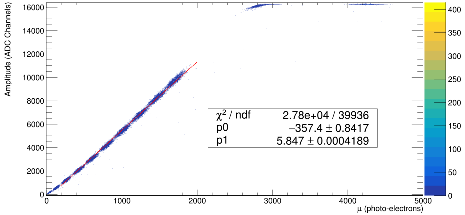


- DAPHNE input stage ”jumped” to avoid undershoot issues
- High background rate, $\sim$100 kHz $\rightarrow$ possibly cosmics and external light

Cold Electronics Tested: VD-copper

Development motivated to have similar membrane and cathode signals.
this is february...no plots from march?





- SPE amplitude $\sim$ 6 ADCs
- Rise time
- Undershoot/Overshoot
- Linear (with LED effects) up to 1750 - 2100 p.e.

Laser R& D

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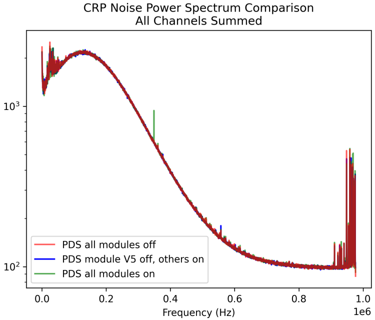
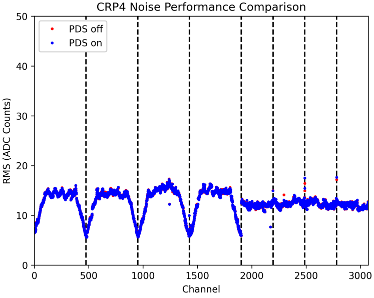
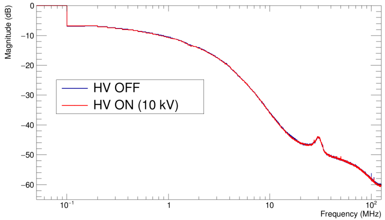
Integration

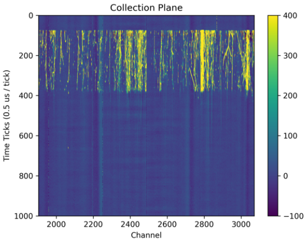


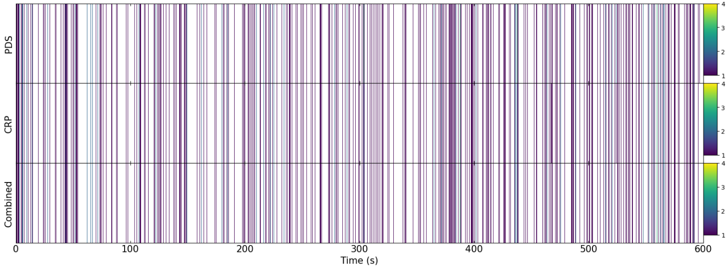




- Only a small 300 kHz peak detected by the CRP electronics, coming from V5 ”hybrid” electronics (now replaced)
- This contribution could not be detected in the electronics noise
- No effect from HV ON/OFF in the PDS

Data taking with CRP





Conclusions

- Last few months of prototype testing campaigns led up to a mature configuration and satisfactory data output
- All PDS components have been running over multiple cycles inside the coldbox
- Performance goals have been mostly achieved
- Reliability of the system was highly improved $\rightarrow$ resistance to multiple thermal cycles $\rightarrow$ but data taking periods are short, longer running tests to be done in the laboratory?

Back Up

Timeline and main benchmarks

February 2021 start of investigations

- analog circuit component selection
- decision to use lasers (over LED) with connectors
- definition of basic circuit characteristics

June 2021 First working analog transmitter

- laboratory tests with SiPMs in LN2 → SPE transmission

September - December 2021 Coldbox A_1

→ **successful SoF operation, with HV ON. Powered using Si PoF modules.**

March 2021: Ariadne parasitic run (A_2)

→ **additional statistics, long operation and first test with (preliminary) DAPHNE**

May 2022 Coldbox A_3 → first test of GaAs

July 2022 Coldbox B

→ **2 xARAPUCAS on cathode and integrated board**

August 2022 Coldbox B+ and B++ → dedicated PDS runs

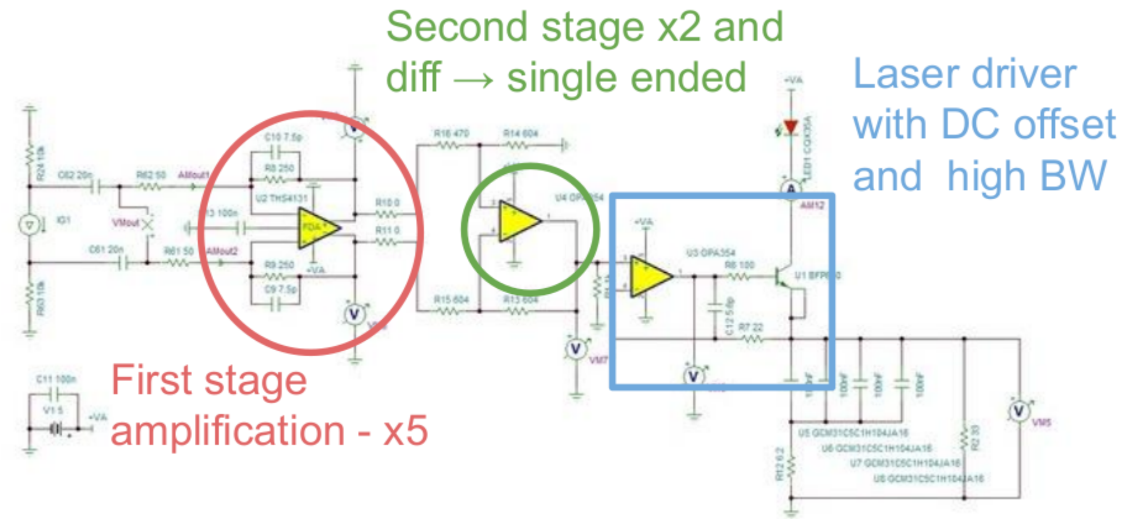
October-December 2022 CRP3, CRP2b runs → Optimized system

March 2023 Module 0

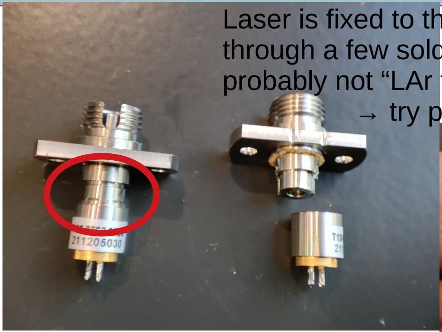
2021 - R&D towards functional prototypes

2022 - Optimization, performance, mechanics and installation - Extensive use of SoF.

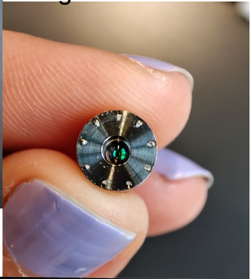
Analog Transmitter Circuit

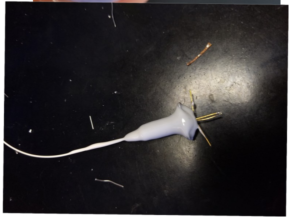


Lasermate FC connector



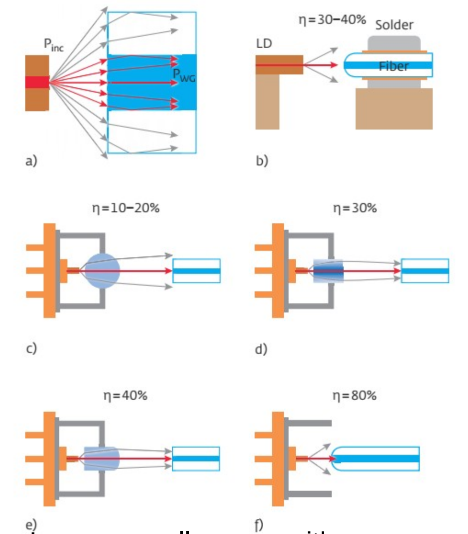
Laser is fixed to the FC connector through a few solder points: probably not “LAr tight”
→ try potting this area?





* There seems to be a lens inside → usually the laser beam has a focus point ~few mm from lens

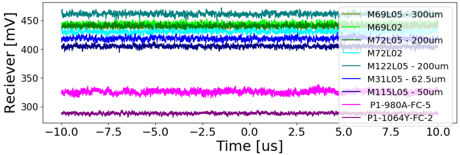
* By fully potting a pigtailed laser we did not see the power output drop
* potting is not trivial

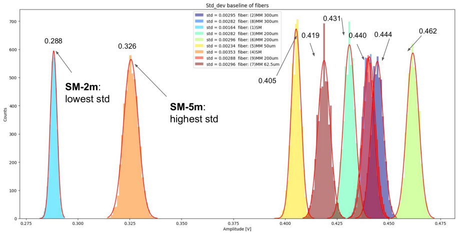


Lasers usually come with some kind of lens → not clear how LAr affects the focus

Fibers

Comparison of 2 single mode and 7 multi mode fibers of different core size and various characteristics and lengths.





- Single mode should be more stable but depends on which fiber. Pigtail is stable
- Multimode has a much larger transmission efficiency
- Multimode could present modal noise
- jacket material could affect the fiber when in cold
- Testing of graded index fiber (as opposed to step index)
- sharp bends should be avoided $\rightarrow$ laser adapter card is vertical

Low-Drop Out Voltage Regulator

First choice of LDO regulator is LP3964

- requires an output capacitor with a relatively high ESR
- recommended tantalum capacitors are not suitable for long-term durability
- tested solution 1: add a resistor in series
- tested solution 2: switch to a more modern LDO AMD7151 that doesn't have this ESR requirement