FE ASIC for PDS Amplification

Shanshan Gao on behalf of BNL CE Team

06/27/2023

@BrookhavenLab

Dual Calorimetry: Improving Light Collection and Charge Resolution

Optimized Vertical Drift FD3-4: Light R/O technology optimization

Most (if not all) large mass, UG detectors for LowEn (solar) neutrino are Light r/o (scintillator or Cherenkov) based detectors
[featuring 4π coverage for a high & uniform LY - the base for a high detection efficiency and good energy resolution for LowEn events]

LAr-PDS optimization options

- **ARAPUCA(w/ SiPM) technology is still young, with large margins of improvement thanks to well proven flexibility**
  - *ARAPUCA bar w/ few (12)SiPM/channel + Warm Elec [Anode plane coverage] - protoDUNE-SP-2018*
  - *X-ARAPUCA bar w/ more (48)SiPM/channel + Cold & Warm Elec [Anode plane]* ⇒ *DUNE **FD1- 2022***
  - *X-ARAPUCA large tile w/ many (80)SiPM/channel + **PoF-CE-SoF** & Warm ADC [HV Cathode plane & Membrane Walls]* ⇒ *DUNE **FD2 - 2023***
- **Next "natural" optimization step:**
  - X-ARAPUCA + **PoF & CE(FE+ADC) & SoF** + design flexibility for massive increase of coverage on FieldCage

⇒ **convert TPC Field Cage structure into a fully active PDS**
- extended optical coverage for High and Uniform (Scintillation) LY

OR

- **Change technology of Light signal read-out**
  - **Integrated light pixels in Anode plane (Solar/Q-pix)**
  - **Combine light pixels in Anode plane with X-ARAPUCA tiles on the Cathode plane**

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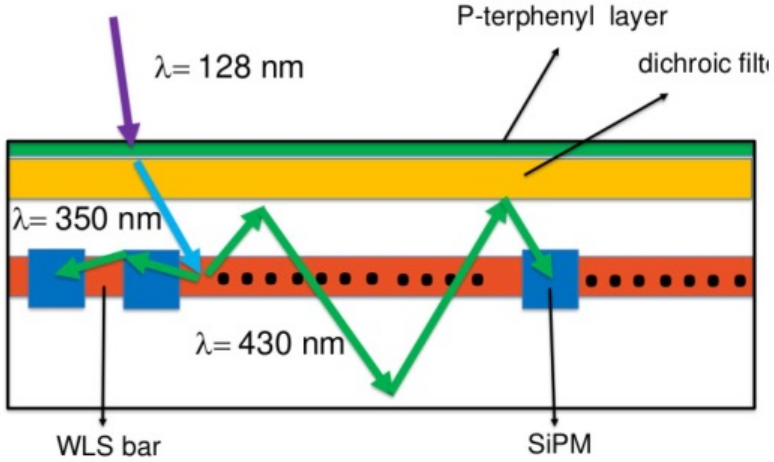
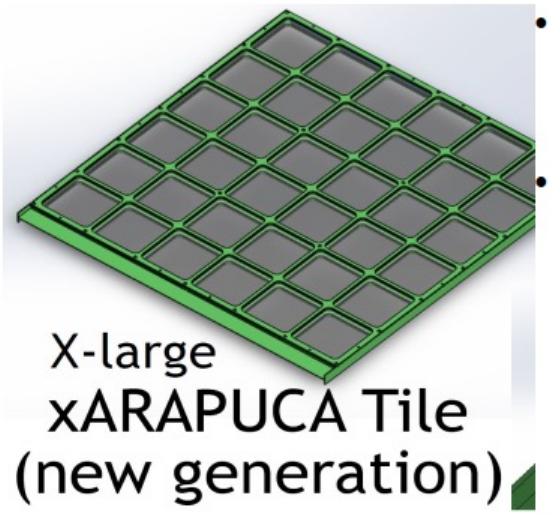
Vejlko's talk on Lidine 2021

DUNE FD-2: ARAPUCA (Argon R&D Advanced Program at UniCAmp).



Credits: F. Terranova

- 160 SiPMs (40 per side)
  - Glued to WLS Bar for improved optical contact
- SiPMs mounted on Kapton flexi-PCB



- **Optical area**
  - **600 mm x 600 mm=3600 cm^2**
- **SiPM area**
  - **160 x 0.36 cm^2 ≈60 cm^2**
  - **≈1.7 % of opt. area**
- **SiPM array capacitance ≈200 nF for V_{bd}~45 V;**
- **≈260 nF for V_{bd}~37 V**

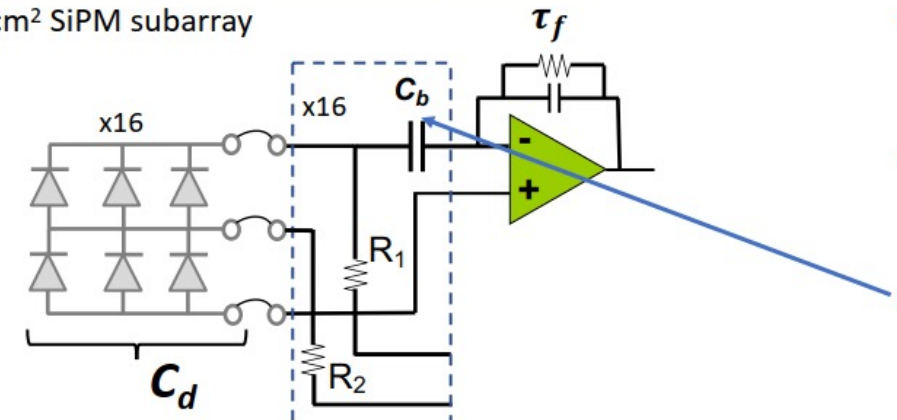
Readout a challenge for DUNE and SBND!

M.C. Queiroga Bazetto, V.L. Pimentel, A.A. Machado and E. Segreto, in Campinas, Brazil

“Giant” SiPM Capacitance

Technology	“HPK”	“FBK”
C/A [nF/cm^2]	3.5	8.5
V_{op} [V]	60	30
C_{6cm^2} [nF]	21	51
C_{2s} [nF]	5	12.5
V_{2s} [V]	120	60

6cm^2 SiPM subarray



Assumptions (approx.):
- Number of readout channels ~8000x6cm^2 ~4.8 m^2
- Readout power dissipation < 80 W

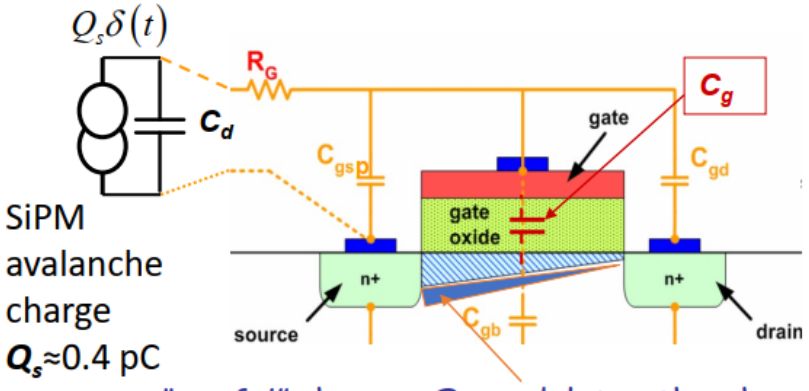
Why “*Giant*”?

SiPM capacitance C_d (in any practical arrangement) is much higher than in any known detector

- C_d is large, but so is the charge/pe, Qs ~ 0.4 pC (2.4 x 10^6 e$^-$)
- *The charge is bound to that giant capacitance, can we “see” it??*
- *How to “extract” the charge while applying the bias to SiPMs?*
- *Does C_b, the decoupling (radiopure) HV capacitor have also to be “giant”?*

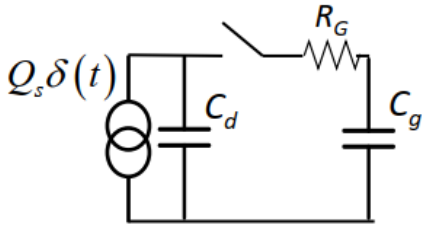
Study based on the nEXO PRE development

How much of the avalanche charge can we really "see"?
SiPM – transistor capacitance mismatch



SiPM avalanche charge Q_s≈0.4 pC

"useful" charge: Q_g modulates the channel and with transistor noise determines S/N



$$\frac{Q_g}{Q_s} = \frac{C_g}{C_g + C_d}$$

Example:

Transistor gate: C_g **=25pF** (very large transistor)

	nEXO	xARAPUCA
SiPM array: C_d	**≥20 nF**	**>200 nF**
$(Q_g/Q_s)=(Cg/Cd)$	≤1/800	≤1/8000

We "see" ~ **1 part in 10^3 or 10^4** of the SiPM avalanche charge Q_s.

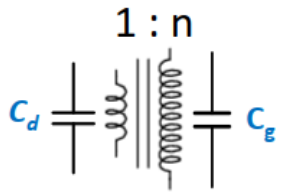
A long way from the optimal sharing of charge:

$(Q_g/Q_s)_{max}$ **= 1/2**
for **(***Cg/Cd)=1*

SiPM-to-transistor capacitance matching: *SNR* vs transformation ratio *n*

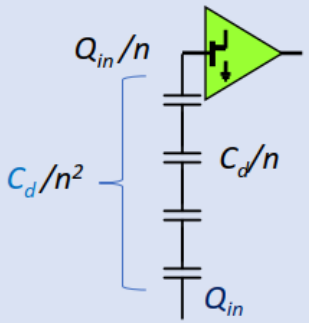
$$n_{opt} = \left(\frac{C_d}{C_{gs}}\right)^{1/2} \qquad \left(\frac{S}{N}\right)_{(n)/(n=1)} \simeq n_{opt}\frac{n/n_{opt}}{1+\left(n/n_{opt}\right)^2} \qquad \left(\frac{S}{N}\right)_{(\max)/(n=1)} = \frac{n_{opt}}{2}$$

n= transformation ratio for ***EM and ES transformers***; for ***transistors in parallel***: $n = n_{trans.}^{1/2}$



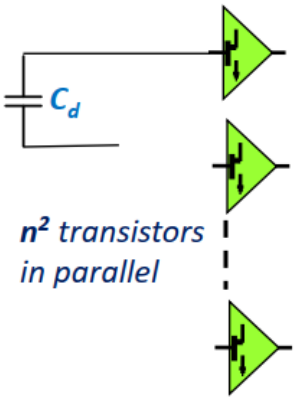
EM transformer, most effective and proven, but not radio pure (introduced 1974)

For C_d=20 nF, C_g=25 pF → n_{opt}={C_d/C_g)^1/2~**28**, ***S/N* is increased by n_{opt}/2=14**



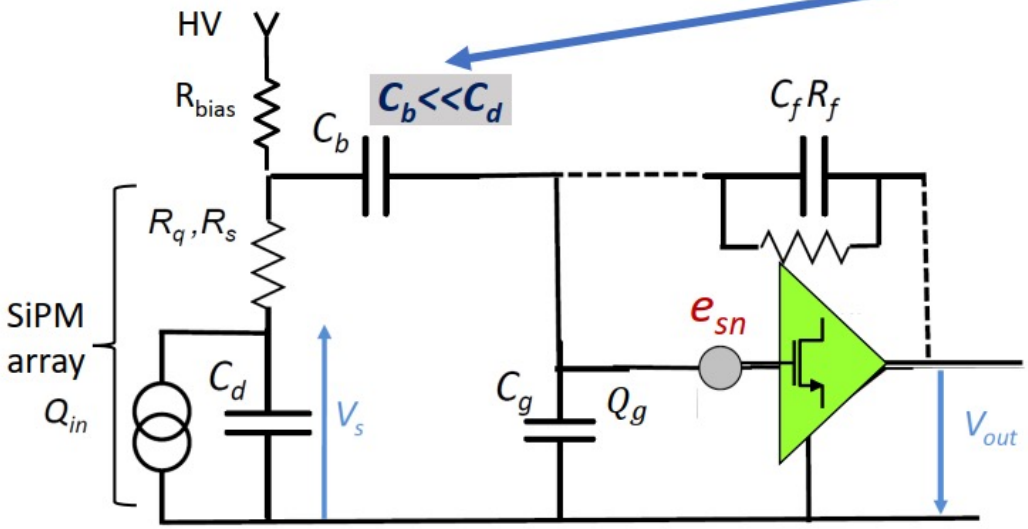
ES (Electrostatic) transformer
(introduced 1990)

ES transformer n=4 improves *S/N* by a factor of ~ 3.95 ;
compared to parallel connection of SiPMs.



For n=4, it would take ***n^2*=16,** times as large a transistor area ***and power*** for the same result as with EM or ES transformer.

Optimal readout for SiPM arrays: Weak coupling to amplifier



Basic limitation: Only ***adiabatically*** *transferred fraction of avalanche charge to transistor gate,* $Q_g \approx \frac{C_g}{C_d} Q_{in}$ *contributes to S/N.*

Conventional approach: Strong coupling -- *active (forced) transfer of charge* is accompanied by corresponding increase in noise ***with no benefit to S/N***. It requires $C_b >> C_d$, resulting in (de)coupling capacitors in ***tens of nanofarads.***

Q_{in} = avalanche charge
C_d = capacitance of SiPM array in parallel;
***n* = ES transformation ratio**

$$\left(\frac{S}{N}\right)_n = \frac{Q_{in}/C_d}{e_{sn}/t_p^{1/2}} \cdot \frac{n}{1 + C_g/C_b + n^2 C_g/C_d}$$

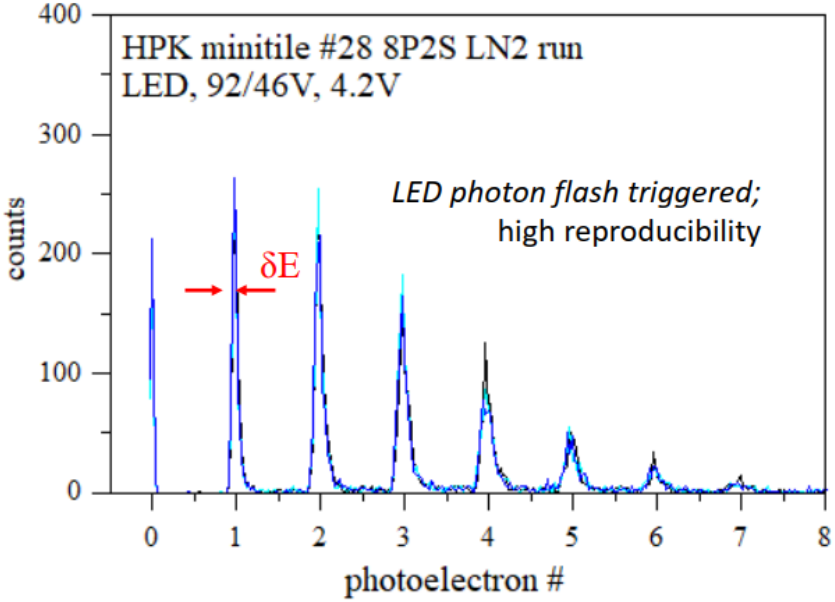
S/N analysis *shows:* C_b *must be larger than* C_g*, but can be* ***much smaller*** *than* C_d*:*

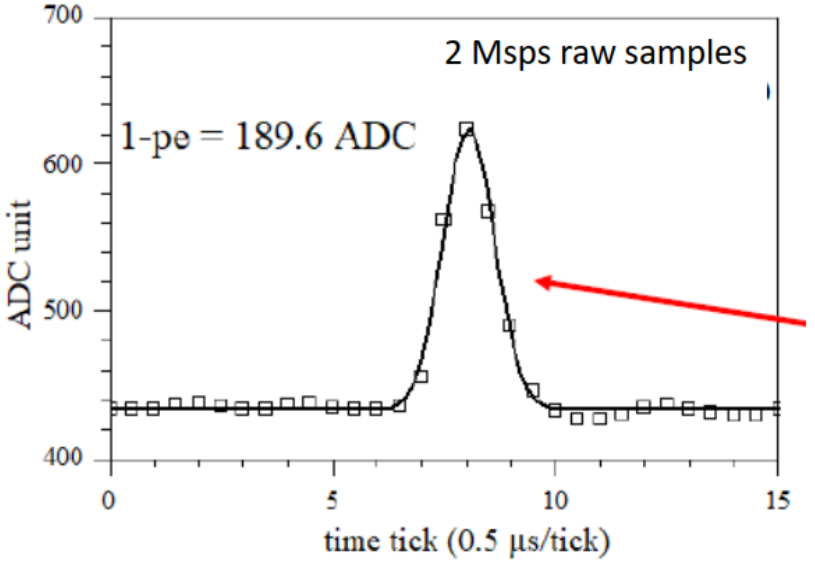
$C_d >> C_b >> C_g$

e.g., 20 nF>>0.5 nF>>25 pF

Solution: ***C_b has to be larger than C_g but can be much smaller than C_d***

BNL: Demonstration of 6 cm^2 SiPM(HPK) *20 nF subarrays* with LArASIC in LN2





Photon rate: ~80 Hz (trigger rate 100 Hz)

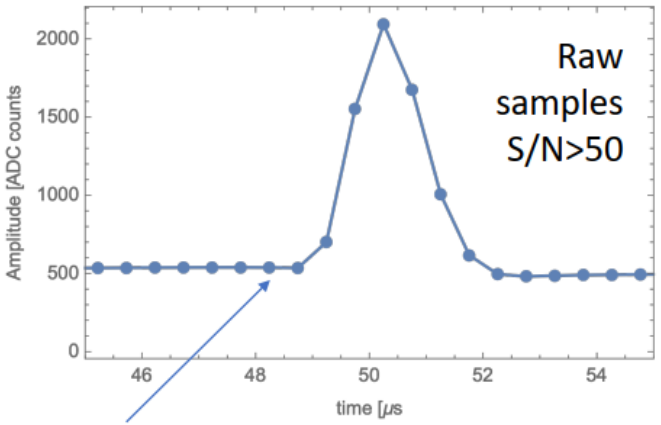
Single photoelectron waveform information provided by a "snippet" of samples :

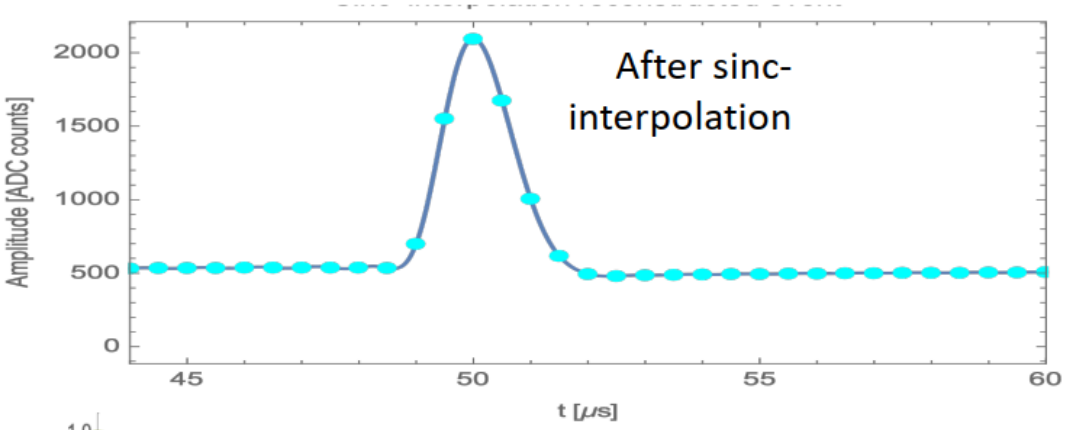
1-pe resolution (δE): 3 to 3.5% rms

- **1-pe *S/N* ~60 ; avalanche = 0.4 pC at OV=4 V**
- **1-pe *coincidence resolution* between two subarrays < 20 ns**

Excellent S/N obtained from the demonstration at BNL

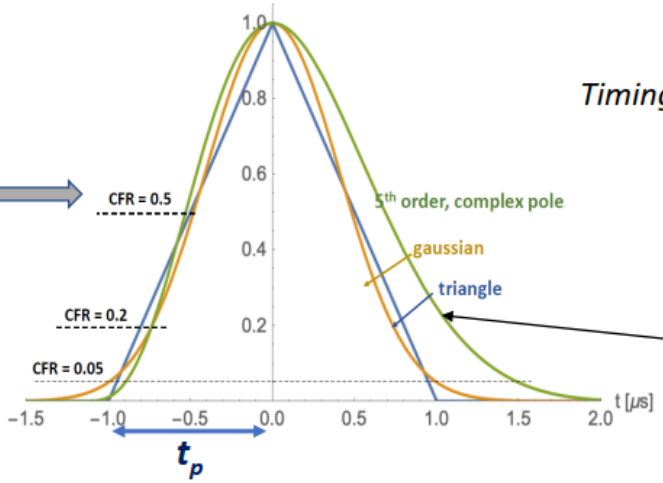
Waveform reconstruction and 1-pe timing resolution (SPTR)





Waveform snippet:
10 μs = 20 samples at **2Msps**;
t_p=1μs anti-aliasing filter (as per **Nyquist**: **$t_p \geq 2/f_s$**)

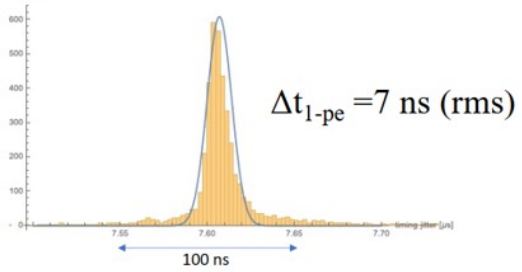
Using ***sinc-interpolation*** + 'digital' constant fraction discriminator, results in a low timing error (SPTR)



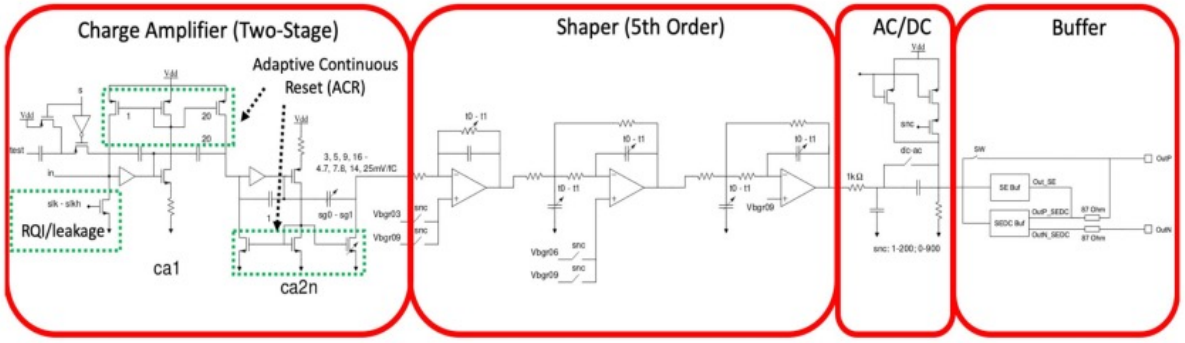
Timing resolution:

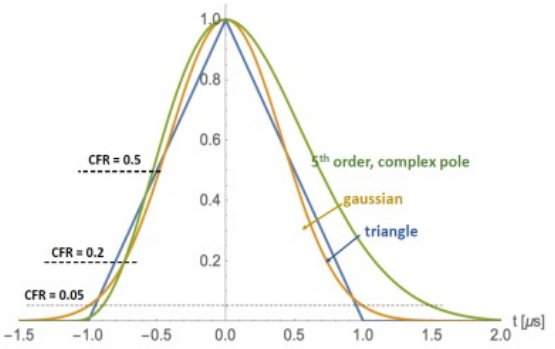
$$\sigma_t = \alpha_f \frac{t_p}{(S/N)}$$

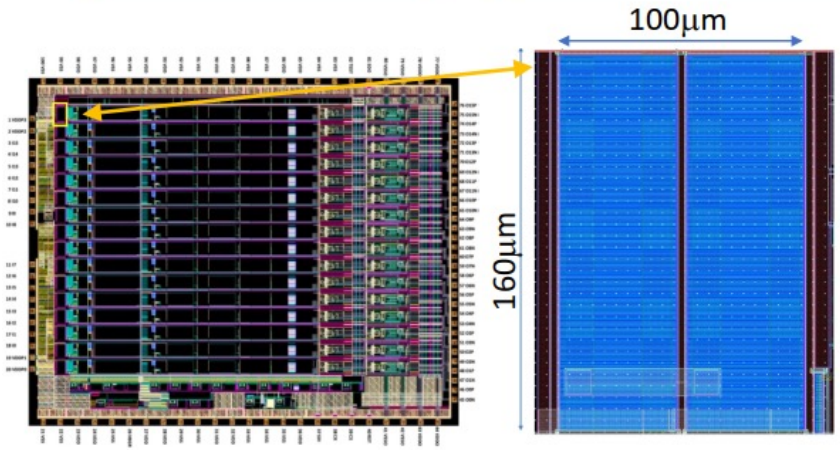
$\alpha_f = shape\,const. \approx 0.63$
(for 5th order complex pole)



LArASIC = Antialiasing Filter

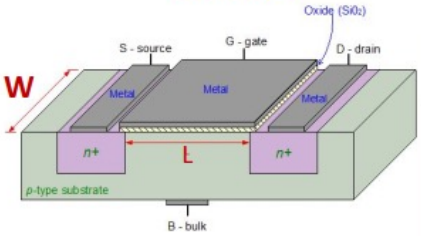






160μm x 100μm=16,000μm²

$$W/L = \frac{20\ mm}{270\ nm}$$



For a *very large low noise PMOS transistor:* W/L~4x10^4, C_g~20pF ; *This very large transistor is a small fraction of the SiPM array capacitance (20-200 nF!)*

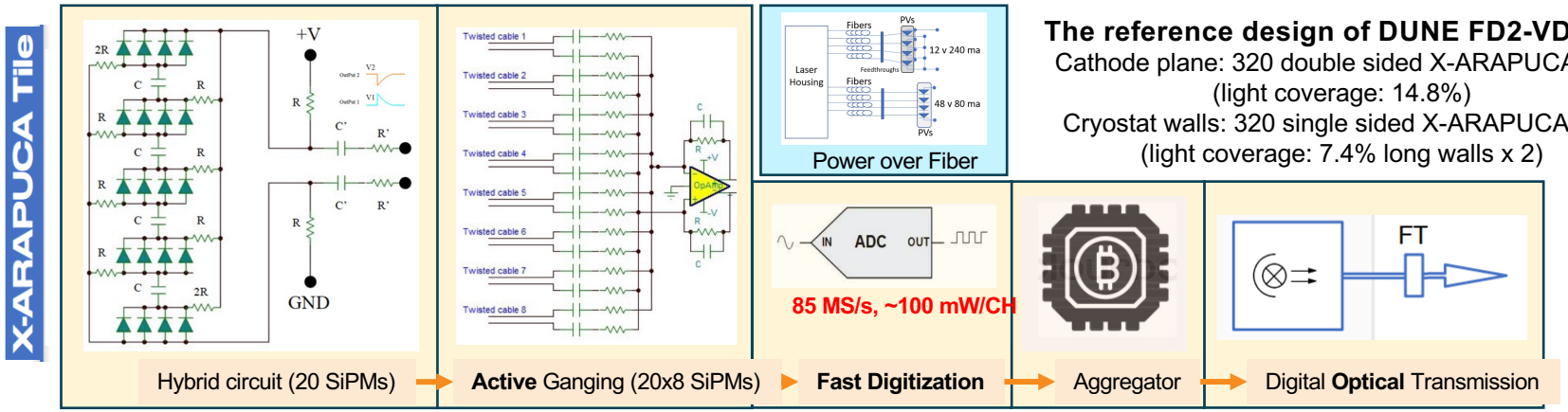
Why not an even larger transistor?

The equivalent noise resistance is smaller than SiPM quenching resistance and interconnections resistance (<10 ohms).

New FE ASIC to address physics requirements

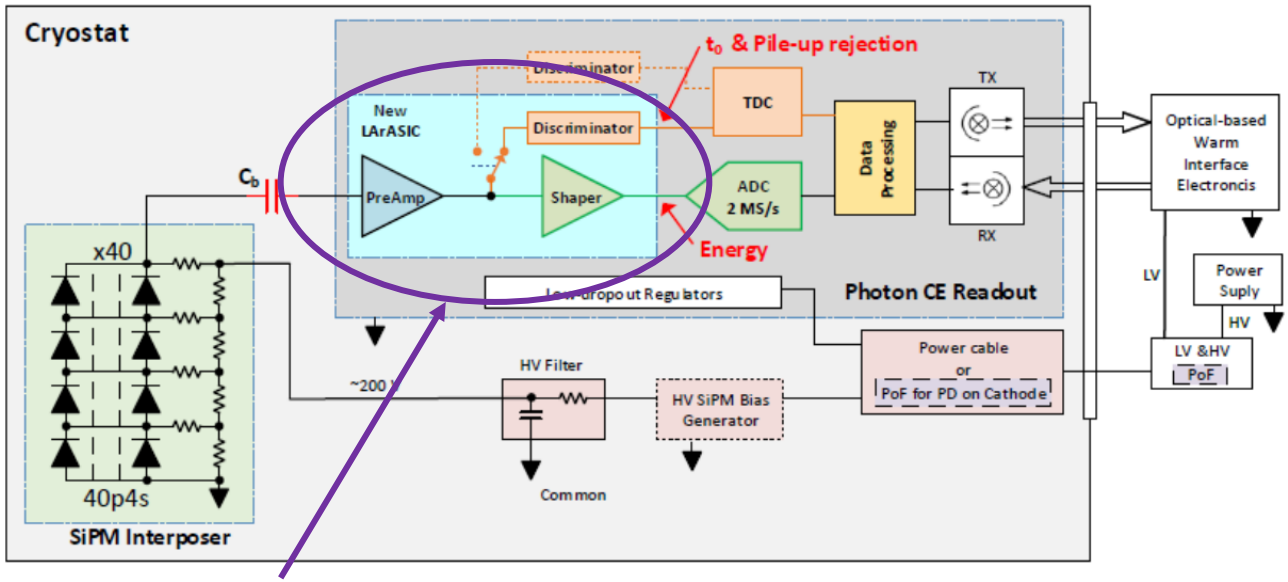
- Some solid physics input on the light vs. time and the information to be extracted
  - Physics Modeling and Simulation is ongoing at BNL
- Veljko's comments
  - A problem arises how to read several ARAPUCAs. Can we benefit from a multi-channel ASIC? 16 ARAPUCAs are spread over a large area. Given the very large capacitance of SiPMs, we could afford low impedance connections with high capacitance and low inductance. This may be ok for a "slow" readout with peaking time ~ 1 μs, but propagation time must be considered if a much faster readout is needed. This brings us to the next question:
  - How fast a readout is really needed in this case? As we know for event timing resolution even better than 100 ns, peaking time of ~ 1 μs is fine. If the physics (once it is understood) requires much faster waveform recording, then the anti-aliasing filter has to be made correspondingly faster, with serious consequences all along the chain (ADC, data serializer, transmission)
  - **Two points above may require a new FE ASIC design**. We may be able to keep the data system as is charge readout, if we use pulse shape discrimination between the fast and slow light components. This will still need a new FE ASIC to provide both the fast and slow signal. However, it will avoid the need to increase the sampling frequency
- The new FE ASIC design may need to take into account
  - Fast peaking time (~50 ns) followed by a peak detector
  - Dual gain configuration to cover large (> 2 k pe) signal dynamic range

The ultimate FD2-VD PDS readout scheme
(ongoing R&D carried by DUNE SP PDS group)



The reference design of DUNE FD2-VD PDS
Cathode plane: 320 double sided X-ARAPUCA tiles
(light coverage: 14.8%)
Cryostat walls: 320 single sided X-ARAPUCA tiles
(light coverage: 7.4% long walls x 2)

a (top), b(bottom)



Propose new FE ASIC design

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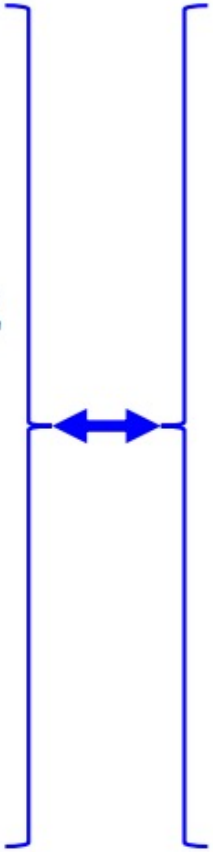
R&D of Advanced Analog FE for Noble Liquid Detectors

- Deep knowledge in low noise electronics systems for noble liquid detectors
- Expertise in low noise microelectronics for applications in extreme environments
- Successful development of AFE ASICs in large HEP experiments recently
- Expertise in signal processing and detector performance studies
- Explore both charge and light readout in noble liquid detectors
- Integral system design approach to optimize detector design



- Invention of LAr calorimeter at BNL ~half century ago
- Cryogenic temperature and high radiation
- LArASIC for DUNE FD1-HD/FD2-VD LArTPC, AFE for ATLAS LAr calorimeter HL-LHC upgrade
- Wire-cell in LArTPC reconstruction
- DUNE, nEXO, PIONEER, FLArE, FCC-ee etc.
- Electrode, analog signal processing, readout electronics system and integration systematically

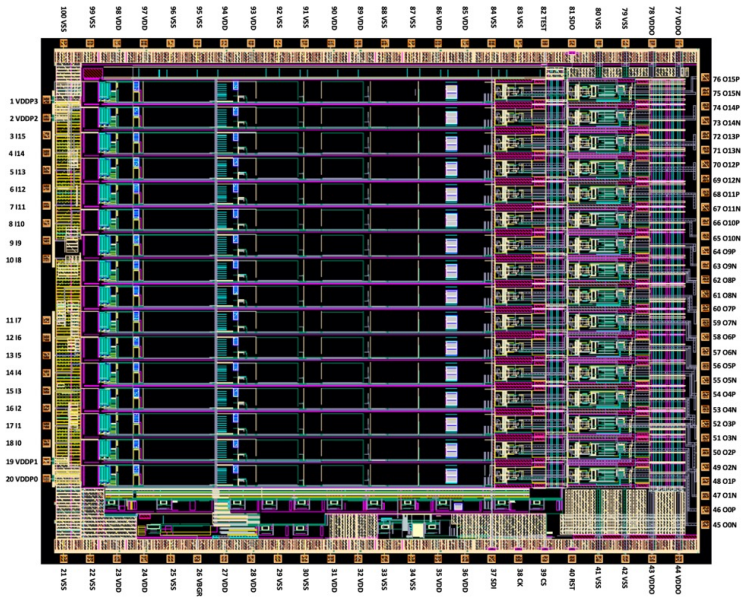
Study on New Front-End ASIC

- CSA design based on LArASIC suitable for charge and light detection
- Explore advanced CMOS node 65 nm suitable for both cryogenic temperature and high radiation environments
- Long cryogenic lifetime and radiation tolerance
- Wide signal dynamic range with excellent linearity
- Versatile configurations to optimize signal processing
- Flexible control and monitoring interface with precision calibration
- Programmable output stage to ease digitization interface

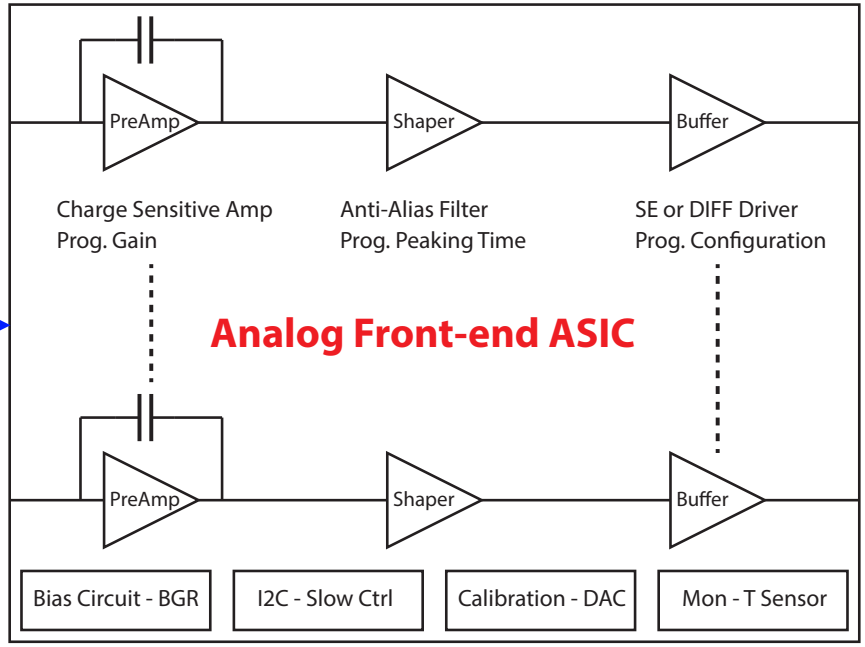
- Demonstrated performance of in charge readout of ProtoDUNE and light readout of nEXO
- Cryogenic model by DUNE and radiation model by RD53
- Follow well established design rules
- Thick oxide for higher supply voltage with more gain options
- Short peaking time options for better time resolution and pile-up rejection
- Standard I2C with built-in charge calibration
- Buffer is readily available for integration with custom or COTS ADC for downstream signal processing

- Studies for trade-off of technical parameters (SNR, power, shaping etc.) to reach optimal balance of performance parameters (energy resolution, time resolution, spatial resolution etc.)

Advanced AFE for Noble Liquid Detectors



180 nm design for DUNE



- Analog front-end ASIC with multiple (16+) channels and programmability
  - Integrated auxiliary circuits for direct application in detector systems
  - High performance ***analog front-end block*** for easy expansion to targeted design of ***future experiments, e.g. FCC-ee***
- Key features and challenges
  - ***65 nm*** CMOS with ***thick oxide*** → Max Vdd (1.8 V, 2.5 V) to support extended ***dynamic range***
  - ***Fast*** peaking time (in the order of 10 ns) → support signal processing with stringent ***time resolution***
  - ***Low*** power consumption → support detector electrodes with ***fine segmentations***
  - ***Cryogenic*** operation with ***long lifetime*** → achieve optimum ***SNR***
  - Long term goals: fast front-end architecture (~***GHz*** bandwidth), high ***radiation*** tolerance → ***FCC-hh***

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New LArASIC Requirements (1)

		New ASIC opportunities		
	DUNE FD1/FD2(bottom) Charge Readout	DUNE FD2/3/4 Light Readout	DUNE FD3/4 Charge Readout	PIONEER
ASIC	**P5B LArASIC**	new	new	new
CMOS process	**180nm (discontinued)**	65nm	65nm	65nm
Supply Voltage	**1.8V**			
Integrated Regulators	**No**	low noise LDO is preferred	low noise LDO is preferred	low noise LDO is preferred
Input channels	**16**			
Power consumption per channel /mW	**~6mW/ch with SE mode**			
Gain	**4.7, 7.8, 14.0, 25 mV/fC (4 options)**			
Input leakage current	**100pA/500pA/1nA/5nA**			
Peak time	**0.5, 1.0, 2.0, 3.0 us**	**~100ns**	**~ 1 us, 2us**	**20ns**
Detector Capacitor	**150~200 pF**	weak-coupling	150-200 pF	**20pF**
Input Impediance	**50 Ohm?**	200 Ohm?		as low as possible
dynamic range	**100 fC @ 14mV/fC**	as large as possible, resolution: 1pe? split signal and record both low and high gains?		up to 40~50 fC
non-linearity	**<1% (0.1%)**	?		< 1% (?)
Baseline options	**200mV/900mV**			

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New LArASIC Requirements (2)

		New ASIC opportunities		
	DUNE FD1/FD2(bottom) Charge Readout	DUNE FD2/3/4 Light Readout	DUNE FD3/4 Charge Readout	PIONEER
ASIC	**P5B LArASIC**	new	new	new
noise	**ENC ~ 500 e- @ 150pF Cd at LAr**	sub 1pe resoluton		<850 e, as long as possible
SNR	**>10**			>10
Crosstalk	**<0.1%**			<0.1%
temperature	**77K - 300K**	77K - 300K	77K - 300K	160K - 300K
Lifetime	**30years**	30years	30years	
digitial interface	**SPI**	I2C	I2C	I2C
Reference	**BGR**	BGR / CMOS ?	BGR / CMOS ?	BGR / CMOS ?
anti-alias filter	**high-order filter**			
Monitor	**Temperature sensor**	Temperature sensor	Temperature sensor	Temperature sensor
DAC	**6-bit, range related to gain**	10-bit (?)	10-bit (?)	10-bit (?)
Output stage	**SE (H-Z) , SE(50Ohm), DIFF**			
Integrated Test Charge Injection Cap.	**~200fF (design)**			
Radiation Tolerance	**N/A**	N/A	N/A	
note	**needs HCE mitigation design**	In order to extend the dynamic range, detector signals is split into 2 weak-coupling channels to FE		

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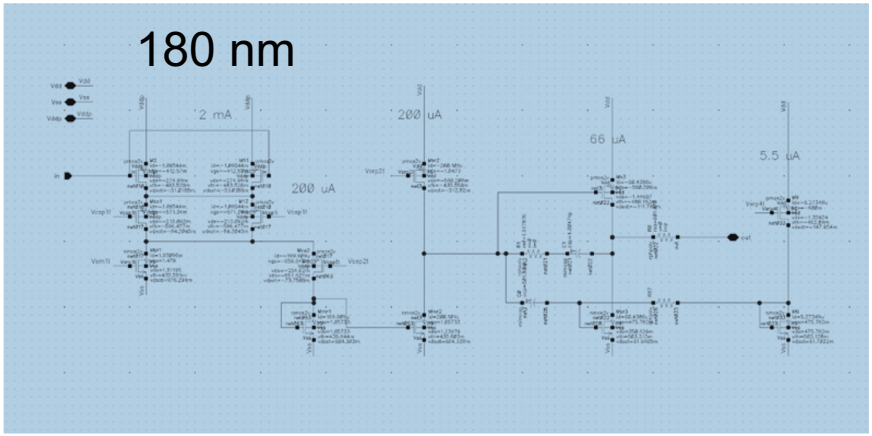
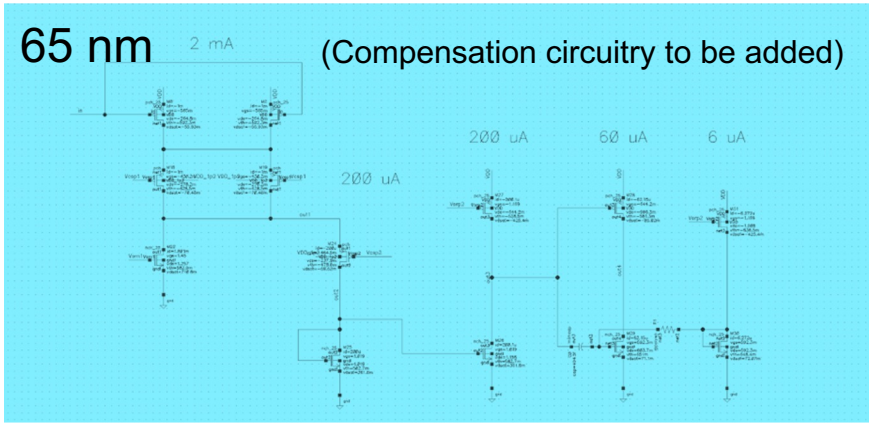
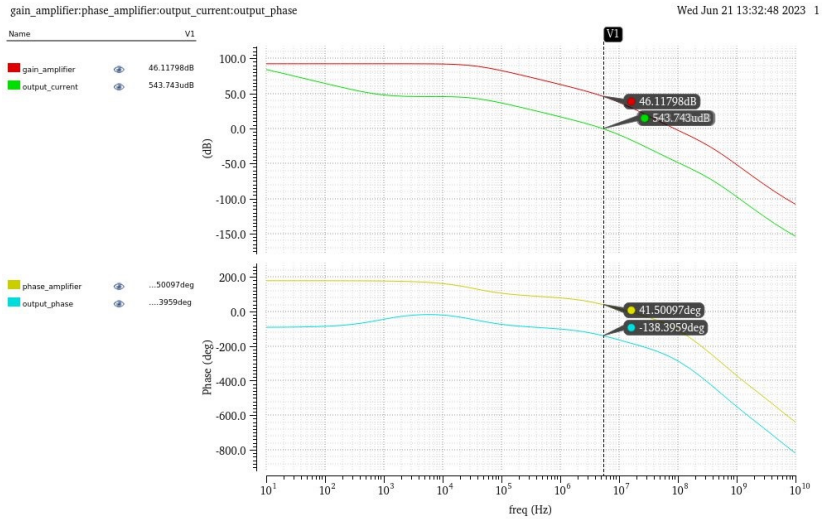
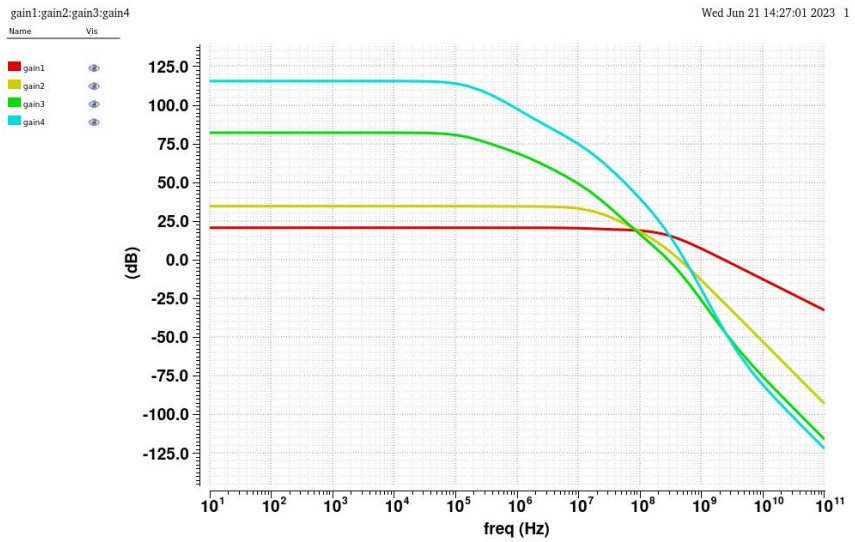
Ongoing 180nm to 65nm Mitigation









- Amp1 translated to 65 nm
- Designed for the same power budget
- Input capacitance maintained at 40-50 pF

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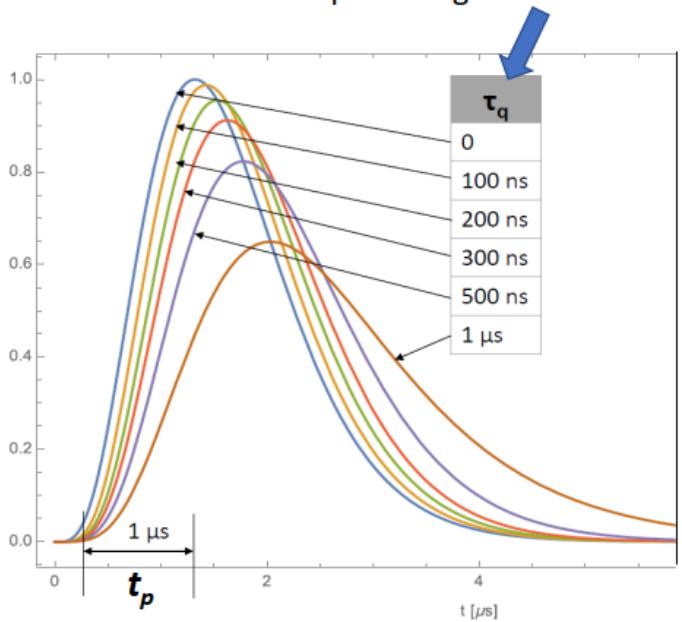
Summary

- **A *weak coupling* between the SiPM and input transistor is sufficient**, where ***Cd>>Cb>>Cg***. ***A charge sensitive amplifier (CSA)***, or a "voltage amplifier" is coupled to a SiPM parallel/series array by a decoupling capacitor only an order of magnitude larger than transistor capacitance, and independent of a much larger SiPM array capacitance **(*Cb*~200-500pF for a SiPM array of 10 nF, or even 100 nF).**
- The LAr FE ASIC has the required characteristics, and it made possible experimental verification of the noise calculations. Measurement results confirm calculation results and demonstrate that all the specifications can be met
- Extract the requirements of a new FE ASIC
  - **Synergies with Projects**
    - DUNE FD3&FD4 charge readout
      - 180nm fabrication for LArASIC was discontinued by TSMC
    - DUNE PD readout
    - PIONEER ATAR readout
    - future experiments, e.g. FCC-ee
  - With the support of BNL LDRD, evaluation of new FE ASIC design has started.
    - Initial simulation studies with 65nm process
- At BNL, we're planning with physics simulation as inputs to motivate the technical R&D, and will continue the development towards the FD3 PDS readout development.

Backups

Is SiPM design optimal for large Area Photo detectors?: The role of Quenching Time Constant τ_q (and quenching resistance)

SiPM quenching time constant



Long quenching time constant and short integration time makes the signal increasingly difficult to detect.

S/N with ES transformation by ***n***:

$$\left(\frac{S}{N}\right)_n = \frac{Q_{in}/C_d}{e_{sn}/t_p^{1/2}} \cdot \frac{n}{1 + C_g/C_b + n^2\, C_g/C_d}$$

Q_{in}= avalanche charge
C_d= capacitance of *all SiPMs in the array connected in parallel*
$C_g/C_d \approx 0.05$ for weak coupling (slide 18)
t_p= peaking ("integration") time of anti-aliasing filter
e_{sn}=noise spectral density of input transistor

xARAPUCA: single channel 1pe *S/N*=12.5 at ***n*=4, t_p=1us, t_q=100ns**

t_p	t_p =100ns	t_p =500ns	t_p =1µs
τ_q=100ns	Ball def=0.58 1pe S/N=2.9 SPTR=31ns	ball def=0.93 1pe S/N=9.4 SPTR=37ns	ball def=0.98 1pe S/N=12.5 SPTR=53ns

t_p	t_p =100ns	t_p =500ns	t_p =1µs
τ_q=500ns	ball def=0.2 1pe S/N=1 SPTR=110ns	ball def=0.58 1pe S/N=5.9 SPTR=76ns	ball def=0.77 1pe S/N=9.8 SPTR=81ns

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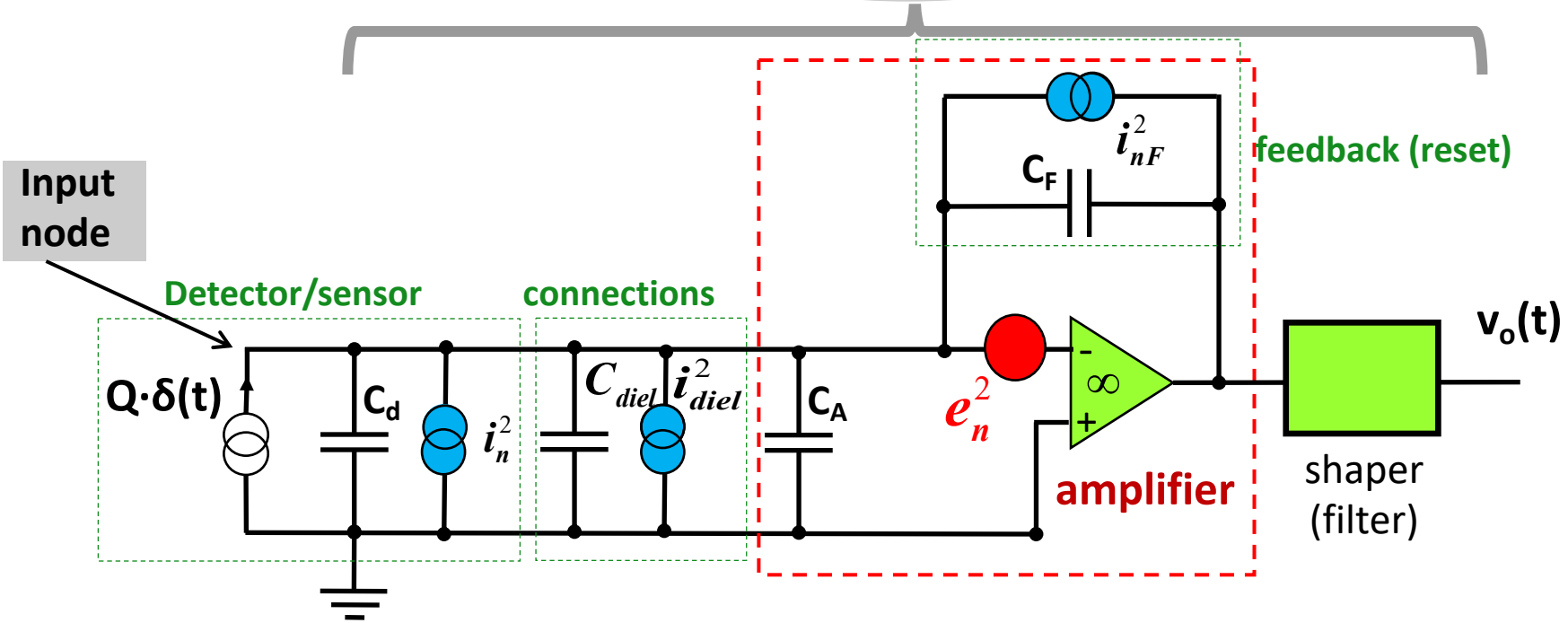
Noise Sources in Detector-Amplifier

Overall system processing function: $h(t); w(t); H(j\omega)$

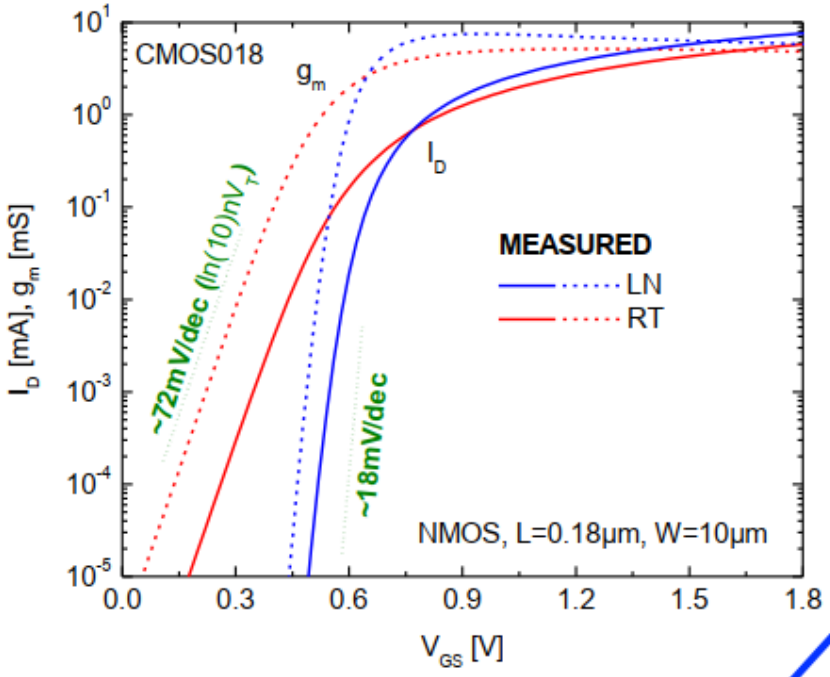


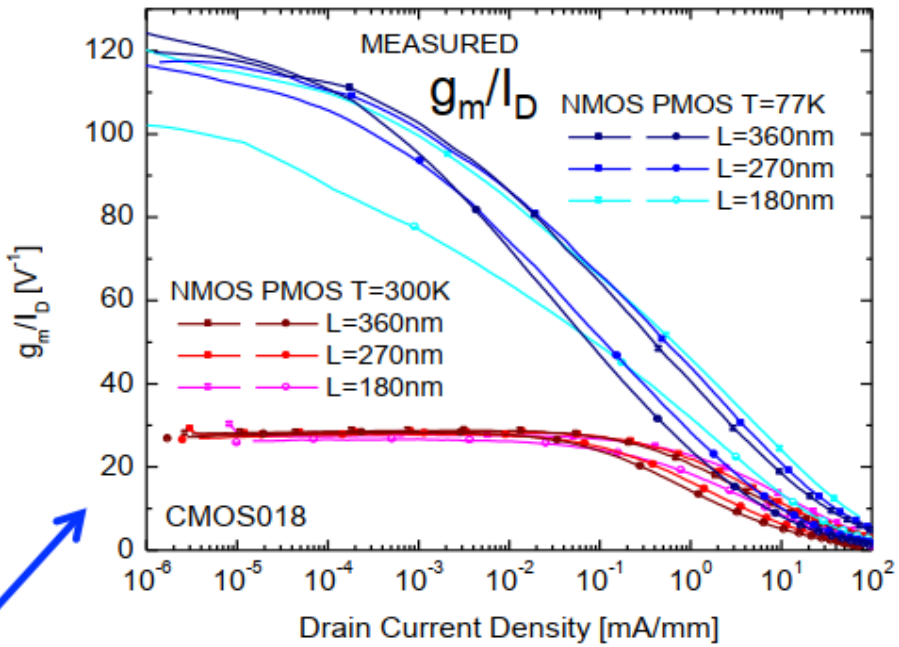
Dominant noise sources are from the components and circuits **directly connected to the input node**. Noise sources from the rest of the signal processing chain should be made negligible.

- i_n^2 arises in the sensor, e.g., from the leakage (dark) current; i_{nF}^2 may arise in feedback circuit
- i_{diel}^2 thermal fluctuations in dielectrics (dielectric loss noise)
- e_n^2 **noise associated with the input transistor:**

MOSFET gain: "*series white noise*"
trapping-detrapping: *1/f* eq. noise voltage generator in series

CMOS Characteristics in LAr





Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

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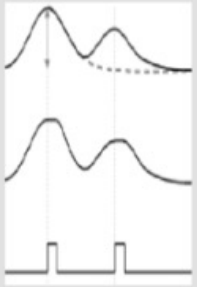
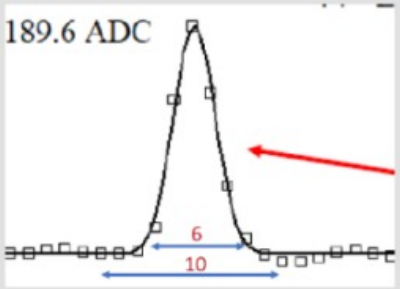
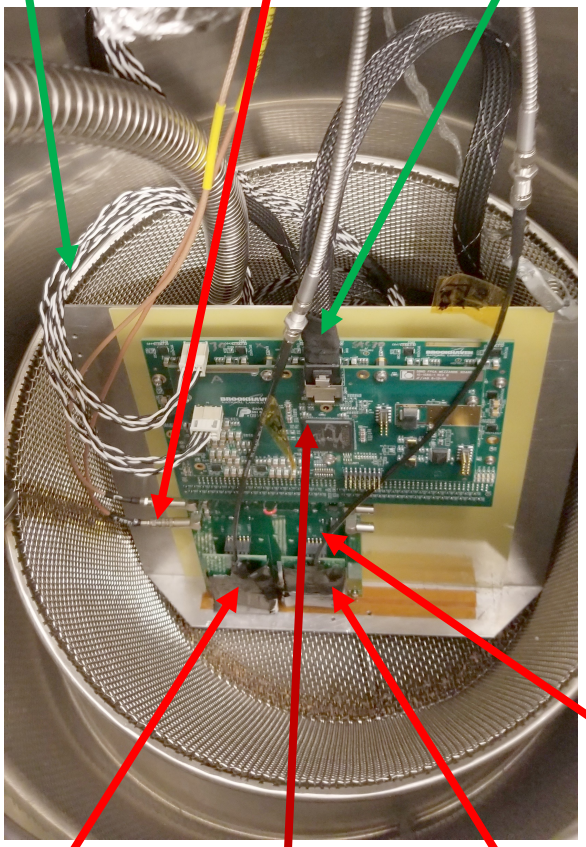
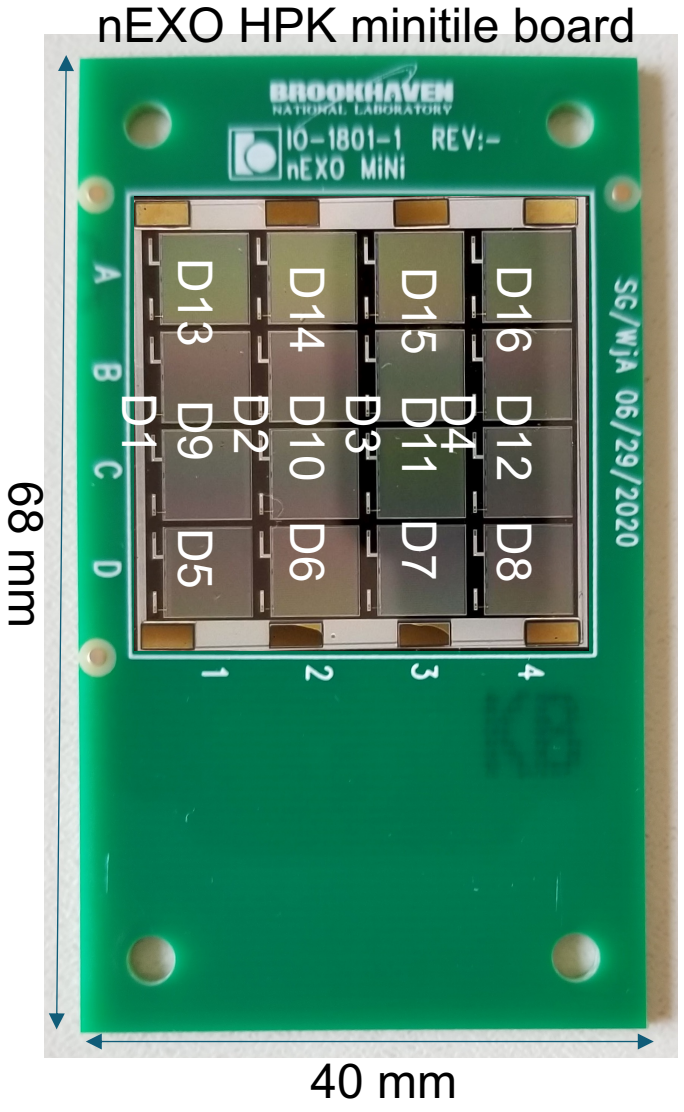
Readout Concepts

Readout scheme	1) Continuous waveform sampling and recording *"data streaming"*	2) Event driven peak sampling and timing *"data push"* (analog sensing)	3) Continuous sampling with event waveform "snippet" readout. *"data push"* (digital sensing)
Event sampling – sensing - recording illustration			
Data rate/tile (total event rate = ~ 4 x 10^3 s^{-1}/subarray)	12 x 16=192 b/(sample tile) **384 Mbps/tile**	**~ 1.536 Mbps/tile** **< 2 Mbps/tile**	Snippet [**20** samples] x event rate = 20 x event rate x 192 b= **≈ 16 Mbps/tile** For **32** samples snippet: **≈ 26 Mbps/tile**
Comments	Highest data rates. Most of the R&D and design studies so far have been devoted to this effort.	Peak sensing techniques well established. Does not provide waveform information.	Low data rate and low cable mass. Lower power dissipation

SiPM + LArASIC Test Stand at BNL





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