CMOS (LDO) Lifetime Testing

FD2-PDS Longevity qualification and Stability test Workshop

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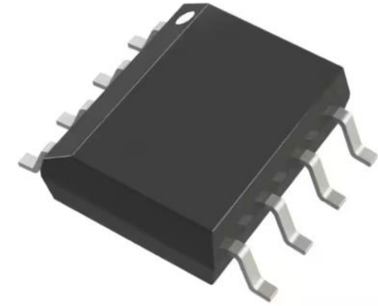
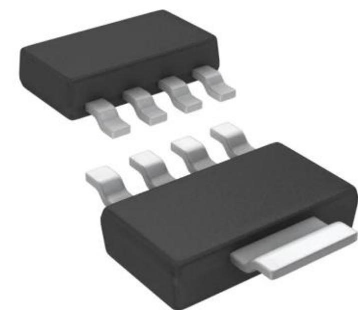
Motivation

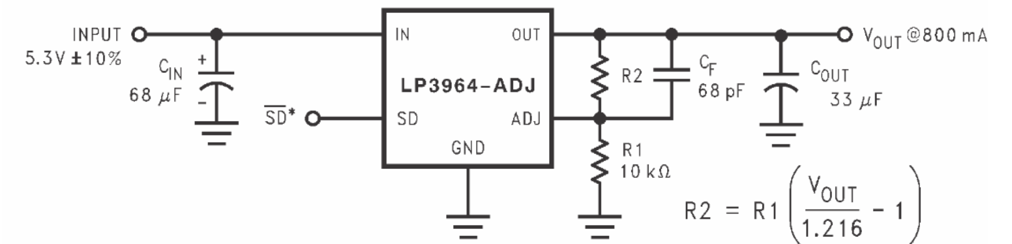
- 2 candidate LDOs identified by the FD2 PDS team to be used for cold electronics:
  - LP3964EMPX-ADJ
  - ADM7151ARDZ-04
- In order to fully understand the potential failure modes of the LDOs (due to the Hot Carrier Effect [HCE] during cryogenic use) a lifetime study be undertaken
- Accelerated aging will be induced by stressing the input voltage

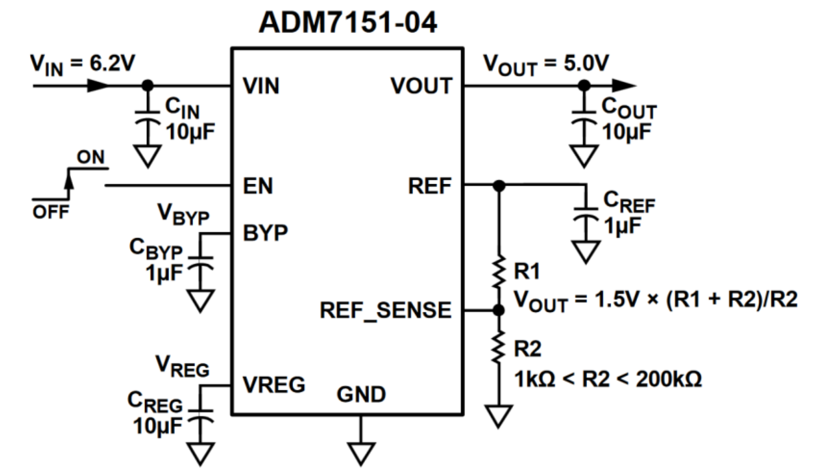




Defining parameters for aging

- We look to observe parameters of the chip that will age monotonically – for the commercial ADC in SBND, it was I_{VCC}
- For LP3964, we can only monitor V_{OUT}
- For ADM7151, we will also monitor V_{BYP} and V_{REG} in addition to V_{OUT}
- We will need to observe initial aging during the exploratory phase to properly define the parameters that will constitute a failure (e.g., one of these voltages rising or falling by 1%)





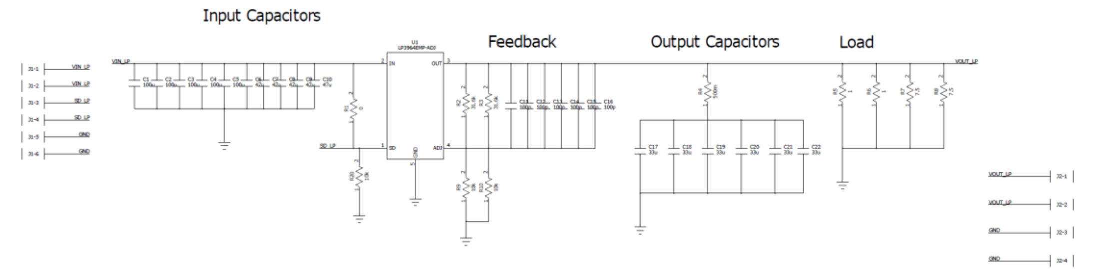
Inducing Aging

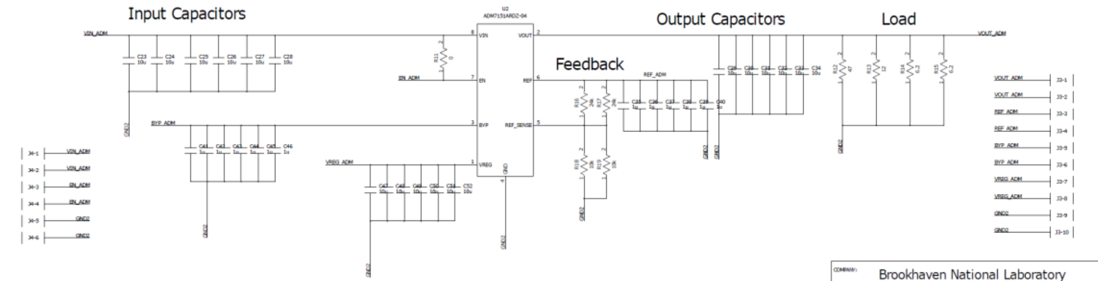
- Before testing, one has to define how much voltage stress will need to be applied
- To be prepared, we are using a Keithley 2460, capable of outputting 1A up to 100V with a 0.015% accuracy and 1 mV RMS

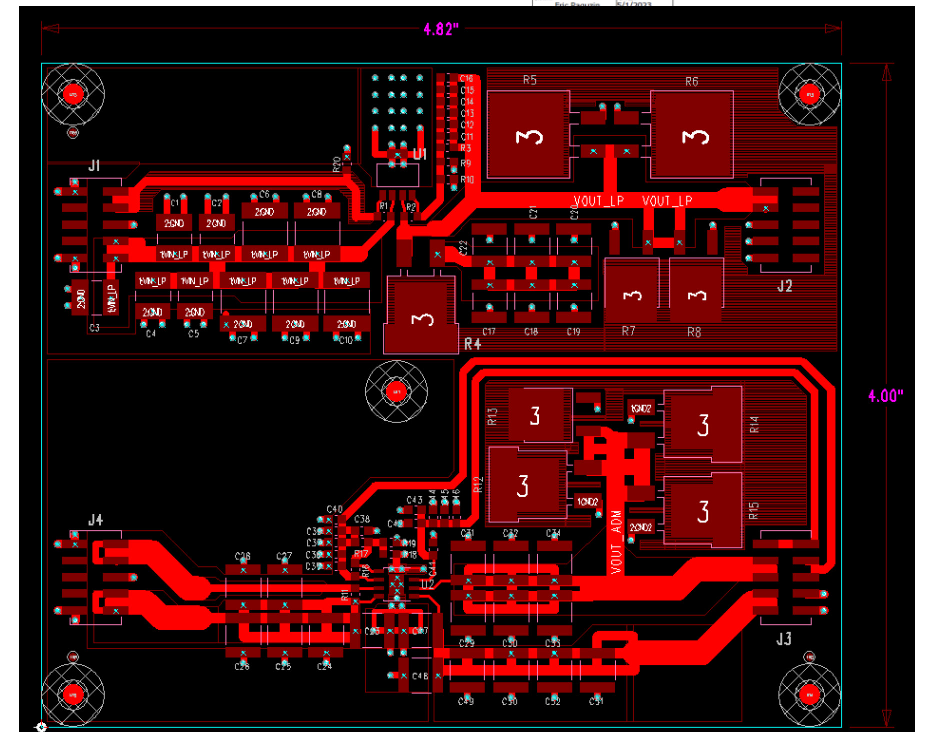
Parameter	Texas Instruments LP3964EMP-ADJ	Analog Devices ADM7151ARDZ-04
Input Voltage Range (Datasheet)	2.5V to 7V	4.5V to 16V
Highest voltage supply for stress test (assumed)	**14V**	**30V**
Output Current (datasheet)	800 mA	800 mA
Highest current supply for stress test (assumed)	**1A**	**1A**

Test PCB

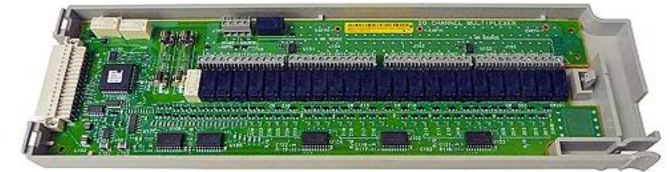
- Custom PCB designed to test both LDO candidates
- Separate ground planes so no interference
- Custom test PCB allows more capacitors in parallel for filtering and stability
  - Cold Electronics experience shows significant drop in capacitance at cryogenic temperatures
- Power resistors to sink 800 mA
- Standard connectors for input and output monitoring on board
- PCB is ordered and being fabricated







Monitoring

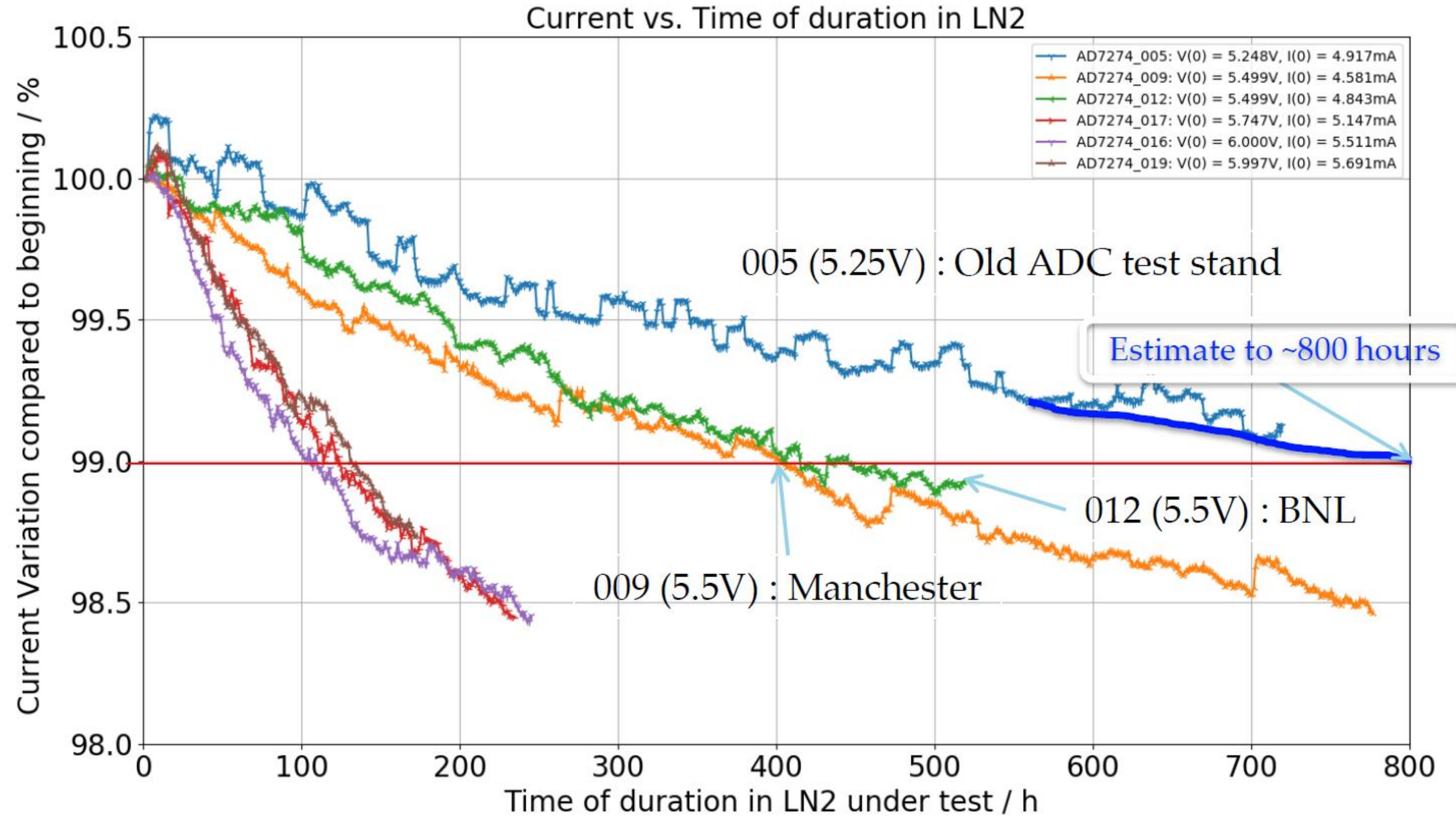


	Range [3]	Frequency, etc.	24 hour [2] 23 ± 1 °C	90 Day 23 ± 5 °C	1 Year 23 ± 5 °C	Temperature coefficient 0 – 18 °C, 28 - 55 °C
DC voltage						
	100.0000 mV		0.0030 + 0.0035	0.0040 + 0.0040	0.0050 + 0.0040	0.0005 + 0.0005
	1.000000 V		0.0020 + 0.0006	0.0030 + 0.0007	0.0040 + 0.0007	0.0005 + 0.0001
	10.00000 V		0.0015 + 0.0004	0.0020 + 0.0005	0.0035 + 0.0005	0.0005 + 0.0001
	100.0000 V		0.0020 + 0.0006	0.0035 + 0.0006	0.0045 + 0.0006	0.0005 + 0.0001
	300.000 V		0.0020 + 0.0020	0.0035 + 0.0030	0.0045 + 0.0030	0.0005 + 0.0003

- An Agilent/Keysight 34970 mainframe with Agilent/Keysight 34901A multiplexer module is being used to sample the outputs

Next steps

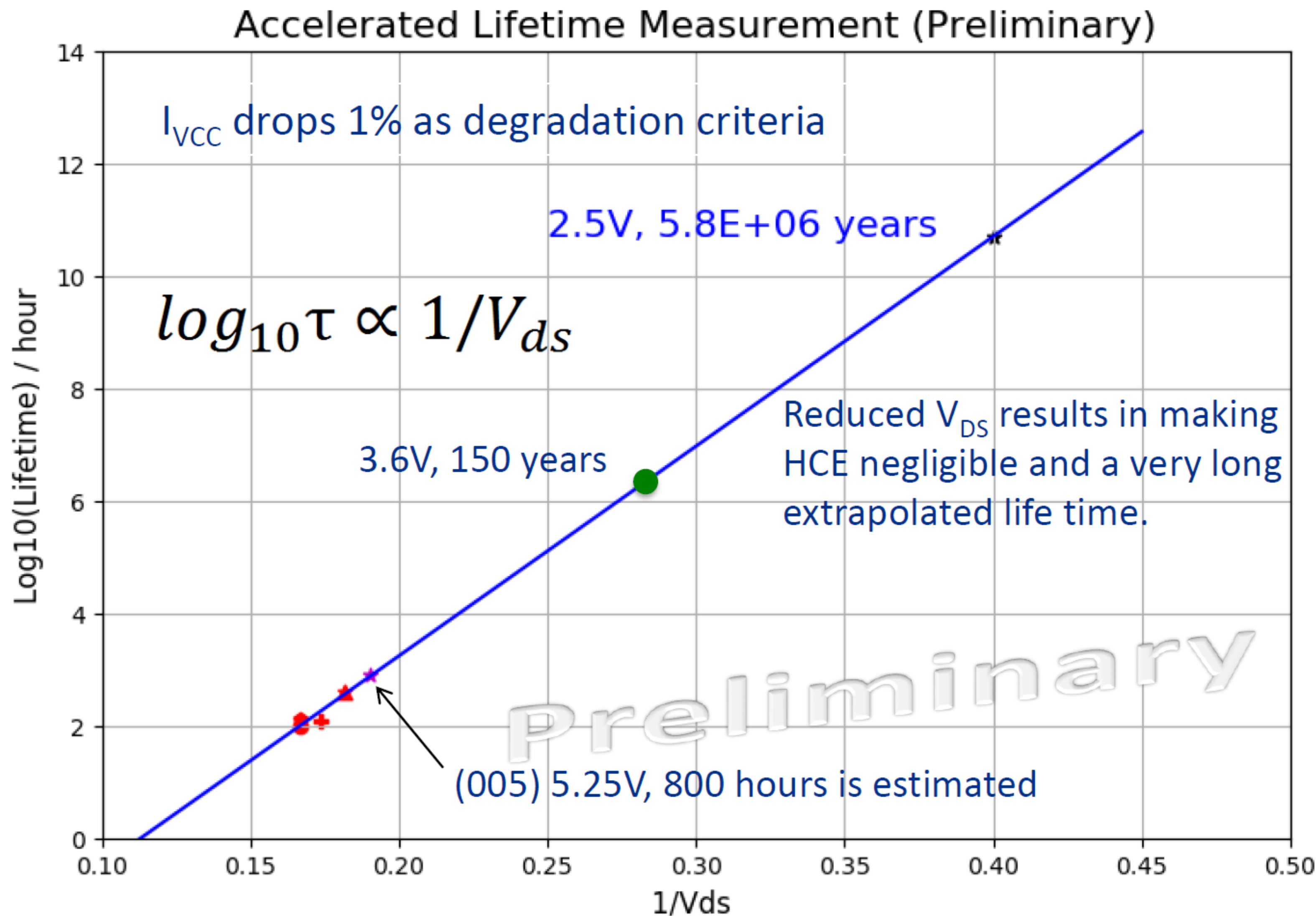
- When setup is fully built and testing begins, we can start overstressing the LDOs to get an indication for how long it takes them to fail
- Example shown to the right for ADC testing with various overstressed voltages



ADC Lifetime Projection

Goal

- With this data we will be able to predict the lifetime before HCE failure for each LDO for a given input voltage
- This will inform us the suitability of LDOs in long term cryogenic operation
- And inform our design (e.g. operating voltages) to ensure that HCE aging is a negligible issue



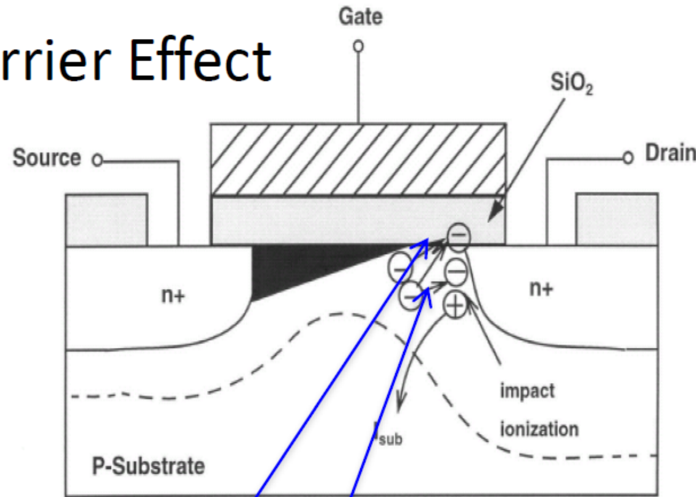
Backup

CMOS Lifetime at Cryogenic Temperatures

- Most of the major failure mechanisms are strongly temperature dependent and become negligible at cryogenic temperature
  - Such as electro-migration, stress migration, time-dependent dielectric breakdown and negative-bias temperature instability
- The degradation (aging) due to channel Hot Carrier Effects (HCE)
  - **The only remaining mechanism** that may affect the lifetime of CMOS devices at cryogenic temperature
  - Lifetime due to HCE aging
    - A limit defined by a chosen level of monotonic degradation
      - Drain current, transconductance, threshold voltage etc.
    - The aging mechanism does **not** result in **sudden device failure**
    - The device “fails” if a chosen parameter gets out of the specified circuit design range
- Reliability and aging are entirely different concepts

Basic on HCE and ALT

Hot Carrier Effect



→Some hot electronics exceed the energy required to create an electron-hole pair, resulting in ***impact ionization***

→ A very small fraction of hot electrons exceeds the energy required to create an ***interface state*** at the Si-SiO2 interface

→ Due to the generation of interface states, negative charges will accumulate causing the degradation

→ More severe at cold than at RT

Accelerated Lifetime Test

CMOS in DC operation

→ ALT at any temperature (well-established by foundries) transistor is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation to a practically observable range.

→ ALT is widely used by industry

→ Lifetime is projected by empirical equation

$$log_{10}\tau \propto 1/V_{ds}$$

CMOS in AC operation

→ Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $4/(f_{clock}*t_{rise})$ compared to dc operation. This factor is large (>100) for deep submicron technology and clock frequency needed for TPC

A Little More Explanation of CMOS HCE Lifetime (Aging)

- Reliability and aging are entirely different
  - The Reliability is dependent on the system design, choice of components, assembly techniques, and in general, by the QA/QC in the work place.
    - M. White and J.B. Bernstein, "*Microelectronics Reliability: Physics-of - Failure Based Modeling and Lifetime Evaluation*", JPL Publication 08-5 2/08
- HCE aging is given by the physical/chemical processes
  - It can be controlled only by the design and the operating conditions
  - It does not result in sudden failure
    - The device "fails" if a chosen parameter gets out of the specified circuit design range
  - It is uniform and reproducible
- **The cold electronics for LAr TPCs** should be designed for a lifetime one or more orders of magnitude longer than the required service life (e.g., > 300 years for DUNE), essentially to **remain outside of the region of HCE degradation**