DMEM and HD cold amp

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For the HD cold amp + DMEM + membrane electronics designers

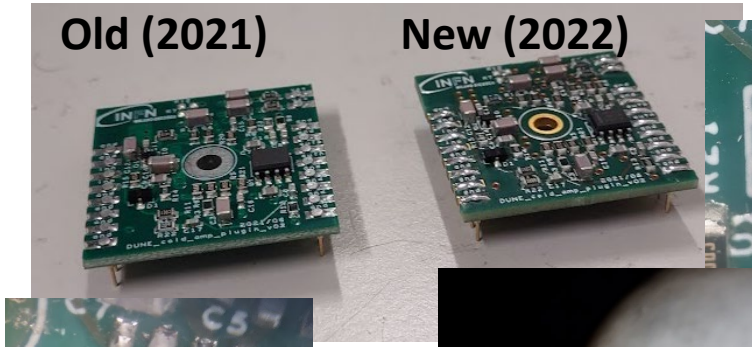
DMEM + HD cold amp

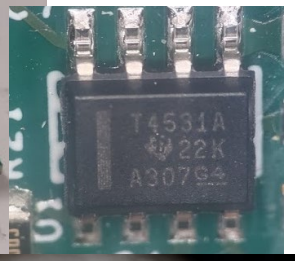
DMEM 1.0 4-channel motherboard designed at FNAL EDMS 2795424

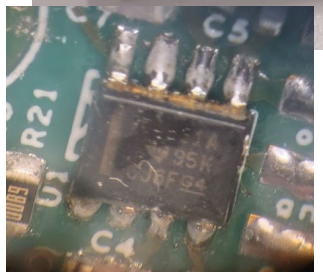
- 10 produced in 2022
- **3@CERN** (2 in module-0 + 1 in cold box), **4@MiB, 1@CIEMAT, 1@Naples(soon)**
- Changes w.r.t. EDMS schematic: Rf=1.2k instead of 2k (2 resistors per channel)
- Change will be propagated to all boards (except M1 M2 in module 0)

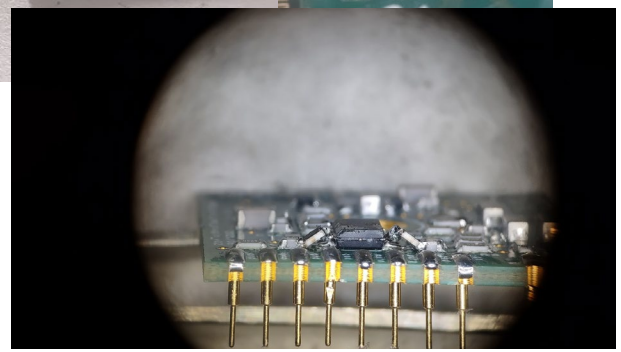
HD-style amplifiers: same as horizontal drift EDMS 2805804

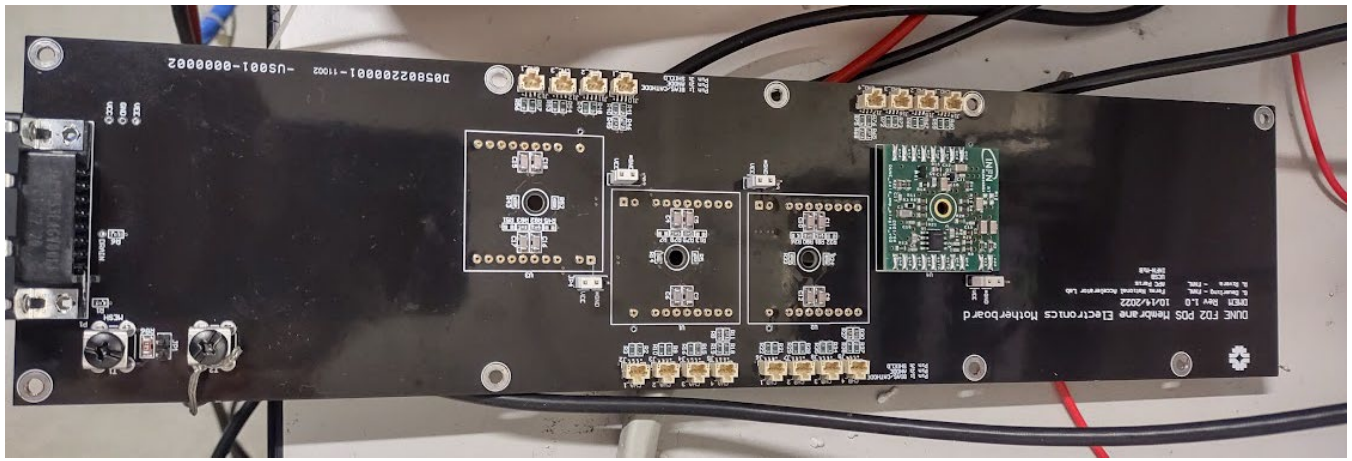
- **8(new)@MiB** (of which 4 in use), **≈15(old)@CIEMAT**, a **few(?)@CERN** (not all in use)
- 50 ohm resistors must be added in series with the THS4531 outputs to prevent instabilities with large (>390 ohm) feedback resistors; likely not necessary with old amplifiers (old batch of THS4531)







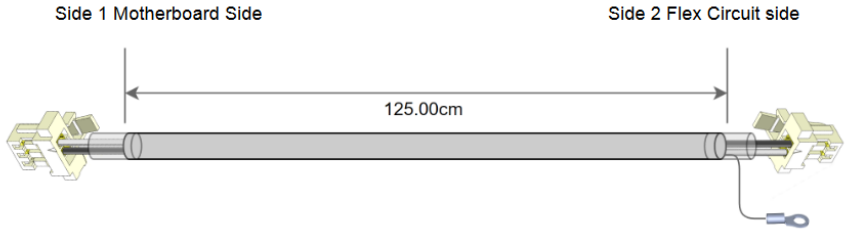




Cables

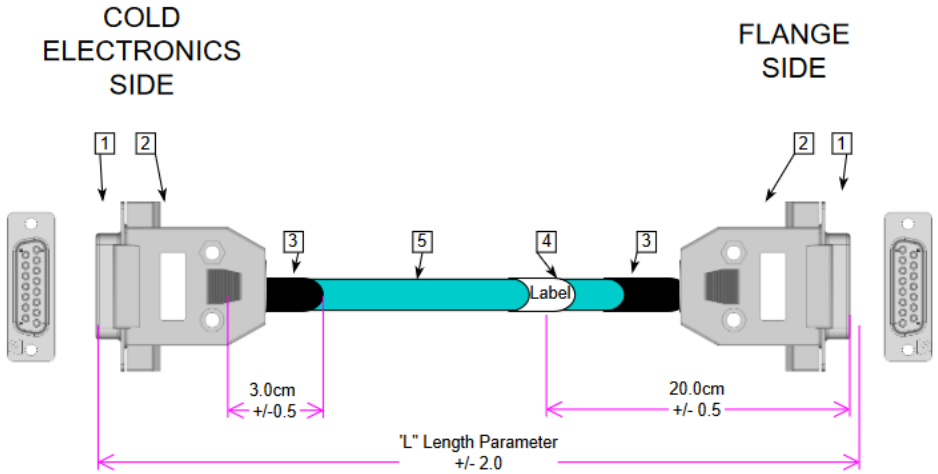
Between flex and DMEM: EDMS 2815448

- White «coaxial» cables (actually 2 conductors + shielding), about 1m long
- Made/ordered by FNAL



Between DMEM and warm (through flange): EDMS 2815464

- Blue superior essex cable (same as HD)
- DSUB15 connectors at both ends (differs from HD)
- Cold side (DMEM to flange): female/female
- Warm side (flange to DAPHNE): female/male



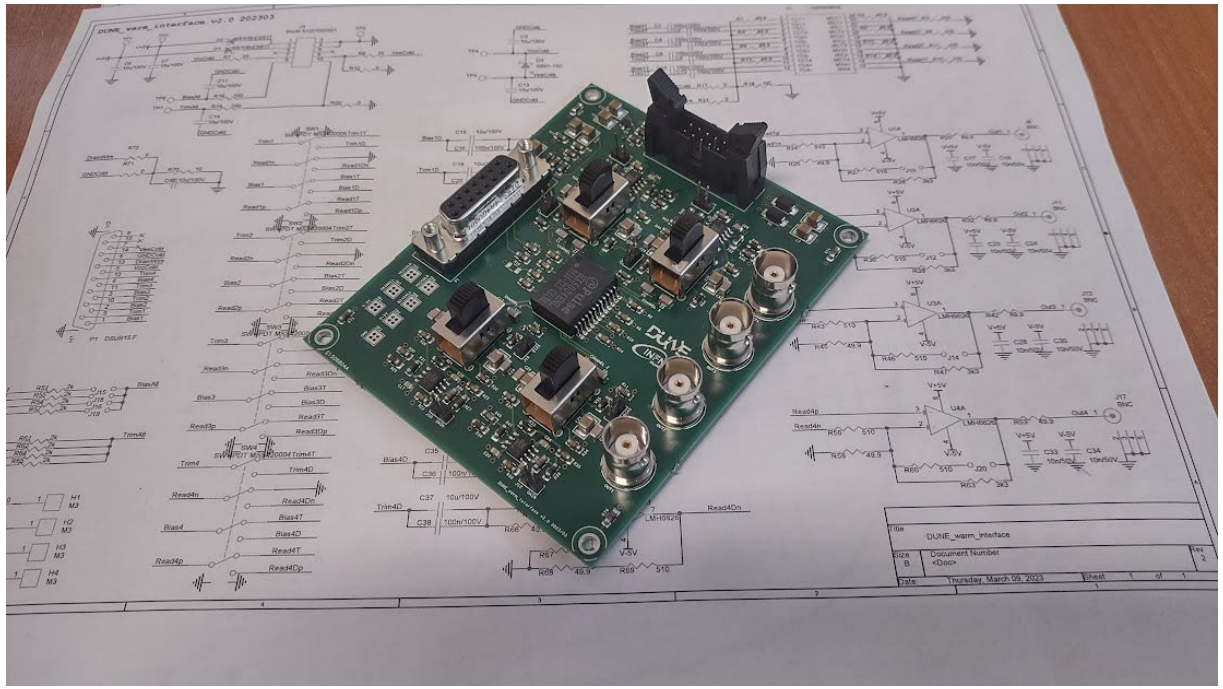
NIOBE-VD flange: EDMS 2802472

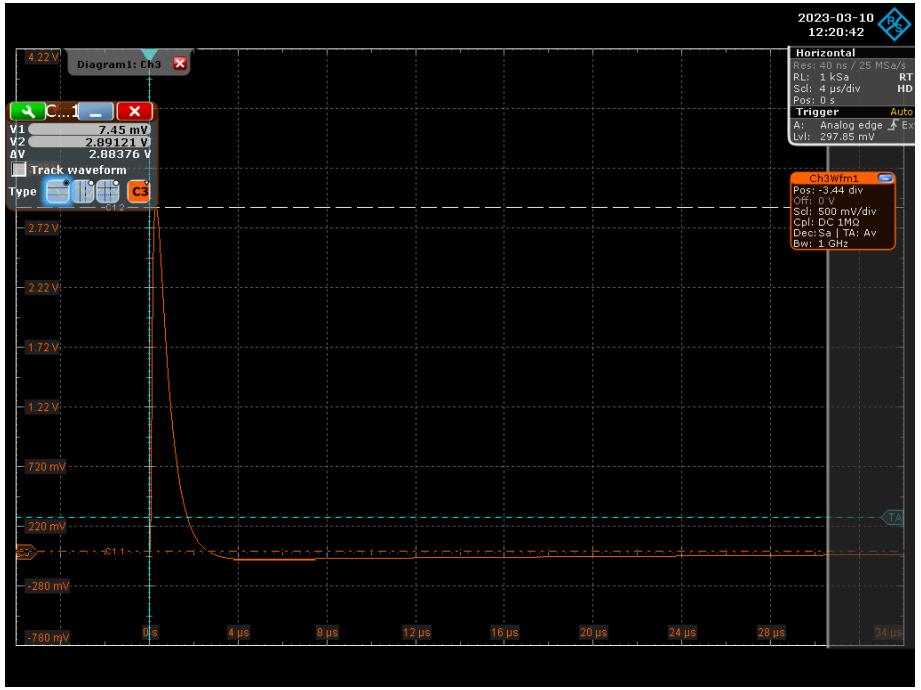
- Male DSUB15 connectors on both sides
- Designed by Jon Ameel (UMich), in use at CERN

Warm second stage v2

- Interface between DMEM and oscilloscope
- Not needed if DAPHNE is used
- 10 populated boards received last Monday, to be tested
- Design updated from first version
- Two options, selectable with a switch on each channel:
  - Transformer as DAPHNE v3 (undershoot ≈8%)
  - Transformer bypassed, AC coupled w large caps (undershoot ≈3%)

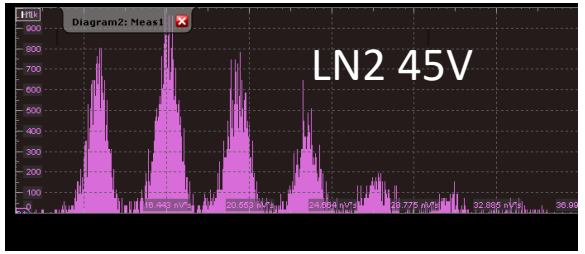
  (smaller undershoot amplitude means that the tail lasts for longer. In any case the integral of the entire signal has to be zero)



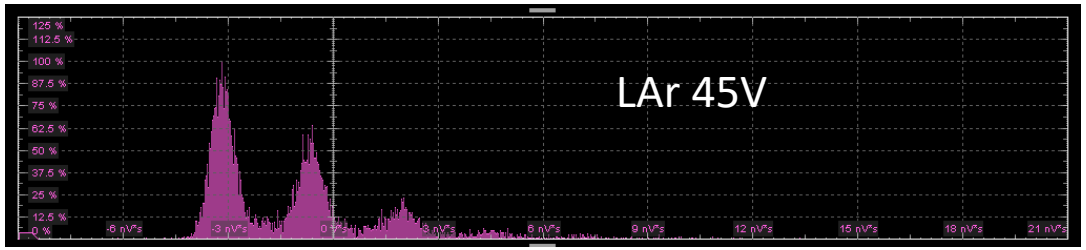


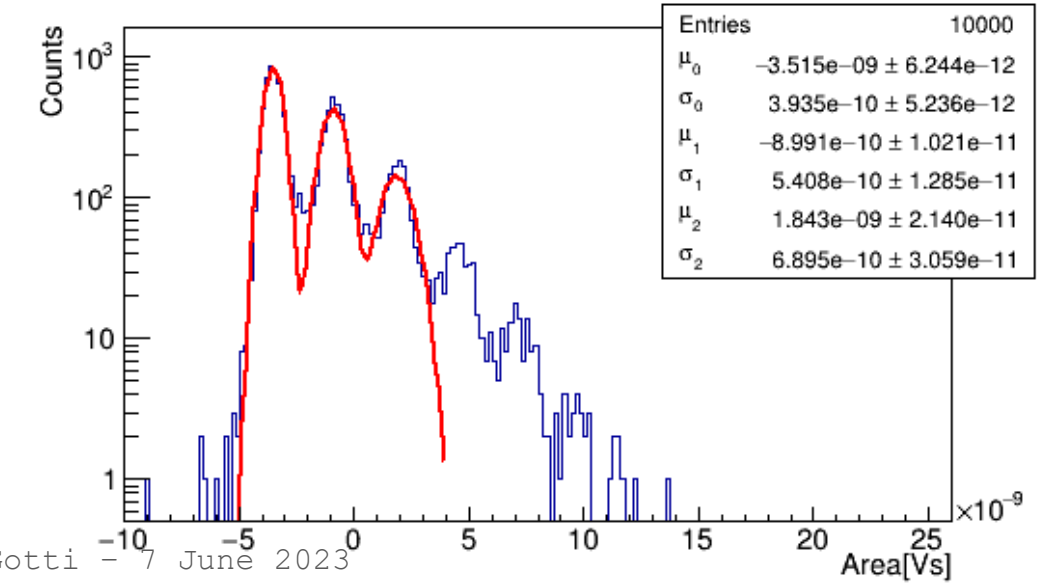
Measured S/N

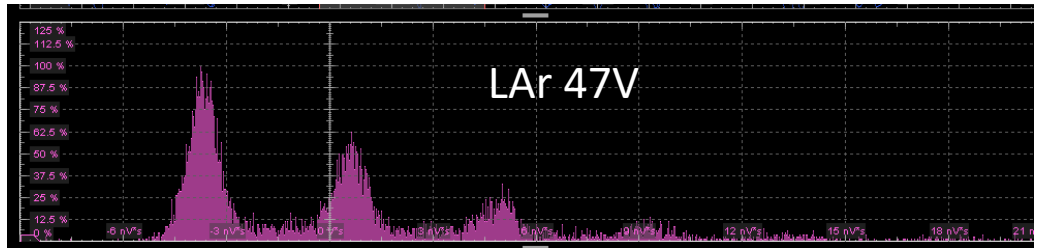
- In the lab @MiB:
  S/N≈8 with HPK SiPMs at 45V in LN2 (+3Vov)

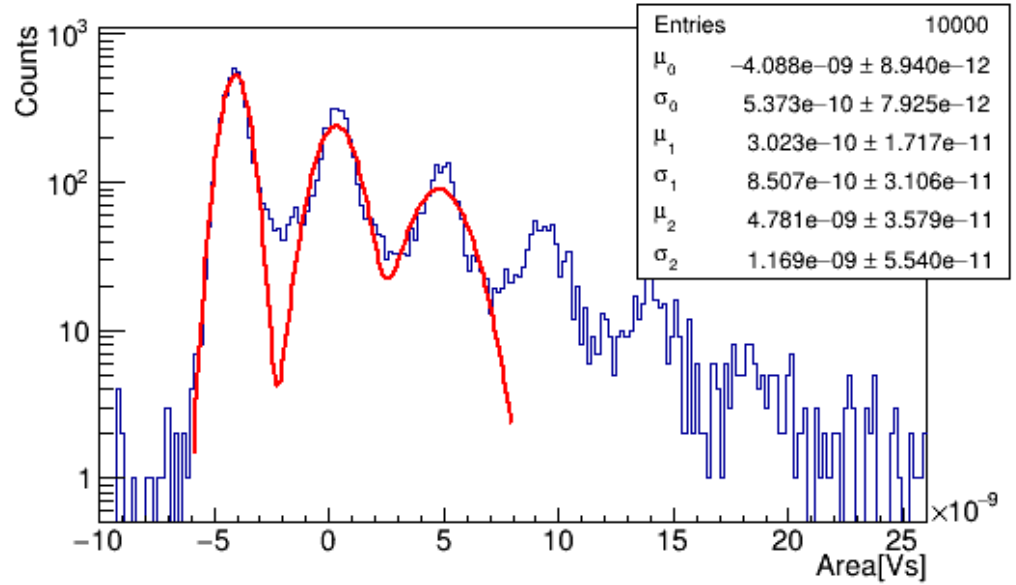


- At the march cold box:
  S/N≈6.7 with HPK SiPMs at 45V in LAr (+2.5Vov)
  S/N≈8.2 with HPK SiPMs at 47V in LAr (+4.5Vov)









Plans for the near future

- The last configuration tested in the March cold box is still the one to use in future tests
  (Same as installed in Module-0 M3+M4)
- Tests with ARAPUCA+DMEM are planned to happen soon in Madrid and Naples,
  which will also validate the electronics further
- Production of additional boards should not be needed before Module-1

- Long term reliability has already been covered for FD1 and passed the FD1 FDR EDMS 2847126
- Only difference is the presence of 47uF X7R capacitors on the DMEM, not used in FD1, but used in the DCEM