MicroTCA for HCAL and CMS

Review / Status

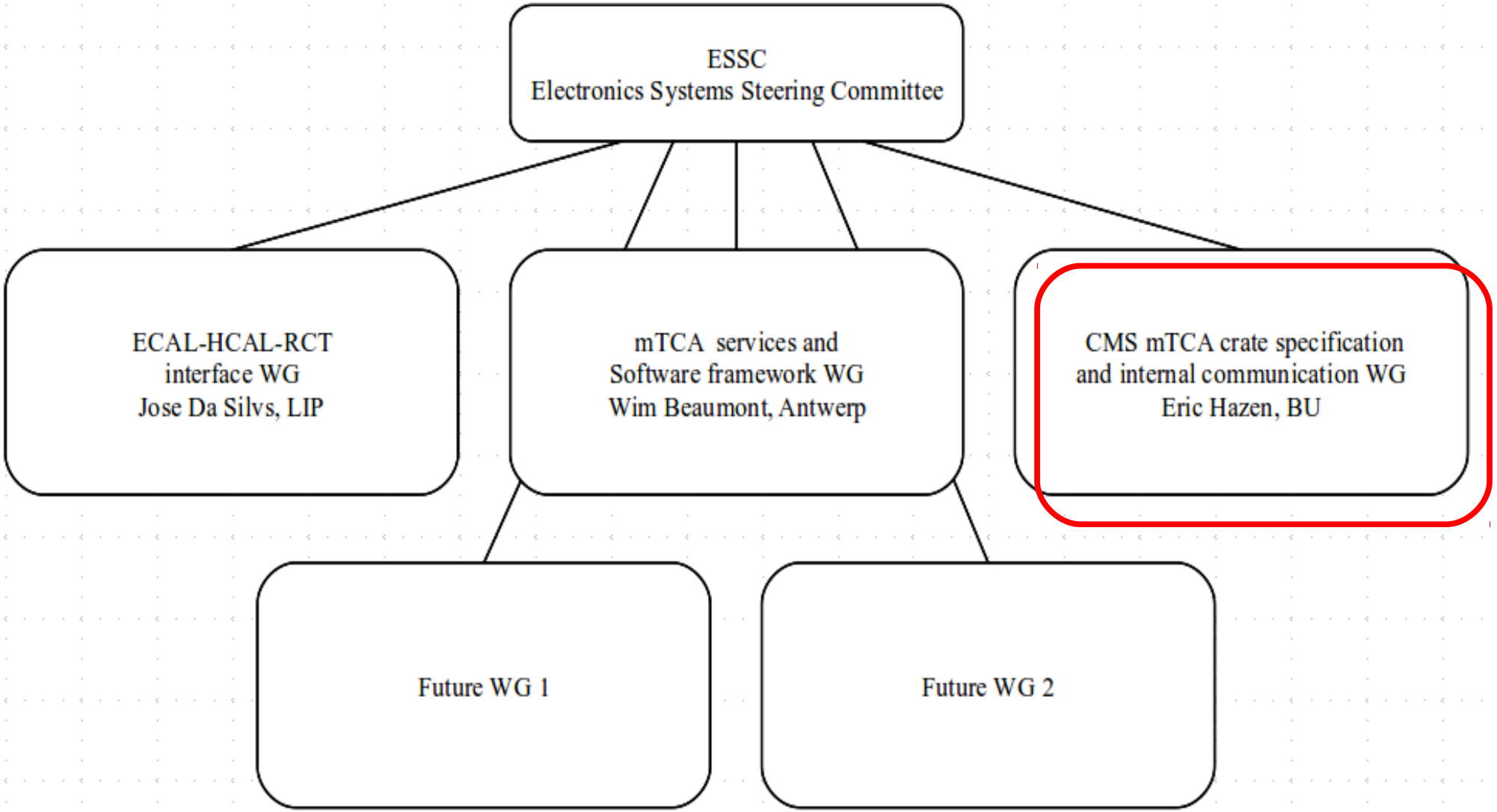
E. Hazen - Boston University
for the CMS Collaboration

Outline

- MicroTCA common platform working group
- The AMC13 project
- DAQ upgrade interface – hardware aspects

CMS MicroTCA Common Platform Working Group

Boxes

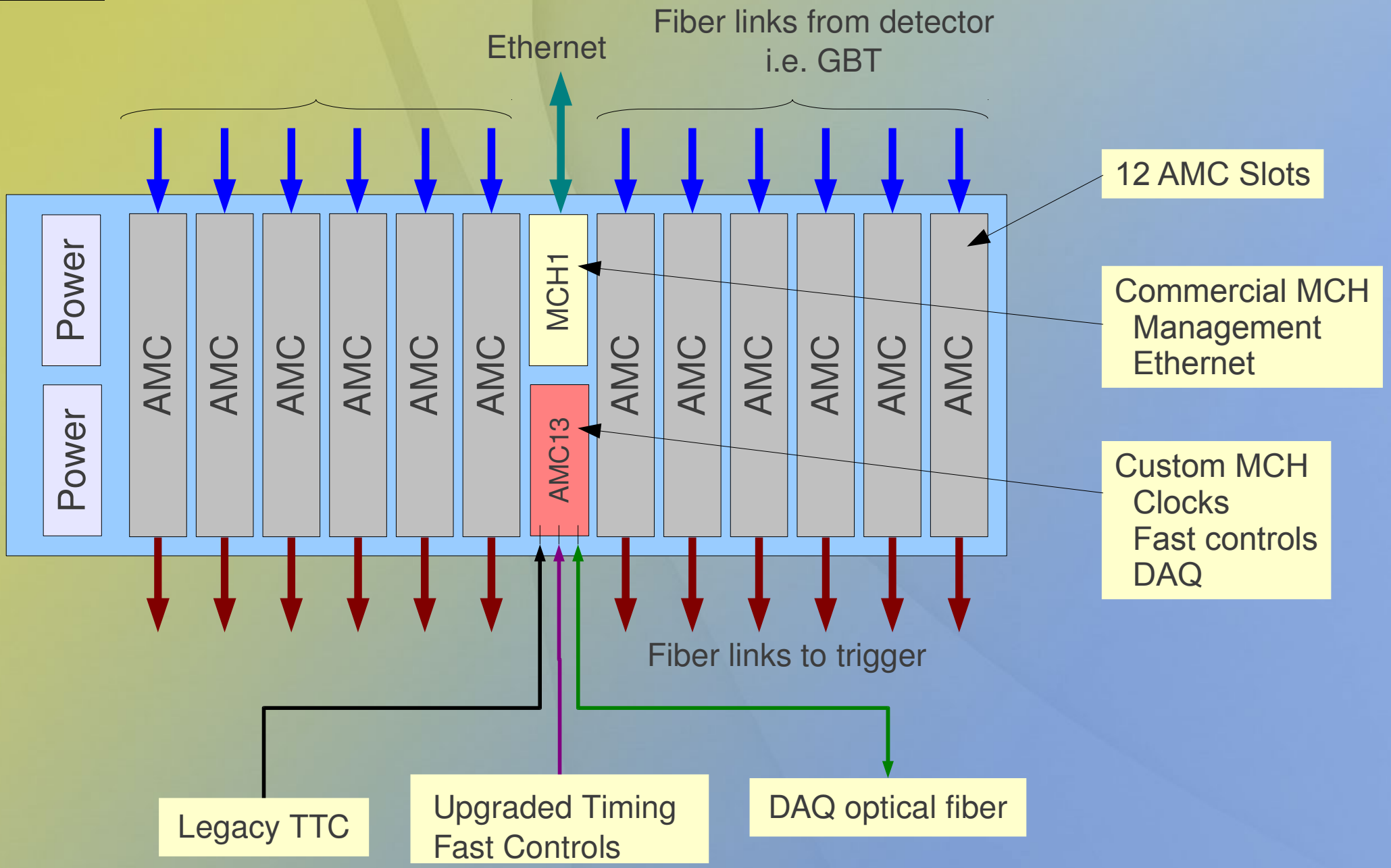


M. Hansen, CERN. magnus.hansen@cern.ch

uTCA Common Platform WG
(convened by me at Magnus' request)

- Included in scope of this WG
  - Backplane connectivity (port connections)
  - Protocols on common ports (TTC / TTS / DAQ)
  - Crate and MCH specification
  - Power supplies
  - Guidelines for AMC designers
- Not in scope
  - Implementation of MMC, GbE on AMCs and MCH

CMS uTCA Readout Crate (i.e. HCAL)



Draft document
Under review by WG

See full text at link below for details

CMS MicroTCA crate concepts & AMC card requirements.

Gregory Iles, Magnus Hansen and Eric Hazen
30 November 2010 Version 0.8 (Draft)

1 General concepts

This document describes a proposed CMS-specific configuration of a MicroTCA crate. It describes requirements for crate mechanics, backplane interconnections and some prescriptions for signal protocols on a few of the interconnections. It does not describe any software requirements, nor prescribe any particular implementation except as examples.

We have chosen to explore MicroTCA as a crate system to replace VME for the next generation of electronics cards inside the CMS experiment at CERN. MicroTCA offers a flexible, high density, high performance backplane that is based on the serial standards in use today (GbE, PCIe, SRIO, SATA, etc). It is relatively inexpensive for both the card manufacture and the customisation of the backplane if required.

MicroTCA is based on the AMC (Advanced Mezzanine Card) standard developed by the PICMG group for ATCA cards. Up to 12 AMC cards can be inserted directly into a MicroTCA backplane. A MCH (MicroTCA Carrier Hub) provides connectivity between slots, although direct connections between slots are also allowed. The system can operate in redundant mode with a second MCH (MCH2) connected to each AMC card and to the primary MCH (MCH1). For CMS we focus exclusively on this redundant type of "dual star" crate.

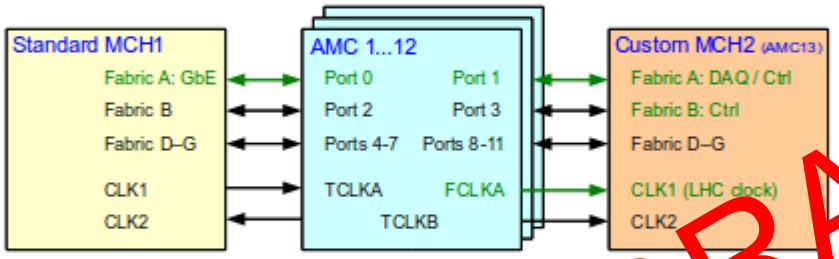


Illustration 1: Typical "Dual-Star" MicroTCA Backplane.
Note that each interconnection shown represents a "star" connection from each MCH to up to 12 AMCs. The Fabric connections are bidirectional (one pair each direction).

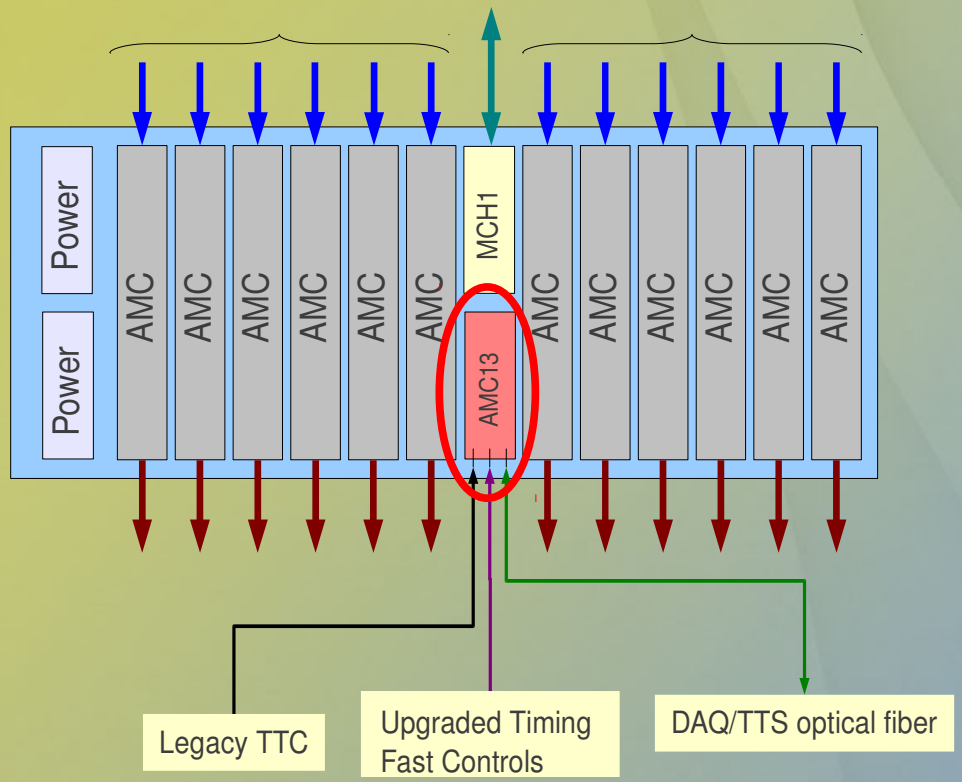
Illustration 1 shows a simplified view of the dual-star configuration. The of the

DRAFT

https://twiki.cern.ch/twiki/bin/view/CMS/MicroTCA

The AMC13 Project

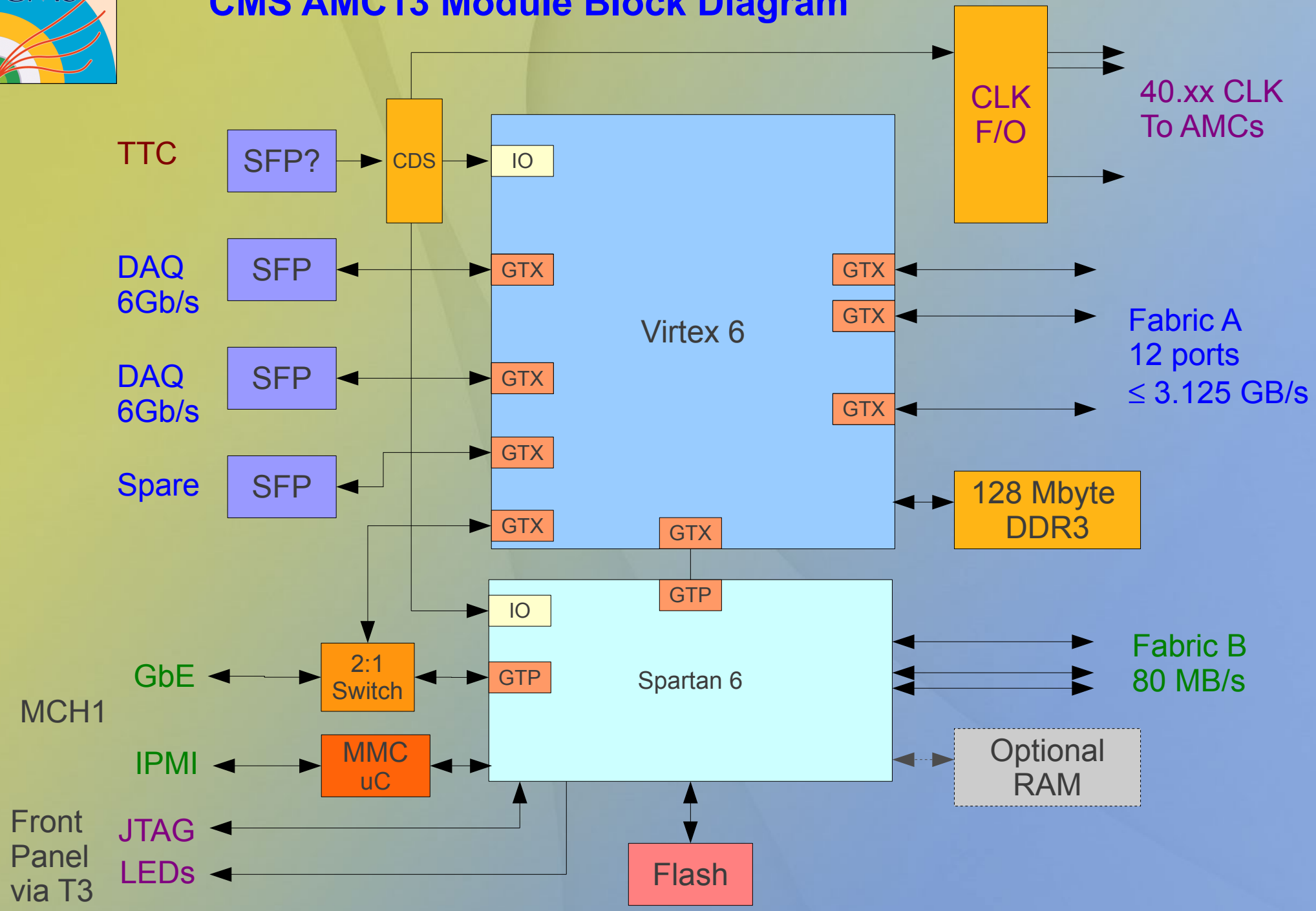
AMC13 Overview



- Proposed for CMS-wide use in all MicroTCA crates which require these services
  - Distributes LHC clock and TTC to AMCs
  - Harvests DAQ data from AMCs
  - Provides interface to CMS-wide systems
    - DAQ, TTC, TTS
- No role in DCS foreseen
- Design underway at Boston Univ.

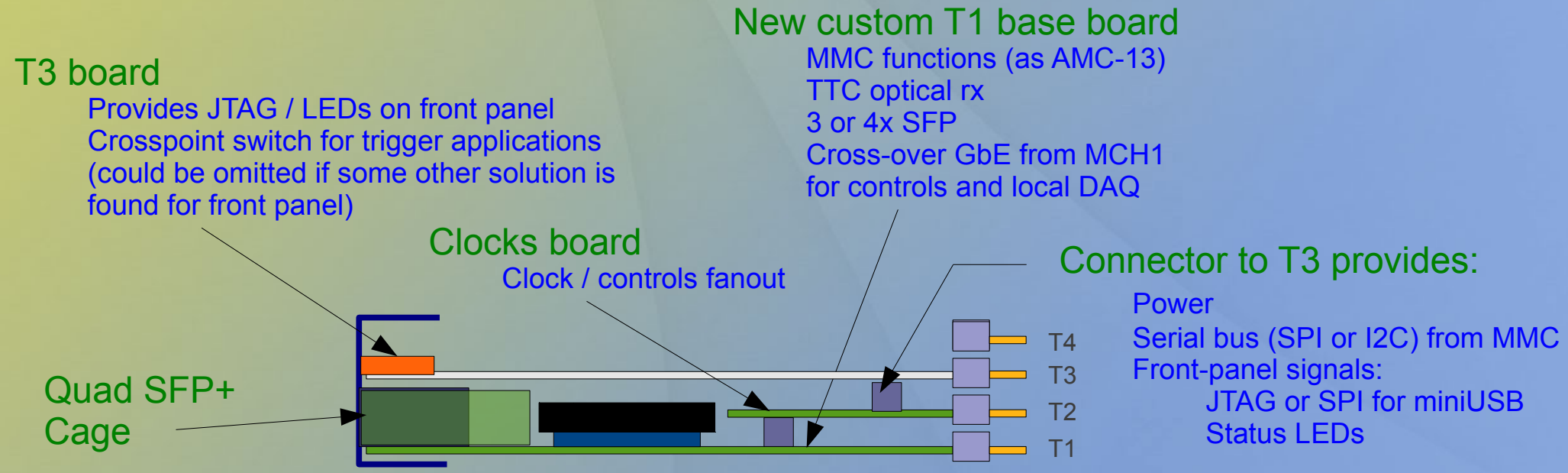
Called “AMC13” because it behaves more like a 13th AMC than an MCH from crate management perspective

CMS AMC13 Module Block Diagram



AMC13 Board Stack

- Base configuration has only tongues 1, 2
- Base board - With optics and HS links (Fabric A)
- Clocks board - distributes LHC clock and controls
- Mezzanine connector for T3 with I2C
  - T3 has JTAG and LEDs



AMC13 Status

- Schematic design complete
- Layout underway – expect prototypes in June 2011
  - Current plan is to produce ~ 10 prototypes
- Expected users so far are:
  - HCAL
  - Calo Trigger
  - Global Trigger

DAQ Interface

DAQ 2013-2014

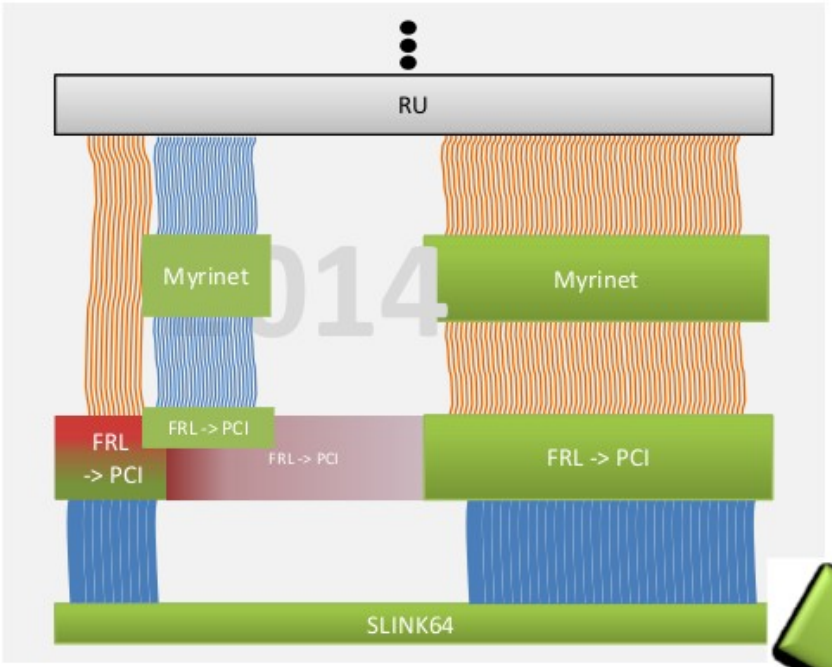
Remarks and draft proposal

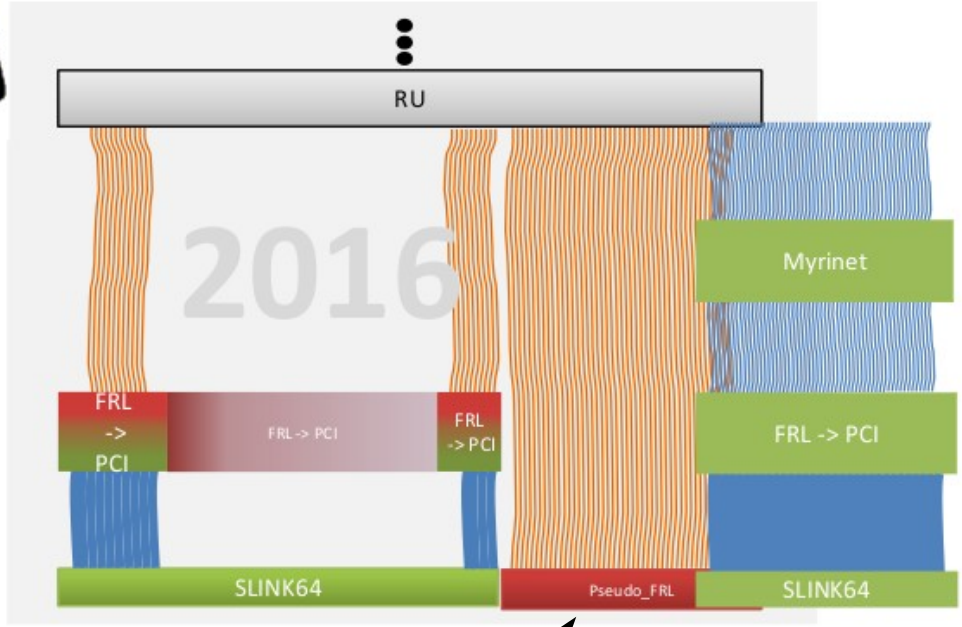
- Recent visits in false floors shows that any new installation will be very difficult and time consuming but nothing is impossible. We must consider to install new cable trays on top of racks
- Our custom hardware (S-link, FRL, FMM) shows to be very reliable so far but will start to fail one day ! Keep them as long as possible and be ready to change when wear out times come
- S-link alone is moving currently 400 MB/s and can be pushed to 480 MB/s if needed
- The way Myrinet is used in our system constitutes the 250 MB/s limitation and especially forces us to stay with obsolete PCI-X based servers.

- Elaborate an upgrade plan that :
  - Minimizes the work in cable trays
  - Allow the progressive removal of the current D2S when needed (schedule or failure driven)
  - Keep as much as possible existing custom hardware (produce additional spares in view of operation till 2020)
  - Allow the cohabitation of old and new D2S
- The proposal is :
  - to keep everything from FED to FRL "asis"
  - design a new card that replaces the Myrinet NIC sitting on the FRL.
  - All FRLs are recabled to use the 2 copper inputs (400-500 MB/s today, 800-1000MB/s max)
  - FRL output is a single fiber@8Gb/s connected to a custom PCIe multi FRL receiver hosted by a server (possibilities to re-use existing Myrinet patch cords if servers stays downstairs)
  - Server acts as a FED builder and sends the super fragment to upstairs RUs via commercial 10GbE links
  - In the future, New NIC can be reformated in order to replace VME transition cards and hence free up spares
  - Use HCAL case to embed our sender design into their MCH. If not possible, HCAL has to provide S-link adapters
- All details in Dominique's slides...

March 10, 2011 Attila and Dominique 4

"Use HCAL case to embed our sender design into their MCH. If not possible, HCAL has to provide S-link adapters"





HCAL is the first to go this route...

DAQ Upgrade

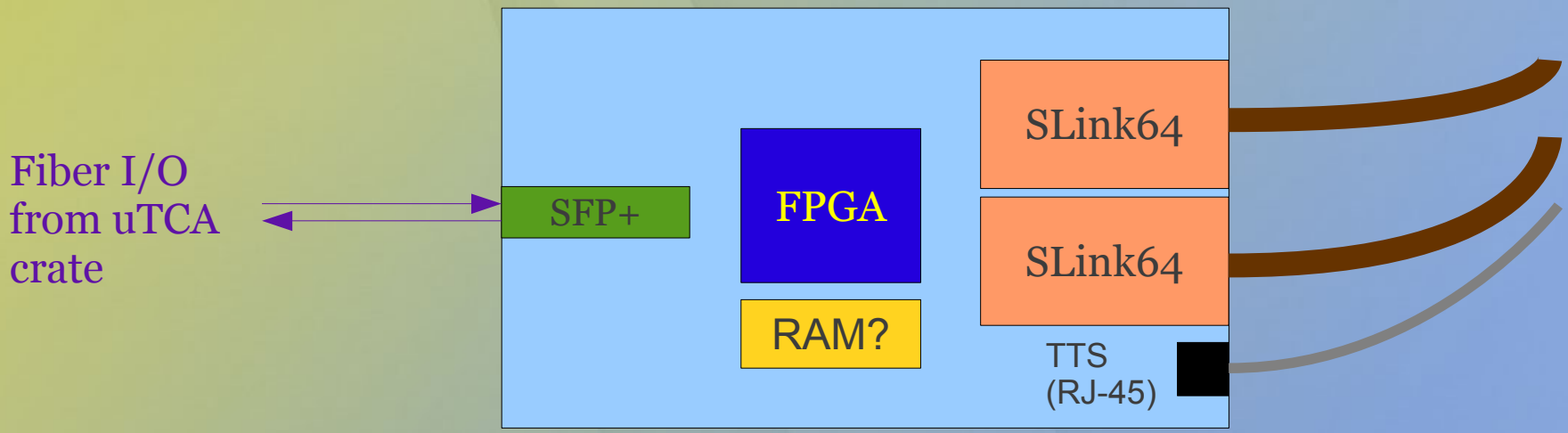
- FRL will eventually be replaced by Fiber… the question is when, and what protocol

- Two options for 2014 operation
  1) DAQ group provides protocol or IP for fiber link
     - We must integrate DAQ sender in AMC13 firmware
  2) DAQ group provides new S-Link64 sender
     - We must design an adapter module

Legacy DAQ Adapter

Basic Requirements:

- Fiber link capable of ~6 Gbit/sec (bidirectional)
- One or two S-Link64 sender card sites
- One or two RJ-45 TTS connectors (LVDS)
- Capable of (burst) operation up to 320 MBytes/sec per S-Link64



Packaging and implementation not constrained, could be MicroTCA module, VME or other.

Backup Slides

Common MicroTCA Platform Details

Requirements Summary

- Commercial MCH1 for crate management, GbE communication, and other user features as desired
- Custom MCH2 providing:
  - LHC 40.xx MHz low-jitter clock distribution
  - Fixed-latency controls distribution (aka TTC)
  - DAQ functionality; readout of data from AMCs
  - Buffer management communications for TTS-like functions as well as possible selective readout control
- Approved crates with the following features:
  - 12 full-height double-width AMC slots
  - Two standard (single-width) MCH slots
  - JTAG access to all modules via JSM
  - Approved power modules with 12V bulk input (? voltage T.B.D.)
  - Vertical airflow for cooling
- Backplane with the following interconnections:
  - Dual-star routing of Fabrics A, B, D, E, F, G to MCH1 and MCH2
  - Dual-star routing of CLK1 to TCLKA (MCH1) and CLK1 to FCLKA (MCH2)

Review: uTCA Ports Use for CMS

Fabric	AMC Port	MCH1	MCH2	Category	MCH Finger	CMS Use
A	0	Yes		Common Options	1	GbE
	1		Yes			DAQ / Controls
B	2	Yes			2	Spare
	3		Yes			Synchronous Controls
Clock	TCLKA	CLK1/2		Clocks		Spare
	FCLKA		CLK1/2			LHC Clock
D-G	4-7	Yes		Fat Pipes	3, 4	User
	8-11		Yes			
H-K	12-15			Extended Fat Pipes		
	16-19					

Review: Fabrics A, B Use

- Port 0 is GbE sourced from commercial MCH1
- Port 1 – Compatible with Xilinx GTP (<= 3.125 Gb/s)
  - DAQ data from AMC to MCH2
  - *May* be used also for fixed-latency controls (TTC)
  - *May* be used also for buffer status (TTS)
  - *May* be used also for auxiliary data (selective readout)
- Port 3 – "Low speed" serial LVDS (80-400 Mb/s)
  - Fixed-latency controls (TTC)
  - Buffer status (TTS)
  - Auxiliary data (selective readout)

Review: Fabrics D and up

- Use not mandated by this WG
- Mainly for trigger users
- Two options for interconnection
  - Star connection to tongue 3, 4 of MCH slots
    - Interconnect passively or with crosspoint switch at MCH
  - Fixed connections on backplane
  - Or, a combination:
    - Ports 4-7 interconnected on backplane
    - Ports 8-12 routed to crosspoint switch on MCH2